Quick Reference Table

The table helps you quickly find information on specific jumpers and connectors.

Jumper/ Connector	Setting / Description	Page
JP1	EXTERNAL BATTERY	20
JP3	FLASH ROM VPP SUPPLY	12
JP5,JP10-14	CACHE JUMPERS	11
JP6-8	CLOCK GENERATOR SELECTOR	10
JP15	KEYLOCK & POWER LED CONNECTOR	20
JP16	VESA CLOCK	11
JP17	VESA WAIT STATE	12
JP18	SPEAKER CONNECTOR	19
JP19	TURBO LED CONNECTOR	20
JP20	RESET SWITCH CONNECTOR	21
JP22	TURBO SWITCH CONNECTOR	21
JP23	SUSPEND SWITCH CONNECTOR	11
JP24-26	CPU POWER SELECTOR	11
JP27-30 JP32-33	CPU TYPE SELECTION	10
JP31	80486DX4 CPU CLOCK MULTIPLIER SELECTOR	10
J1	KEY BOARD CONNECTOR	19
J9	POWER SUPPLY CONNECTOR	19

Key Features

The advanced features of the 80486 Deep Green Mainboard include:

- Support microprocessor running at 25/33/40/50/66/75/100 MHz
  -Intel P24T
  -Intel P24D
  -Intel 80486DX4(P24C)
  -Intel 80486DX2/DX/SX-SL
  -Intel 80486DX2/DX/SX
  -Cyrix CX486DX2/DX/S
  -AMD AM486DXLT/DX2/DX
  -UMC U5
- L1 write back or write through cache.
- L2 write back policy for high performance.
- Flexible cache RAM size 64/128/256/512/1024KB in two banks or one bank with 16 bytes line size.
- DRAM auto-dectection / banking.
- Four banks of DRAM with memory size up to 64 MB using combinations of 256K, 1M, 2M, 4M, 8M, 16M, 32MB, 64MB, SIMM modules.
- Providing green PC power management.
- Level 2 cache power saving.
- Four power management modes for SMM (system management mode) CPU: On, Standby, Inactive, Off
  Standard mode: Either put CPU in stop grant state or scaling CPU and system clock.
  Inactive mode: Stop CPU clock.
- Fully support Microsoft APM (advance power management).
- Providing flash ROM support.
- Seven 16-bit I/O slots (including three 32-bit VESA master Local Bus Slots).
- On-board CR2032 3.0 Volt lithium battery.
- ZIF socket
- 3.3 volt for Low Voltage CPU.

1. **System microprocessor**

   The system microprocessor is a high-performance 32-bit 80486SX, 80486DX, 80486DX-2, 80486DX-4, Cyrix 486DX2, 486DX, 486S, AMD AMDXLT, AM486DX2, AM486DX and UMC U5 microprocessor. The 80486 microprocessor is available in seven different clock speeds: 25MHz, 33MHz, 40MHz, 50HMz, 66MHz, 75MHz, or 100MHz.

2. **Integrated System Controller (ISC)**

   The chip contains AT bus control logic, data bus conversion logic, CPU reset logic, clock generating for CPU, keyboard and timer, DMA/refresh logic, peripheral interface logic, page mode DRAM controller, and direct-mapped cache controller with write-back operation.

3. **Chips Integrated Peripherals Controller (IPC)**

   The Chips integrated peripherals controller provides all of the standard peripherals required for system board implementation except the keyboard interface controller. The Chips offers 7 DMA channels, 13 interrupt request channels, 2 timer/counter channels, and a real-time clock.

4 **Cache Memory**

   The on-board cache memory consists of eight SRAM (Static Random Access Memory) chips that contain the cached code and data.

   The cache tag subsystem consists of one SRAM chip that registers the address of the cache data.

5. **Main Memory**

   Four 30pin and two 72pin SIMM sockets are provided for 256k, 1MB, 2MB, 4MB, 8MB, 16MB, 32MB and 64MB Memory can be configured from 1MB to 64 MB.

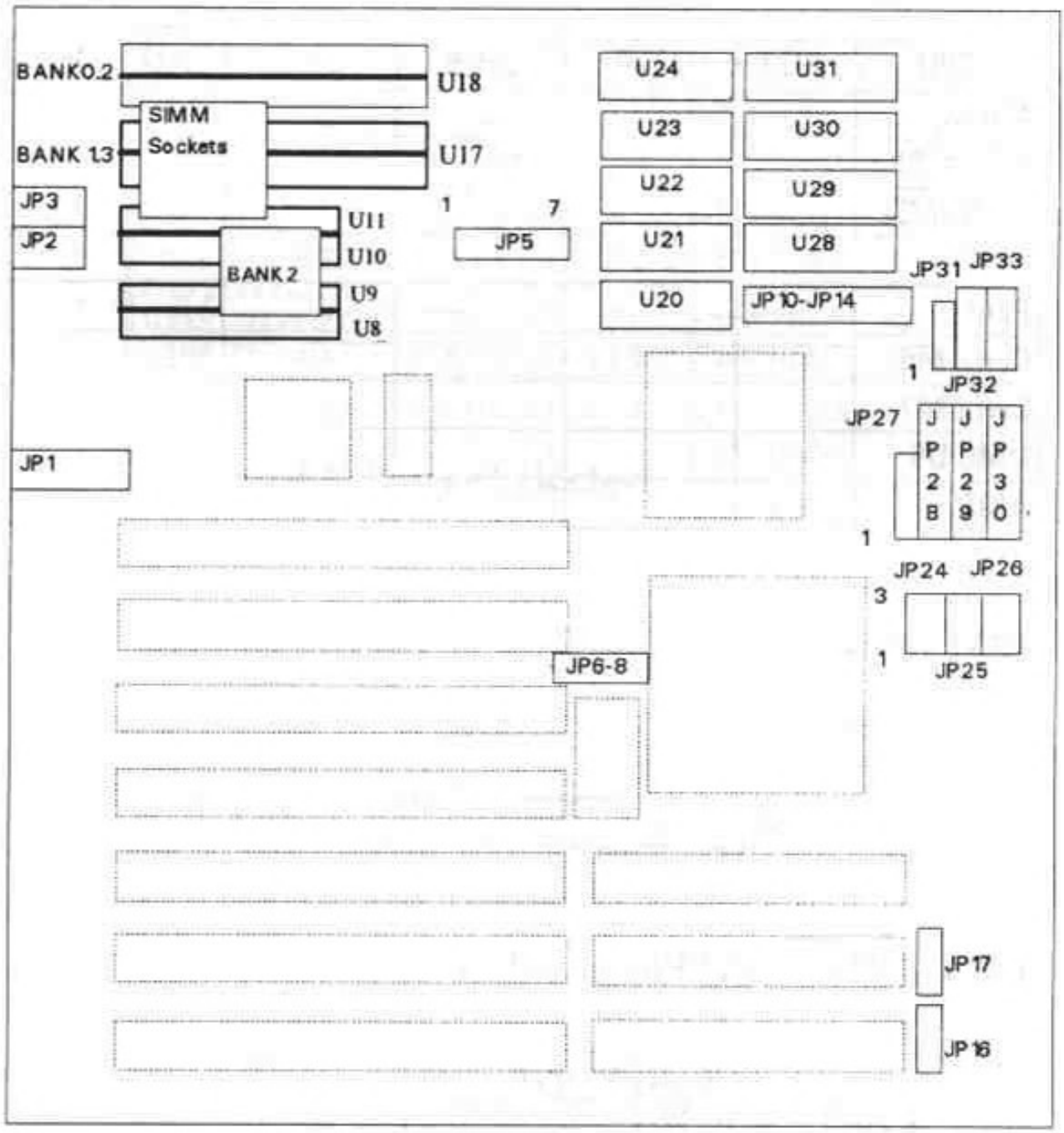
6. **System BIOS**

   The AWARD BIOS is included in this ROM chip. The BIOS lets you control the speed of system, shadow RAM and cache functions by setting up BIOS system.

7. **Expansion slots**

   Seven standard 16-bit ISA bus expansion slots including three 32-bit MASTER Local Bus slots are provided on the mainboard.

Jumper and Socket Locations



JP27 ~JP30,JP32,JP33 - CPU Selectors

Jumpers JP27~JP30,JP32,JP33 configure the mainboard to accept different CPUs.

CPU	JP27	JP28	JP29	JP30	JP32	JP33
486SX	OPEN	2-3	OPEN	OPEN	OPEN	2-3
486DX/DX2	OPEN	2-3	OPEN	OPEN	1-2	1-2,3-4
486DX4/SL	1-2,3-4	1-2	1-2	5-6	1-2	1-2,3-4
P24D	1-2,3-4	1-2,4-5	1-2,4-5	3-4,5-6	1-2	1-2,3-4
P24T	1-2,3-4	1-2	1-2	5-6	2-3	1-2,3-4
Cyrix M6	2-3,4-5	1-2,3-4,5-6	1-2,3-4,5-6	2-3,4-5	OPEN	2-3
Cyrix M7	2-3	1-2,3-4,5-6	1-2,3-4,5-6	2-3,4-5	1-2	1-2,3-4
UMC U5	OPEN	2-3	2-3	1-2	3-4	2-3
AMD	OPEN	2-3	OPEN	OPEN	1-2	1-2,3-4

JP31 - 80486DX4 CPU Clock Multiplier Selector

Jumper	3X	2.5X	2X
INTEL JP31	OPEN	1-2	2-3
AMD JP34	OPEN		ON

JP24~JP26 - CPU Power Selector

	JP24	JP25	JP26	JP35
5 VOLT	2-3	2-3	2-3	
3.3 VOLT	1-2	1-2	1-2	ON
4 VOLT	1-2	1-2	1-2	OFF

JP5,JP10~JP14 - Cache Jumper

Cache Memory size is configured with jumpers JP5, JP10 ~ JP14.

1 BANK	JP5	JP10	JP11	JP12	JP13	JP14
512KB (128Kx8x4)	1-2,3-4,5-6	1-2	OFF	ON	ON	ON
256KB (64Kx8x4)	1-2,3-4	1-2	OFF	OFF	ON	ON
128K(32Kx8x4)	1-2	1-2	OFF	OFF	OFF	ON

2 BANKS	JP5	JP10	JP11	JP12	JP13	JP14
1024KB (128Kx8x8)	2-3,4-5,6-7	2-3	ON	ON	ON	ON
512KB (64Kx8x8)	2-3,4-5	2-3	OFF	ON	ON	ON
256KB (32Kx8x8)	2-3	2-3	OFF	OFF	ON	ON
128KB (16Kx8x8)	2-3	2-3	OFF	OFF	OFF	ON
64KB (8Kx8x8)	2-3	2-3	OFF	OFF	OFF	OFF

JP24~JP26 - CPU Power Selector

	JP24	JP25	JP26
5 VOLT	2-3	2-3	2-3
3.3 VOLT	1-2	1-2	1-2

JP23 - Suspend Switch Connector

In order to force system enter suspend mode, you can attach a push button to this connector.

JP16 - VESA clock

JP16 to be set opened - when CPU Clock <= 33 MHz.
JP16 to be set closed - when CPU Clock > 33 MHz.

	JP16
<=33MHZ	OPEN
> 33MHZ	CLOSE

JP17 - VESA Wait State

The JP17 is VESA wait state setting. 0WS to be opened; 1WS to be closed.

	JP17
0WS	OPEN
1WS	CLOSE

JP3 - Flash ROM VPP Supply Selector

The JP3 is Flash ROM Program Voltage selector. Pin 1 and 2 are shorted in 5 volt; Pin 2 and 3 are shorted in 12 volt.

5 VOLT	1 -2
12 VOLT	2-3

Memory Configuration

The DRAM sub-system contain 4 banks. Four 30-pin SIMM Socket U8 - U11 using as bank 2 ; two 72-pin SIMM Socket U17 using as bank 1 and 3 ; U18 using as bank 0 and 2 . So you can not install 30-pin SIMM if using 2 banks type DRAM on to U18 and you can install 30-pin SIMM if using 1 bank type DRAM on to U18.

U8-U11 BANK2	U18 BANK 0 , 2	U17 BANK 1 , 3
INSTALL	1 BANK TYPE DRAM OR NONE	2 BANKS TYPE DRAM OR 1 BANK TYPE DRAM OR NONE
NONE	2 BANKS TYPE DRAM OR 1 BANK TYPE DRAM OR	2 BANKS TYPE DRAM OR 1 BANK TYPE DRAM OR

Cache Configuration

The 80486 mainboard has a built-in cache controller. It requires external SRAM chips as tag and cache memory. The caching Scheme is direct mapping with write-back operation. The mainboard allows 1024KB cache configurations. Memory size is selected by the hardware jumpers. The BIOS automatically detects cache size.

The speed of the SRAM chips needed depends on the clock speed of the microprocessor:

- **50MHz** and above CPU requires **20ns (tag)** and **20ns (data)** SRAM chips.
- **40MHz** CPU requires **20ns (tag)** and **20ns (data)** SRAM chips
- **33MHz** CPU requires **20ns (tag)** and **20ns (data)** SRAM chips.
- **25MHz** CPU requires **20ns (tag)** and **20ns (data)** SRAM chips

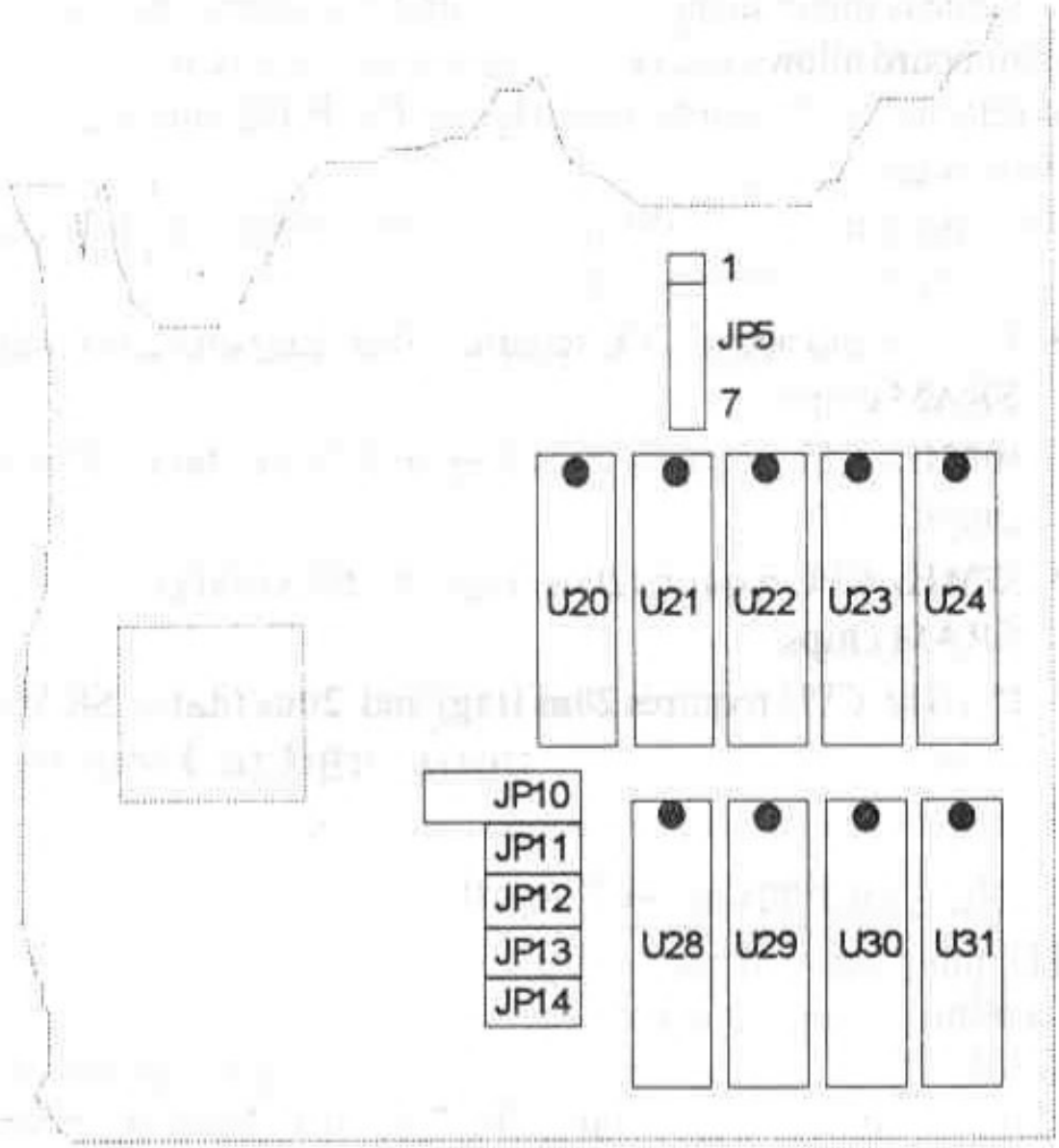
Cache Size and Memory Location

The table below describes the chip capacity and socket location reqired for each cache size configuration. You can use 8K x 8-bit, 32K x 8-bit, 64K x 8-bit, or 128K x 8-bit SRAM chips in banks 0 and 1, and in the TAG RAM sockets. Note that you cannot combine different chip capacities in banks 0 and 1.

	Cache Memory								TAG
Size	U21	U22	U23	U24	U28	U29	U30	U31	U20
64KB	8Kx8	8Kx8	8Kx8	8Kx8	8Kx8	8Kx8	8Kx8	8Kx8	8Kx8
128KB	32Kx8	32Kx8	32Kx8	32Kx8	---	---	---	---	8Kx8
256KB	32Kx8	32Kx8	32Kx8	32Kx8	32Kx8	32Kx8	32Kx8	32Kx8	32Kx8
256KB	64Kx8	64Kx8	64Kx8	64Kx8	---	---	---	---	32Kx8
512KB	64Kx8	64Kx8	64Kx8	64Kx8	64Kx8	64Kx8	64Kx8	64Kx8	32Kx8
512KB	128Kx8	128Kx8	128Kx8	128Kx8	---	---	---	---	32Kx8
1024KB	128Kx8	128Kx8	128Kx8	128Kx8	128Kx8	128Kx8	128Kx8	128Kx8	64Kx8

Cache Chip Sockets and Jumper Locations

The diagram below describes the location of the cache chip sockets and cache jumpers.



Installing Cache Chips

Install Cache chips on the mainboard as follows:

Caution: Static electricity can damage a cache chip.

1. Review the section on static electricity precautions at the beginning of this manual, and make sure that power to the mainboard is off.
2. Align the chip so that the notched corner of the chip