SBX/386

SMX/386 *OEModule*™ Development Board

FEATURES

Includes all PC/AT motherboard functions

1. 33 MHz 80386SX CPU
2. Supports up to 16M bytes using 4M byte SIMMs
3. Full PC core logic—DMA, interrupts, timer/counter, AT keyboard, RTC
4. Full 8- or 16-bit ISA bus and PC/104 bus
5. 2 RS232C serial ports
6. Enhanced (bi-directional) parallel port
7. Super VGA video controller
8. Floppy interface
9. IDE hard disk interface
10. Removable CompactFlash™ solid state disk, 2-80 MB on IDE bus
11. Bootable internal 307KB solid state floppy disk
12. Watchdog timer
13. PC-compatible BIOS
14. DOS operating system
15. 5V only operation
16. Power supply threshold detector

Additional Features

- ◊ Support standard ISA bus cards and PC/104 add-on modules
- ◊ Use as a stand-alone motherboard or in a passive backplane
- ◊ JEDEC byte-wide memory expansion socket

GENERAL DESCRIPTION

OEModules combine system hardware, software, and solid state mass storage in a single compact device.

The SBX/386 represents the fastest way to incorporate a ZFMicroSystems SMX/386 *OEModule* into a fully operational AT-compatible system for hardware and software development. It provides you with a complete PC/AT-compatible motherboard

Rev051096

that can be plugged into a passive backplane, or mounted as a stand-alone motherboard. The board's ISA bus is available at standard edge connectors, or through a standard PC/104 bus header. You can develop software on a PC/AT and transfer your code directly to an SMX/386-equipped embedded system with little or no modification, or you can develop your software directly on the SBX/386 system.

Complete Feature Set

The SBX/386 includes all standard motherboard functions: serial and parallel I/O, floppy and IDE disk controllers, an internal 307 KB resident Flash disk for program storage, an external JEDEC byte-wide socket for additional program storage, ISA and PC/104 expansion buses, a standard AT BIOS, and embedded Mini-DOS.

Industry Standard PC/AT Compatibility

◊ The SBX/386's full compatibility with the two popular PC expansion busses, the PC/AT ISA (Industry Standard Architecture) bus and the PC/104 expansion bus, allows you to easily integrate the widest selection of low-cost hardware peripherals. Install the board in a standard passive backplane for interfacing standard peripherals, or attach standard PC/104 expansion modules directly to the board.

◊ Standard I/O interfaces, serial ports, parallel port, floppy and hard disk interfaces, and SVGA controller allow you to use standard hardware, cables, and software libraries in your development program.

◊ A standard PC ROM-BIOS and embedded Mini-DOS in Flash EPROM let you develop your application software directly on the SMX/386-based hardware it will run on when your project is finished.

SPECIFICATIONS

386SX CPU

◊ Full 32-bit internal architecture, cost-effective 16-bit external bus

◊ Virtual memory, paging, and hardware-enforced protection

DRAM Controller

◊ High performance MUXed DRAM interleave, CPU pipelined operation

◊ Compatible with standard PC SIMMs and page-mode DRAMs (60–70 Ns)

◊ Shadowed BIOS for optimum performance

PC Core Logic

◊ AT-compatible DMA controllers, interrupt controllers, timer/counters

◊ AT keyboard controller

◊ Real-time clock

Serial Ports

◊ Two independent 16450-compatible RS232C serial ports

◊ Standard modem handshake lines

◊ Baud rates up to 115.2 K baud

◊ Second serial port can be programmed to support MIDI data rate (31.25K Baud)

Parallel Port

◊ Fully-compatible PC/AT parallel port

◊ Bi-directional operation

Floppy Disk Controller

◊ Supports all standard PC floppy formats

◊ Software compatible with 72065B controller and PC BIOS

◊ Integrated digital data separator for high reliability and noise immunity

IDE Hard Drive Interface

◊ Full 40-pin interface to standard IDE hard disk drive

◊ Supports up to two IDE drives (master/slave)

Solid State CompactFlash™

◊ SunDisk™ removable cartridge

◊ 2–15 MB (soon up to 80 MB)

◊ Runs on IDE bus

Solid State Flash Storage

◊ 307 KB Flash EPROM available for OS and OEM software

◊ DOS-compatible BIOS in Flash EPROM

◊ 47 KB Flash EPROM available for OEM operating system

◊ Expandable by adding an external Flash memory device to the expansion memory socket

◊ Can be configured to be the boot drive

Expansion Busses

◊ Fully compliant with standard PC/AT expansion bus (ISA)

◊ Fully compliant with the PC/104 expansion bus

SVGA Controller

◊ 512 KB video memory

◊ Fully compatible with VGA standard

◊ Supports high resolution 800x600/256 color and 1024x768/16 color modes (interlaced and non-interlaced)

◊ Supports extended text modes

PC BIOS

◊ Standard AT BIOS functionality

◊ Support for OEM add-ons and special customization

◊ SETUP information stored in non-volatile Flash EPROM. Allows battery-free operation

Disk Operating System

◊ General Software, Inc. Mini-DOS included in all modules.

◊ Supports most PC/AT-compatible operating systems, including MS-DOS

◊ Supports Embedded DOS 6-XL, fully multi-threaded version of the

standard PC DOS. Real-time designs benefit from true multi-threading from the kernel up. Embedded DOS features APIs for non-DOS file systems, and other optional features

Configurable Memory Socket

◊ Supports implementation of an external BIOS

◊ Supports popular byte-wide EPROM, Flash EPROM, and non-volatile SRAM (NVRAM) devices

◊ Occupies all or part of the C0000h–DFFFFh memory region

Watchdog Timer

◊ Multiple tickle sources (system, application, external)

◊ Automatic reset or NMI (jumper selectable) if program goes out of control

Power Monitor

◊ Brownout protection—settable voltage threshold

◊ Provides reliable reset signal if power fluctuates

Electrical Specifications

◊ 5 volt only operation—requires 5VDC @ 1.3 A ±5% (0 MB DRAM)

◊ 2.7 A with 4 1M x 8 SIMMs:

◊ 3.4 A with 4 4M x 8 SIMMs:

◊ Support for low-power modes

Mechanical/Environmental

◊ Standard AT/ISA bus card form factor, 10 in. by 4.5 in.

◊ Standard PC/104 16-bit non-stacking connector for PC/104-compliant modules

◊ Standard ribbon cable connectors for floppy and IDE.

◊ VGA, mini-DIN keyboard and serial COM1 connectors. Ribbon cable connectors for serial COM2 and parallel port

◊ Operating temperature:

◊ 14F to 158F (-10C to 70C)

◊ Storage temperature:

◊ -67F to 185F (-55C to 85C)

◊ Weight: 8.5 oz (241 gm)

◊

ORDERING INFORMATION

SMX-3SX-K-01 Development Kit—Includes SBX/386 OEModule, technical manual, utility software, embedded DOS

SMX-3SX-Q-10 OEModule—SBX/386 OEModule with embedded DOS (no documentation or software)

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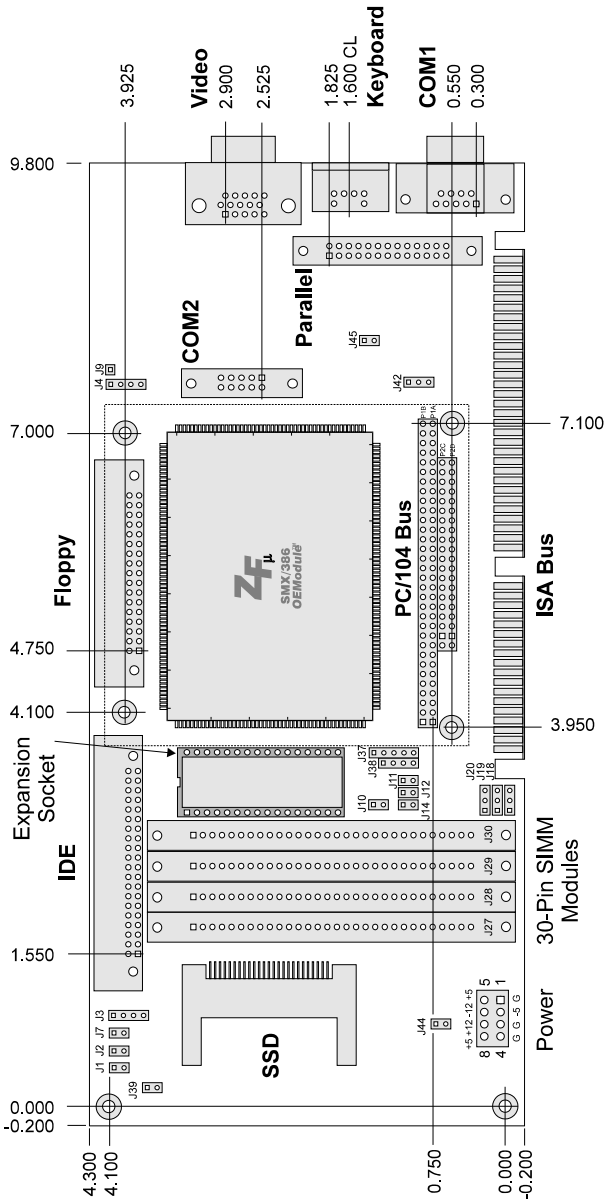


Figure 1. SBX/386 Board Diagram

JUMPER SUMMARY

The SBX/386 provides a number of jumper options to configure features on the board. The jumpers, labeled "J*n*", are configured with .1 inch shorting blocks. Jumpers labeled "W*n*" are cuttable traces and patchable pads.

The following table shows a summary of each jumper, its function, and the factory default setting. For jumper options with more than two pins, default shorted pin-pairs are listed as *n1*/*n2*.

Jumper	Function	Default
J10	BIOS Disable; short accesses BIOS from the memory socket (U6)	OFF
J11, J12, J14	Memory socket (U6); size and address	ON, ON, ON
J18, J19, J20	Watchdog timer;	OFF, OFF, OFF
J37, J38	Memory socket (U6) configuration	
J42	Video interrupt select (IRQ7/IRQ9)	
J44	SanDisk master/slave (ON = master)	ON
J45	Video interlace. (ON = interlaced)	OFF

Table 1. J Jumper Summary

Jumper	Function	Default
W1	Floppy DMA, DRQ2	Connected
W2	Floppy interrupt, IRQ6	Connected
W3	Parallel port interrupt, IRQ7	Connected
W4	Low CPU speed	Not connected
W5	Color/Mono (color = not connected)	Not connected
W6-W9	Video controls (cut to disable video)	Connected
W11	Onboard speaker	Connected
W12-W15	Factory settings	

Table 2. W Jumper Summary

EXTERNAL CONNECTIONS

Several of the jumper blocks are used as small connectors for external devices. These connectors are summarized in Table 3.

Jumper	Function
J1	Power monitor input
J2	Hard disk LED
J3	External speaker
J4	Real-time clock battery
J7	Keyboard lock
J39	External reset switch

Table 3. External Connection Summary

DRAM INTERFACE

The SBX/386 provides a standard DRAM interface for standard 8- and 9-bit 30-pin SIMM modules. The interface is designed to support 70 nS or faster DRAMs.

The 80386 can address up to 16M bytes of memory, limited by the number of address lines provided by the CPU. The SBX/386 can support the full complement of memory.

Installing 30-pin SIMM Modules

A minimum of 1MB of DRAM memory is required for normal operation.

Any standard page-mode 1M x 8, 1M x 9, 4M x 8, or 4M x 9 SIMMs with 70nS (or better) access time can be used. DRAM parity is supported when 9-bit SIMMs are used.

Because of the 16-bit wide DRAM data bus, SIMMs must be installed in pairs. Install the first two SIMMs in sockets J27 and J28.

Setting Memory Size in SETUP

The BIOS automatically senses the amount of memory installed in your system and saves that information in the CMOS SETUP memory when you save the SETUP information. If you change the amount of memory in your system, you must enter SETUP and save the current CMOS values to register the new amount of memory. If the amount of memory in the system does not match the amount saved in CMOS memory, the BIOS displays an error message at boot time.

POWER INTERFACE

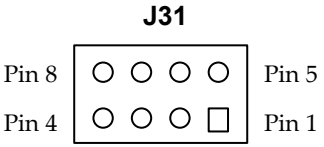
Power to the board may be supplied through the PC/AT edge-card connectors, the PC/104 bus, or through connector J31.

Refer to the PC/AT bus and PC/104 bus tables to determine which pins are used for power. Refer to the following table for how to connect power through J31. A cable is supplied with the ABX development kit to adapt a standard PC power supply motherboard connector to J31.

J31 Pin	Description
1	Ground
2	-5 Volts
3	Ground
4	Ground
5	+5 Volts
6	-12 Volts
7	+12 Volts
8	+5 Volts

Table 4. Power Connector (J31)

Note: The pin numbers of J31 count right-to-left, as shown in the following diagram.



Power Monitoring Circuit

There are two power up/power failure monitoring circuits:

1. When Vcc goes below 4.40V, main the power monitoring circuit resets the board. The duration of the reset pulse is at least 200 ms (this is guaranteed when Vcc is above 1V).

2. The second circuit (optional) monitors an external voltage at input J1. Positions on the circuit board are provided for you (the OEM) to set a voltage threshold for this circuit using component values you choose. Positions for a resistor divider (R1, R2), a diode, and a noise suppression/time delay capacitor (C1) are used to match an internal threshold of 1.25V. When the voltage at the junction of R1/R2 drops below 1.25V, the PFO- signal is generated (active low) until the voltage returns above the threshold.

Jumpers are provided to connect the PFO- signal to one of three inputs:

1. **MR-** This is the master reset input to the system. If PFO- is jumpered to this pin, the system will be reset and will restart when PFO- goes high.

2. **IOCHCHK-** This is an ISA failure signal which activates the Non Maskable Interrupt (NMI). The NMI will occur on the leading edge of PFO-.

3. **RTCIRQ**- This is the Real Time Clock Interrupt, IRQ8, which is often used for RTC alarm outputs. It is a maskable interrupt of lower priority than NMI. The interrupt would occur on the leading edge of PFO-.

The following table shows how to connect the PFO- signal to one of these control signals. Note that the jumper array is shared with the output from the watchdog timer. That is, you can connect the output of the watchdog timer to one of these three control signals as well. The Watchdog Timer output signal (WDO-) will go active (low) if not triggered at least once in each 1.6 seconds. See the section "Watchdog Timer" later in this chapter for details.

	RTCIRQ-	Master Reset (MR-)	IOCHCHK-
Power Fail (PFO-)	J18-2/3	J19-2/3	J20-2/3
Watchdog Timer (WDO-)	J18-1/2	J19-1/2	J20-1/2
Note: Do not attempt to connect both PFO- and WDO- to the same control signal.			

Table 5. Power Fail and Watchdog Timer Output Options

SERIAL INTERFACE

The SBX/386 provides two full-featured PC-compatible asynchronous serial ports. Typically, the serial ports are treated as COM1 and COM2 devices by DOS. Standard system resources are allocated to the serial ports:

Serial Port	Typical Usage	I/O Address	Standard Interrupt
Serial 1	COM1	3F8h–3FFh	IRQ4
Serial 2	COM2	2F8h–2FFh	IRQ3

Table 6. Serial Port Resources

Either or both serial ports can be disabled using SETUP. When disabled, the port's I/O address and interrupt are made available for other expansion devices on the PC bus. The module port drivers are powered-down.

A full complement of input and output handshaking lines are supported by the serial ports. All serial port signals are at standard RS232C levels. The RS232C level converters provide the required RS232C voltage levels with internal +5 volt to ±9 volt converters.

Serial 1 is brought out to a standard DE-9 serial connector on the board's mounting bracket. Serial 2 is brought out to a dual-row ribbon-cable connector at J8. J8's pin out is arranged so that you can construct a simple straight-through ribbon cable to a panel-mount DB9 connector. A PC mounting bracket with an appropriate cable and DE-9 connector is provided with the SBX Development Kit.

DE-9 Pin	J8 Pin	Signal	Function	In/Out
1	1	DCD1	Serial 1 Data Carrier Detect	INPUT
6	2	DSR1	Serial 1 Data Set Ready	INPUT
2	3	RXD1	Serial 1 Receive Data	INPUT
7	4	RTS1	Serial 1 Request To Send	OUTPUT
3	5	TXD1	Serial 1 Transmit Data	OUTPUT
8	6	CTS1	Serial 1 Clear To Send	INPUT
4	7	DTR1	Serial 1 Data Terminal Ready	OUTPUT
9	8	RI1	Serial 1 Ring Indicator	INPUT
5	9	GND	Signal Ground	
	10	N/C	No connection	

Table 7. Serial Port Connections

PARALLEL INTERFACE

The SMX/286 parallel port is fully compatible with the PC/AT parallel port. In the extended mode, it functions as a PS/2-like bi-directional port. The parallel port uses the following PC resources when enabled:

Parallel Port	Typical Usage	I/O Address	Standard Interrupt
Parallel 1	LPT1	378h - 37Fh	IRQ7

Table 8. Parallel Port Resources

The default interrupt for the parallel port is IRQ7. IRQ7 is connected through a cuttable jumper, W3. Cutting the trace between the pads of W3 frees IRQ7 for other uses.

The parallel port output signals provide up to 48 mA drive current (active low). RC filters are provided for noise suppression.

Error: Reference source not found summarizes the parallel port register interface. In this table, "A" indicates the port's base address, 378h:

Register	Bit	Signal Name	In/Out	Active High/Low
DATA (A+0)	0	PD0	I/O	HIGH
	1	PD1	I/O	HIGH
	2	PD2	I/O	HIGH
	3	PD3	I/O	HIGH
	4	PD4	I/O	HIGH
	5	PD5	I/O	HIGH
	6	PD6	I/O	HIGH
	7	PD7	I/O	HIGH
STATUS (A+1))	0	1	-	-
	1	1	-	-
	2	1	-	-
	3	ERROR-	IN	LOW
	4	SLCT-	IN	HIGH
	5	PE	IN	HIGH
	6	ACK-	IN	HIGH
	7	BUSY	IN	LOW

Table 9. Parallel Port Registers

Register	Bit	Signal Name	In/Out	Active High/Low
CONTROL (A+2)	0	STRB-	OUT	LOW
	1	AUTOFD-	OUT	LOW
	2	INIT-	OUT	HIGH
	3	SLCTIN-	OUT	LOW
	4	IRQ ENABLE	-	HIGH
	5	1	-	-
	6	1	-	-
	7	1	-	-

Table 9. Parallel Port Registers (Cont.)

The parallel port signals appear on J40, a dual-row ribbon-cable connector. The port may be cabled to appear on a standard PC DB-25 connector. A DB-25 connector and cable are provided for this purpose on the second I/O bracket provided with the SBX Development Kit. The following table shows the parallel port signals appearing on J40 and the equivalent pinout on a DB-25S connector.

J40 Pin	DB-25S Pin	Signal	Function	In/Out
3	2	PD0	Data bit 0	I/O
5	3	PD1	Data bit 1	I/O
7	4	PD2	Data bit 2	I/O
9	5	PD3	Data bit 3	I/O
11	6	PD4	Data bit 4	I/O
13	7	PD5	Data bit 5	I/O
15	8	PD6	Data bit 6	I/O
17	9	PD7	Data bit 7	I/O
25	13	SLCT	Printer selected	INPUT
23	12	PE	Out of paper	INPUT
21	11	BUSY	Printer busy	INPUT
19	10	ACK-	Character acknowledged	INPUT
8	17	SLCTIN-	Selects printer	OUTPUT
6	16	INIT-	Initialize printer	OUTPUT
4	15	ERR-	Printer error	INPUT
2	14	AUTOFD-	Auto feed	OUTPUT
1	1	STRB-	Output data strobe	OUTPUT
Even 18–24	18–25	GND	Signal Ground	N/A

Table 10. Parallel Port Connections

FLOPPY INTERFACE

A DOS-compatible floppy drive interface is supplied with the SBX/386. This interface allows cable connection to up to four floppy drives. In PC-compatible systems, the BIOS and DOS support just two drives, A: and B:. These are configured using the BIOS SETUP function. Hardware controls for two additional drives are provided by the interface. You must use a floppy driver to support the additional drives.

Table 11 shows the PC resources used by the floppy subsystem.

Resource	Function
I/O Address 3F0h-3F7h	3F2 FDC Digital Output Register (LDOR) 3F4 FDC Main Status Register 3F5 FDC Data Register 3F7 FDC Control Register (LDCR)
IRQ6	Interrupt
DRQ2–DACK2	DMA Controller Channel

Table 11. Floppy Interface Resources

Cuttable trace W2 connects the floppy controller to IRQ6, and cuttable trace W1 connects the floppy DMA request line to DRQ2. If you disable the floppy controller (using SETUP), you may cut the traces between the pads of W1 and W2 to free these resources for other peripherals on the PC bus.

The floppy drive interface supports the following standard floppy formats:

Capacity	Drive Size	Tracks	Data Rate
360K	5-1/4 inch	40	250 KHz
1.2M	5-1/4 inch	80	500 KHz
720K	3-1/2 inch	80	250 KHz
1.44M	3-1/2 inch	80	500 KHz

Table 12. Supported Floppy Formats

You can select the type of drives connected to the floppy interface using the BIOS SETUP function. The first drive appears to DOS as drive A:, and the second drive appears as B:. 1.2M drives can read floppy disks formatted for 360K bytes. 1.44M drives can read floppy disks formatted for 720K bytes.

Floppy drives are normally connected to a system using ribbon cables. The typical PC connection for dual floppy drives uses a special cable with certain ribbon cable wires (conductors 10 through 16) reversed between the two floppy connectors. Using this arrangement, all floppy drives can be jumpered for drive select 1 (the "second" drive). The wires to drive B: are unswapped.

Note: The board's internal Resident Flash Disk, if enabled, will be drive A and any floppy disk drive configured as drive A will become Drive B automatically. Only two floppy drives (A and B) are supported.

J6 Pin	Signal Name	Function	In/Out
2	DENSEL	Speed/Precomp	
4	N/A		N/A
6	N/S	Key pin	N/A
8	INDEX-	Index Pulse	IN
10	MTR0-	Motor On 0	OUT
12	DRV1-	Drive Select 2	OUT
14	DRV0-	Drive Select 1	OUT
16	MTR1-	Motor On 1	OUT
18	DIR-	Direction Select	OUT
20	STEP-	Step Pulse	OUT
22	WDATA-	Write Data	OUT
24	WGATE-	Write Gate	OUT
26	TRK0-	Track 0	INPUT
28	WRPRT-	Write Protect	INPUT
30	RDATA-	Read Data	INPUT
32	HDSEL-	Head Select	OUT
34	DSKCHG-	Disk Change	INPUT
1–33	Ground	Ground	

Table 13. Floppy Drive Interface

IDE DRIVE INTERFACE

The SBX/386 is supplied with a standard IDE Hard Disk Interface. This is the standard interface used in PC-compatible systems for hard disk drives. Up to two drives can be connected, in a master-slave arrangement. Generally, the first hard disk drive (master) will appear as the C drive to DOS. The second drive, if attached, will appear as D.

Note: Due to drive manufacturer's different implementations of the master/slave arrangement, it may not be possible to properly configure drives from different sources to share the IDE bus.

Resource	Function
I/O Address 1F0h-1F7h	Hard Disk Interface
IRQ14	Interrupt

Table 14. Parallel Port Resources

The native IDE interface supports drives of up to 512M bytes each. Disk drive manufacturers typically supply a driver to support drives larger than this limit. (These drivers modify the hard disk's boot record, allowing them to be the boot drive.) Using such drivers, multi-gigabyte drives can be used.

Use SETUP to enable your attached hard drives. You must match the drive parameters in setup with the actual parameters of your connected drive(s). See the SETUP description later in this document for further details about setting up IDE hard disk parameters.

The SBX/386 IDE interface supplies the signals you need to interface to IDE drives. Use an insulation displacement connector that has two rows of pins on .1 inch centers. IDE drives are typically attached to the drive interface with a 40-pin ribbon cable. Miniature drives sometimes require a cable adapter circuit board for translation between the standard .1 inch spacing connector and the smaller connector on the drive. These generally are supplied with the drive.

In some systems, an IDE drive activity LED is desirable. To connect an activity LED to indicate IDE drive activity, connect the LED anode to J2-1 and the LED cathode to J2-2.

IDE Pin	Signal Name	Function	In/Out
1	HDRESET-	Reset signal from host	OUT
2	GND	Ground	OUT
3	HDD07	Data bit 7	I/O
4	HDD08	Data bit 8	I/O
5	HDD06	Data bit 6	I/O
6	HDD09	Data bit 9	I/O
7	HDD05	Data bit 5	I/O

8	HDD10	Data bit 10	I/O
9	HDD04	Data bit 4	I/O
10	HDD11	Data bit 11	I/O
11	HDD03	Data bit 3	I/O
12	HDD12	Data bit 12	I/O
13	HDD02	Data bit 2	I/O
14	HDD13	Data bit 13	I/O
15	HDD01	Data bit 1	I/O
16	HDD14	Data bit 14	I/O
17	HDD00	Data bit 0	I/O
18	HDD15	Data bit 15	I/O
19	GND	Ground	OUT
20	KEY	Keyed pin	N/C
21	N/A	Reserved	N/C
22	GND	Ground	OUT
23	HDIOW-	Write strobe	OUT
24	GND	Ground	OUT
25	HDIOR-	Read strobe	OUT
26	GND	Ground	OUT

Table 15. IDE Drive Interface

IDE Pin	Signal Name	Function	In/Out
27	RSVD	Reserved	N/C
28	HDALE	Address latch enable	OUT
29	RSVD	Reserved	N/C
30	GND	Ground	OUT
31	HED14	Drive interrupt request	IN

Table 16. IDE Drive Interface (Cont.)

NOTE: For maximum reliability, limit IDE drive cables to less than 18 inches long.

MEMORY SOCKET

A standard 32-pin JEDEC-compatible memory socket is provided at U6. You may install a Flash EPROM or standard EPROM in this socket. A variety of memory device types are supported.

Use J11, J12, and J14 to select the socket's memory address space size using Table 17.

Note: The address space defined by the memory address jumpers (J11, J12, and J14) will be occupied by the memory socket even if no memory device is installed. Set the socket's configuration jumpers to their default setting (disabled) to make the memory address space available for other devices.

Size and Address	J11	J12	J14
Disabled*	ON	ON	ON
16K bytes at DC000h	ON	ON	OFF
32K bytes at D8000h	OFF	OFF	ON
64K bytes at D0000h	ON	OFF	OFF
80K bytes at CC000h	OFF	ON	ON
96K bytes at C8000h	OFF	ON	OFF
112K bytes at C4000h	OFF	OFF	ON
128K bytes at C0000h	OFF	OFF	OFF
* This is also the setting for installing an external BIOS in U6. (See details below.)			

Table 17. Memory Socket Size and Address Selection

The address decode logic set by J11, J12, and J14 selects only the address range indicated, allowing other devices, (e.g. BIOS extensions) at lower regions.

Installing an External BIOS

When J10, J11, J12 and J14 are jumpered (shorted), the memory socket can be used for an external BIOS PROM of 64 or 128 KB. The lower 64KB will be mapped to F000:0 (the BIOS) and the higher 64KB (if any) will be mapped to D000:0, allowing it to be copied into the E000:0 region if desired.

Memory Socket Signal Jumpers

These jumpers support JEDEC memory pinouts for 28- and 32-pin DIP devices. The socket's address window can be set to a maximum of 128K bytes, therefore larger devices are not supported.

When installing a 28-pin device, install pin 1 of the device in U6-3. A 28-pin device does not connect to socket pins 1, 2, 31, and 32.

Use J37 and J38 to supply the appropriate signals to your installed memory device. Figure 2 shows the signals appearing on J37 and J38.

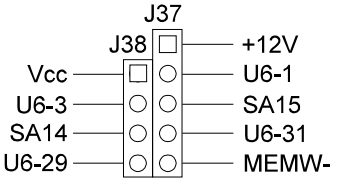


Figure 2. Expansion Socket Configuration Options

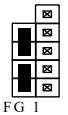
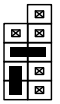
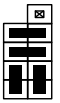
Device	Size	Jumper Diagram
EPROM		
27C256	32K bytes	 CFG 1
27C512	64K bytes	 CFG 2
27C010	128K bytes	 CFG 3

Table 18. Expansion Socket Jumpers for Typical Devices

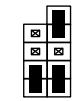
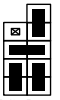
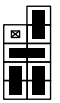
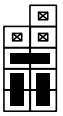
Device	Size	Jumper Diagram
Flash EPROM		
28F256A	32K bytes	 CFG 4
28F512	64K bytes	 CFG 5
28F010	128K bytes	 CFG 5
AM29F020	128K bytes	 CFG 6

Table 19. Expansion Socket Jumpers for Typical Devices (Cont.)

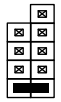
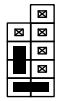
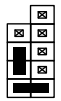
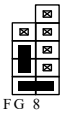
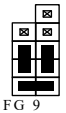
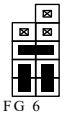
Device	Size	Jumper Diagram
NVRAM Devices		
Dallas DS1225Y	8K bytes	 CFG 7
Dallas DS1230	32K bytes	 CFG 8
Dallas DS1235Y	32K bytes	 CFG 8
Dallas DS1630	32K bytes	 CFG 8
Dallas DS1245Y	128K bytes	 CFG 9
Dallas DS1645Y	128K bytes	 CFG 6

Table 19. Expansion Socket Jumpers for Typical Devices (Cont.)

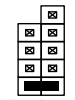
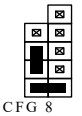
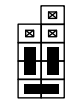
Device	Size	Jumper Diagram
NVRAM Devices		
Benchmarq BQ4010Y	8K bytes	 CFG 7
Benchmarq BQ4011Y	32K bytes	 CFG 8
Benchmarq BQ4013Y	128K bytes	 CFG 9

Table 19. Expansion Socket Jumpers for Typical Devices (Cont.)

WATCHDOG TIMER

The watchdog timer will alarm if not triggered by the system or application at least once every 1.6 seconds. If the watchdog timer does not receive its reset ("tickle") when 1.6 seconds has elapsed, it generates its alarm signal. The watchdog timer alarm is reset ("tickled") by toggling the WDI signal which is also the signal MTR3, the motor control for the fourth floppy drive. By default, the module's BIOS will toggle the MTR3 signal every RTC interrupt (approximately 18 times per second) to keep the WDT from alarming. An application can take over the tickle function by making calls to WDT functions in the BIOS. An explanation of the WDT API (application programming interface) is provided in the BIOS API document available from ZF MicroSystems. Contact your ZF MicroSystems sales representative for details.

The watchdog timer alarm signal (WDO-) can be jumpered to one of three supervisory signals:

1. **MR-** This is the master reset input to the system. If WDO- is jumpered to this pin, the system will be reset and will restart when WDO- goes high.

2. **IOCHCHK-** This is an ISA failure signal which activates the Non Maskable Interrupt (NMI). The NMI will occur on the leading edge of WDO-.

3. **RTCIRQ**- This is the Real Time Clock Interrupt, IRQ8, which is often used for RTC alarm outputs. It is a maskable interrupt of lower priority than NMI. The interrupt would occur on the leading edge of WDO-.

The following table shows how to connect the WDO- signal to one of these control signals. Note that the jumper array is shared with the output from the powerfail monitor. That is, you can connect the output of the powerfail monitor to one of these three control signals as well. The powerfail monitor output signal (PFO-) will go active (low) if power conditions violate the internal thresholds. See the section "Power Interface" earlier in this chapter for details.

	RTCIRQ-	Master Reset (MR-)	IOCHCHK-
Watchdog Timer (WDO-)	J18-1/2	J19-1/2	J20-1/2
Power Fail (PFO-)	J18-2/3	J19-2/3	J20-2/3
Note: Do not attempt to connect both PFO- and WDO- to the same control signal.			

Table 19. Power Fail and Watchdog Timer Output Options

KEYBOARD PORT

The SBX/386 keyboard port provides a standard miniature 5-pin DIN connector typical of standard PS/2 keyboards. This connector appears at the back of the board, at J23. The following table lists the pins on this connector.

Ground return5KEYBOARD POWERKeyboard Power (+5 VDC)5-Pin DIN	**Signal Name**	Function2
KDATAKeyboard Data1KCLOCKKeyboard Clock4GROUND		

Table 20. Keyboard Connections

Keyboard Lock

The SBX/386 also provides a keyboard lock mechanism. Shorting J7-1 to J7-2 (ground) disables keyboard input.

SPEAKER PORT

A small piezoelectric speaker is provided on the SBX/386 board. In addition, a standard PC speaker connector appears at J3. To connect an external speaker (typically a small 8-ohm speaker) connect it to J3 as shown in Table 21. Standard cables (provided with PC enclosures) connect the speaker between pins 1 and 4. To disconnect the onboard speaker, cut the trace between the pads labeled W11. The port supplies approximately 0.1 watt to the speaker.

J3 Pin	Signal
1	+ Output
2	Key, no connection
3	Ground
4	+5 Volts

Table 21. External Speaker Connections

REAL-TIME CLOCK

The real-time clock requires a 3.6 volt lithium cell to maintain the correct time, date, and CMOS memory values when power is off. Connect the battery to J4 as shown in the following table. The battery uses the standard wiring found on most PC/AT motherboards.

If the battery is not present and power is removed the RTC will lose the current Time and Date, but the SETUP data will remain intact. The "CMOS" is always read from a Flash EPROM copy (inside the SMX/386) if there is a fault in the "CMOS" version of the setup parameters.

J4 Pin	Signal
1	Battery + terminal
2	No connection
3	No connection
4	Battery - terminal (Ground)

Table 22. Backup Battery Connections

SVGA CONTROLLER

The onboard SVGA controller supports resolutions up to 800x600 in 256 colors and up to 1024x768 in 16 colors, interlaced or non-interlaced. It includes a fully PC compatible Video BIOS and hardware-level register compatibility with existing PC video standards. The CRT video signals are brought out to a standard PC high-density DE-15 connector. Most PC-compatible multifrequency monitors will cable directly to this connector. A list of the signals provided on the video connector is provided in Table 23.

DE-15 Pin	Signal
1	Red
2	Green
3	Blue
13	Horizontal Sync
14	Vertical Sync
5, 6, 7, 8, 10	Ground
4, 9, 11, 12, 15	No connection

Table 23. Video Connector

Interlace Jumper

Jumper **J45** controls interlace/non-interlace. Leave J45 open for non-interlace monitors (the default).

Interrupt Jumper

Jumper **J42** selects the vertical retrace interrupt used by some programs to synchronize the display with changes in screen content. (It is rarely used. The BIOS does not use this interrupt.) The usual interrupt for this function is IRQ9. J42 provides two choices, IRQ9 and IRQ7. To select IRQ9, jumper pin 2 to pin 3. To use IRQ7, jumper pin 1 to pin 2. Note that if you use IRQ7, you must cut W3 to disconnect it from the parallel port.

REMOVABLE SOLID STATE DISK

A connector is provided for a SanDisk™ CompactFlash™ (CF) card. Connected to the IDE bus, these CF cards can provide 2 to 15 M bytes or more of removable "disk" storage. Documentation for the SanDisk interface is provided in separate manual.

EXPANSION BUS INTERFACE

Addr ess bit 19I/ OIO 12A 13S A18 Addr ess bit 18I/ OIO 12A 14S A17 Addr ess bit 17I/ OIO 12A 15S A16 Addr ess bit 16I/ OIO 12A 16S A15 Addr ess bit 15I/ OIO 12A 17S A14 Addr	AEN	Address Enable	I/O	O6	

ess bit 14I/ OIO 12A 18S A13 Addr ess bit 13I/ OIO 12A 19S A12 Addr ess bit 12I/ OIO 12A 20S A11 Addr ess bit 11I/ OIO 12A 21S A10 Addr ess bit 10I/ OIO 12PinSignal NameFunctionIn/outTypeL					

oad* A1I OCH CK- Bus NMI input InPU 4.7K A2S D7S yste m Data bit 7I/OI O24 A3S D6S yste m Data bit 6I/OI O24 A4S D5S yste m Data bit 5I/OI O24 A5S D4S yste m Data bit 4I/OI O24 A6S D3S yste m					

Data bit 3I/OIO24 A7SD2System Data bit 2I/OIO24 A8SD1System Data bit 1I/OIO24 A9SD0System Data bit 0I/OIO24 A10IOCHRDY Processor Ready CtrlInPU 1KA11					

A22SA9Address bit 9I/OIO12A23SA8Address

bit
8I/OIO12A24
SA7Address
bit
7I/OIO12A12
SA19

Table 24. Expansion Bus Connector, A1–A32

Address bit 5I/OIO12 A27 SA4 Address bit 4I/OIO12 A28 SA3 Address bit 3I/OIO12 A29 SA2 Address bit 2I/OIO12 A30 SA1 Address bit 1I/OIO12 A31 SA0 Address bit 0I/OIO12 A32 GND PC/1	SA6	Address bit 6	I/O	IO12	

04 GroundPinSignal NameFunctionIn/outCurrentLoad*A25					

A26SA5

Table 24. Expansion Bus Connectors, A1–A32 (Cont.)

Notes for Table

* PU = pull up.
All values in ohms.
A32 appears only on the PC/104 bus connector.

Pin	Signal Name	Function	In/out	Current	Load*
B1	GND	Ground	N/A		
B2	RESETDRV	System reset signal	Out	OC8	
B3	+5V	+5 volt power	N/A		
B4	IRQ9	Interrupt request 9	In		
B5	-5V	To J7 pin 5	N/A		
B6	DRQ2	DMA request 2	In		
B7	-12V	To J7 pin 6	N/A		
B8	ENDXFR- (0WS-)	Zero wait state	In		PU 300
B9	+12V	To J7 pin 4	N/A		
B10					
B11	SMEMW-	Mem Write (lower 1MB)	I/O	O12	
B12	SMEMR-	Mem Read (lower 1MB)	I/O	O12	
B13	IOW-	I/O Write	I/O	O12	
B14	IOR-	I/O Read	I/O	O12	
B15	DACK3-	DMA Acknowledge 3	Out	O6	
B16	DRQ3	DMA Request 3	In		
B17	DACK1-	DMA Acknowledge 1	Out	O6	
B18	DRQ1	DMA Request 1	In		
B19	REFRESH-	Memory Refresh	I/O	OC8	
B20	SYSCLK	System clock (8 MHz)	Out	O12	
B21	IRQ7	Interrupt Request 7	In		
B22	IRQ6	Interrupt Request 6	In		
B23	IRQ5	Interrupt Request 5	In		
B24	IRQ4	Interrupt Request 4	In		

Table 25. Expansion Bus Connector, B1–B31

Pin	Signal Name	Function	In/out	Current	Load*
B25	IRQ3	Interrupt Request 3	In		
B26	DACK2-	DMA Acknowledge 2	Out	O6	
B27	TC	DMA Terminal Count	Out	O4	
B28	BALE	Address latch enable	Out	12 mA	
B29	+5V	+5 volt power			
B30	OSC	14.318 MHz clock	Out	O6	
B31	GND	Ground			
B32	GND	PC/104 Ground			

Table 26. Expansion Bus Connectors, B1–B32

Notes for Table

* PU = pull up.
All values in ohms.
B32 only appears on the PC/104 bus connector.

Pin	Signal name	Function	In/out	Current	Load*
C0	GND	PC/104 Ground			
C1	SBHE-	Bus High Enable	I/O	IO6	
C2	LA23	Address bit 23	I/O	IO24	
C3	LA22	Address bit 22	I/O	IO24	
C4	LA21	Address bit 21	I/O	IO24	
C5	LA20	Address bit 20	I/O	IO24	
C6	LA19	Address bit 19	I/O	IO24	
C7	LA18	Address bit 18	I/O	IO24	
C8	LA17	Address bit 17	I/O	IO24	
C9	MEMR-	Memory Read	I/O	IO12	
C10	MEMW-	Memory Write	I/O	IO12	
C11	SD8	System Data bit 8	I/O	IO24	
C12	SD9	System Data bit 9	I/O	IO24	
C13	SD10	System Data bit 10	I/O	IO24	
C14	SD11	System Data bit 11	I/O	IO24	
C15	SD12	System Data bit 12	I/O	IO24	
C16	SD13	System Data bit 13	I/O	IO24	
C17	SD14	System Data bit 14	I/O	IO24	
C18	SD15	System Data bit 15	I/O	IO24	
C19	GND	PC/104 Ground			

Table 27. Expansion Bus Connectors, C0–C19

Notes for Table

PU = pull up.
All values in ohms.
C0 and C19 only appear on the PC/104 bus connector.

Pin	Signal Name	Function	In/out	Current	Load*
D0	GND	PC/104 Ground			
D1	MEMCS16-	16-bit Mem access	In		PU 300
D2	IOCS16-	16-bit I/O access	In		PU 300
D3	IRQ10	Interrupt Request 10	In		
D4	IRQ11	Interrupt Request 11	In		
D5	IRQ12	Interrupt Request 12	In		
D6	IRQ15	Interrupt Request 15	In		
D7	IRQ14	Interrupt Request 14	In		
D8	DACK0-	DMA Acknowledge 0	Out	O6	
D9	DRQ0	DMA Request 0	In		
D10	DACK5-	DMA Acknowledge 5	Out	O6	
D11	DRQ5	DMA Request 5	In		
D12	DACK6-	DMA Acknowledge 6	Out	O6	
D13	DRQ6	DMA Request 6	In		
D14	DACK7-	DMA Acknowledge 7	Out	O6	
D15	DRQ7	DMA Request 7	In		
D16	+5V	+5 volt power	N/A		
D17	MASTER-	Bus master assert	In		PU 300
D18	GND	Ground	N/A		
D19	GND	PC/104 Ground			

Table 28. Expansion Bus Connectors, D0–D19

Notes for Table

* PU = pull up.
All values in ohms.
D0 and D19 only appear on the PC/104 bus connector.

BIOS SETUP

The SBX/386 system BIOS (Basic Input Output System) supports a standard SETUP function to configure system parameters. The BIOS uses these parameters to establish default conditions during system initialization, both during the Power On Self Test (POST) phase, and during system boot.

SETUP parameters are stored in non-volatile memory in the resident SMX/386 module.

Using SETUP

To enter the SETUP function, press the <DEL> key during POST. Del can be asserted at any time prior to boot.

Note: When you change SETUP parameters, the new values do not take effect until the system is rebooted.

There are three SETUP screens:

- ◊ **Main Menu Screen**—Displays a top-level of SETUP choices
- ◊ **Basic CMOS Configuration**—Use this screen to set the standard CMOS options
- ◊ **Advanced CMOS Configuration**—Use this screen to set a set of advanced options

For details about how to set the various parameters using SETUP, refer to the SMX/386 OEModule™ documentation.

EMBEDDED DOS

Each SBX/386 has General Software's Mini-DOS installed in Flash memory internal to the SMX/386 module. The system is set up to boot directly from Mini-DOS.

Full documentation of the many features and functions of Mini-DOS is beyond the scope of this manual. Full documentation is provided in a separate manual.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS*

Absolute Maximum Voltage on any pin, with respect to Ground .....-0.3V – 6.5V

Storage Temperature (case) .....-55°C – 80°C (-67°F – 176°F)

OPERATING CONDITIONS*

Supply Voltage (V_{CC}) .....4.75V – 5.25V

Case Temperature (under bias) .....-10°C – 70°C (14°F – 158°F)

*** Stresses above those listed above can cause permanent damage to the board. These values are stress ratings only, and do not imply that the device should be operated at these extremes. Exposure beyond the "Operating Conditions" may affect device reliability. Note that some power supplies exhibit voltage spikes when AC power is switched on or off, or when voltage transients appear on the AC power line. If this possibility exists, it is suggested that you use a clamp circuit on the DC supply.**

LITERATURE REFERENCES

The following references are for information about the PC architecture, the 386SX microprocessor, the PC DOS, and the PC BIOS.

ISA System Architecture

MindShare, Inc., Tom Shanley and Don Anderson
Internet: mindshar@interserv.com
CompuServe: 72507,1054
Published by Addison Wesley, Inc.

AT Bus Design

Edward Solari
Anabooks
12145 Alta Carmel Ct., Suite 250
San Diego, CA 92128
ISBN 0-929392-08-6

Personal Computer Bus Standard P996

Institute of Electrical and Electronic Engineers, Inc.
445 Hoes Lane
Piscataway, NJ 08854

PC Interrupts

PC Interrupts, Ralf Brown, Addison/Wesley.

MS-DOS References

MS-DOS Functions, Ray Duncan, Microsoft Press

MS-DOS Programmer's Reference, Microsoft Press, Microsoft Corporation

Undocumented DOS, Andrew Schulmen, Addison/Wesley

BIOS Reference

System BIOS for IBM PC/XT/AT Computers, Phoenix, Addison/Wesley

Technical data on the 386SX microprocessor:

386 SX Microprocessor Programmer's Reference Manual
Intel
1751 Fox Drive
Suite 29000
San Jose, CA 95131

Technical data on Embedded DOS 6-XL

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The LIM 4.0 Expanded Memory Specification:

Lotus/Intel/Microsoft Expanded Memory Specification, Version 4.0
Lotus Development Corporation
55 Cambridge Parkway
Cambridge, MA 02142

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