1 INSTALLING SYSTEM MEMORY

Dynamic Random Access Memory (DRAM) is essential system memory. It can be configured from 2 MB to 128 MB using 36-bit SIMMs (Single In-line Memory Modules). This is the only type of memory which can be installed by the user.

1.01 STATIC ELECTRICITY PRECAUTIONS

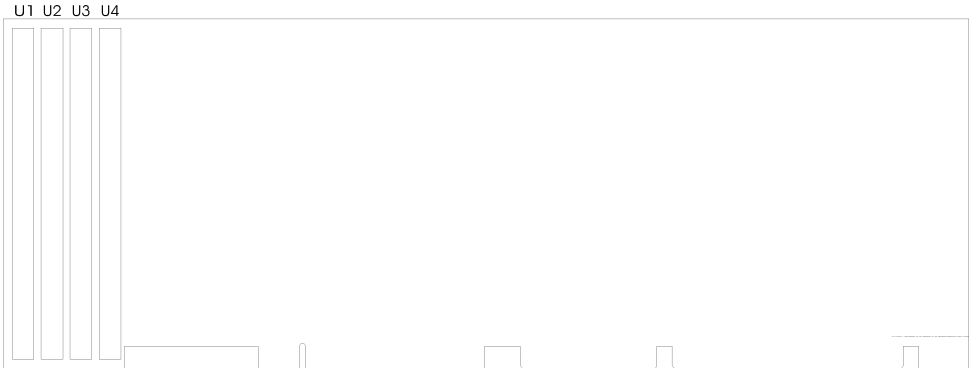
Since static electricity can damage a board, the following precautions should be taken whenever you handle the TEK932:

- Keep the board in its antistatic package, until you are ready to install it.
- Touch a grounded surface before removing the board from its package or wear a grounding wrist strap; this will discharge any static electricity that may have built up in your body.
- Handle the board by the edges.
- When handling the board, touch a grounded surface often or wear a grounding wrist strap.

1.02 LOCATION OF SIMM SOCKETS

The location of the four 72-pin vertical SIMM sockets appear on Diagram 1-1 and are labeled U1, U2, U3 and U4.

DIAGRAM 1-1: SIMM Sockets Location



1.03 SIMM CONFIGURATION

At least 2 MB of system memory must be installed on the TEK932 for proper operation.

Each of the 72-pin vertical SIMM sockets on the board can accept the following 36-bit modules:

- 256 K x 36-bit = 1 MB module,
- 512 K x 36-bit = 2 MB module,
- 1 M x 36-bit = 4 MB module,
- 2 M x 36-bit = 8 MB module,
- 4 M x 36-bit = 16 MB module, and
- 8 M x 36-bit = 32 MB module.

SIMM modules must be installed in either two or four sockets:

- In U4 and U3, or
- In U2 and U1, or
- In U4, U3, U2 and U1.

SIMMs installed in U4 and U3 must be of the same capacity; likewise, U2 and U1 must be of the same capacity (however, SIMMs in U4-U3 may of a different capacity than those in U2-U1).

Consult the tables on the following pages to see which SIMM configurations are supported by the TEK932.

DRAM devices with page mode at 70 ns maximum access time is recommended. Please refer to Appendix D for a list of recommended devices.

TABLE 1-1a: TEK932 SIMM Configurations: 2 MB - 24 MB

TOTAL SYSTEM MEMORY	U4	U3	U2	U1
2 MB	1 MB (256Kx36)	1 MB (256Kx36)	--	--
2 MB	--	--	1 MB (256Kx36)	1 MB (256Kx36)
4 MB	1 MB (256Kx36)	1 MB (256Kx36)	1 MB (256Kx36)	1 MB (256Kx36)
4 MB	2 MB (512Kx36)	2 MB (512Kx36)	--	--
4 MB	--	--	2 MB (512Kx36)	2 MB (512Kx36)
6 MB	2 MB (512Kx36)	2 MB (512Kx36)	1 MB (256Kx36)	1 MB (256Kx36)
6 MB	1 MB (256Kx36)	1 MB (256Kx36)	2 MB (512Kx36)	2 MB (512Kx36)
8 MB	2 MB (512Kx36)	2 MB (512Kx36)	2 MB (512Kx36)	2 MB (512Kx36)
8 MB	4 MB (1Mx36)	4 MB (1Mx36)	--	--
8 MB	--	--	4 MB (1Mx36)	4 MB (1Mx36)
10 MB	4 MB (1Mx36)	4 MB (1Mx36)	1 MB (256Kx36)	1 MB (256Kx36)
10 MB	1 MB (256Kx36)	1 MB (256Kx36)	4 MB (1Mx36)	4 MB (1Mx36)
12 MB	4 MB (1Mx36)	4 MB (1Mx36)	2 MB (512Kx36)	2 MB (512Kx36)
12 MB	2 MB (512Kx36)	2 MB (512Kx36)	4 MB (1Mx36)	4 MB (1Mx36)
16 MB	4 MB (1Mx36)	4 MB (1Mx36)	4 MB (1Mx36)	4 MB (1Mx36)
16 MB	8 MB (2Mx36)	8 MB (2Mx36)	--	--
16 MB	--	--	8 MB (2Mx36)	8 MB (2Mx36)
18 MB	8 MB (2Mx36)	8 MB (2Mx36)	1 MB (256Kx36)	1 MB (256Kx36)
18 MB	1 MB (256Kx36)	1 MB (256Kx36)	8 MB (2Mx36)	8 MB (2Mx36)
20 MB	8 MB (2Mx36)	8 MB (2Mx36)	2 MB (512Kx36)	2 MB (512Kx36)
20 MB	2 MB (512Kx36)	2 MB (512Kx36)	8 MB (2Mx36)	8 MB (2Mx36)
24 MB	8 MB (2Mx36)	8 MB (2Mx36)	4 MB (1Mx36)	4 MB (1Mx36)
24 MB	4 MB (1Mx36)	4 MB (1Mx36)	8 MB (2Mx36)	8 MB (2Mx36)

TABLE 1-1b: TEK932 SIMM Configurations: 32 MB - 128 MB

TOTAL SYSTEM MEMORY	U4	U3	U2	U1
32 MB	8 MB (2Mx36)	8 MB (2Mx36)	8 MB (2Mx36)	8 MB (2Mx36)
32 MB	16 MB (4Mx36)	16 MB (4Mx36)	--	--
32 MB	--	--	16 MB (4Mx36)	16 MB (4Mx36)
34 MB	16 MB (4Mx36)	16 MB (4Mx36)	1 MB (256Kx36)	1 MB (256Kx36)
34 MB	1 MB (256Kx36)	1 MB (256Kx36)	16 MB (4Mx36)	16 MB (4Mx36)
36 MB	16 MB (4Mx36)	16 MB (4Mx36)	2 MB (512Kx36)	2 MB (512Kx36)
36 MB	2 MB (512Kx36)	2 MB (512Kx36)	16 MB (4Mx36)	16 MB (4Mx36)
40 MB	16 MB (4Mx36)	16 MB (4Mx36)	4 MB (1Mx36)	4 MB (1Mx36)
40 MB	4 MB (1Mx36)	4 MB (1Mx36)	16 MB (4Mx36)	16 MB (4Mx36)
48 MB	16 MB (4Mx36)	16 MB (4Mx36)	8 MB (2Mx36)	8 MB (2Mx36)
48 MB	8 MB (2Mx36)	8 MB (2Mx36)	16 MB (4Mx36)	16 MB (4Mx36)
64 MB	16 MB (4Mx36)	16 MB (4Mx36)	16 MB (4Mx36)	16 MB (4Mx36)
64 MB	32 MB (8Mx36)	32 MB (8Mx36)	--	--
64 MB	--	--	32 MB (8Mx36)	32 MB (8Mx36)
66 MB	32 MB (8Mx36)	32 MB (8Mx36)	1 MB (256Kx36)	1 MB (256Kx36)
66 MB	1 MB (256Kx36)	1 MB (256Kx36)	32 MB (8Mx36)	32 MB (8Mx36)
68 MB	32 MB (8Mx36)	32 MB (8Mx36)	2 MB (512Kx36)	2 MB (512Kx36)
68 MB	2 MB (512Kx36)	2 MB (512Kx36)	32 MB (8Mx36)	32 MB (8Mx36)
72 MB	32 MB (8Mx36)	32 MB (8Mx36)	4 MB (1Mx36)	4 MB (1Mx36)
72 MB	4 MB (1Mx36)	4 MB (1Mx36)	32 MB (8Mx36)	32 MB (8Mx36)
80 MB	32 MB (8Mx36)	32 MB (8Mx36)	8 MB (2Mx36)	8 MB (2Mx36)
80 MB	8 MB (2Mx36)	8 MB (2Mx36)	32 MB (8Mx36)	32 MB (8Mx36)
96 MB	32 MB (8Mx36)	32 MB (8Mx36)	16 MB (4Mx36)	16 MB (4Mx36)
96 MB	16 MB (4Mx36)	16 MB (4Mx36)	32 MB (8Mx36)	32 MB (8Mx36)
128 MB	32 MB (8Mx36)	32 MB (8Mx36)	32 MB (8Mx36)	32 MB (8Mx36)

1.04 SIMM INSTALLATION

When you are ready to install the SIMMs in the sockets, follow the steps outlined below.

- With the board flat on the table, turn it so that the sockets are at the end of the board farthest from you.

- Hold the module with the notch on the bottom right facing you, and insert the connector into the socket at a 70° angle from the board.

- Snap the module to a vertical position in the socket. The module is fully inserted when the retaining pegs snap into the holes at each end of the module.

2 JUMPER LOCATIONS & CONFIGURATION

2.01 JUMPER LOCATIONS ON THE BOARD

Diagram 2-1 shows 19 jumpers labeled from W1 to W18 and J8. These appear as rectangular boxes containing small circles which represent the pins. The jumpers are labeled on the board as well. When there are more than two pins in a jumper, then some of the pins are also numbered on the diagram and on the board, so that it will be possible to locate each pin with its number.

DIAGRAM 2-1: Jumper Locations

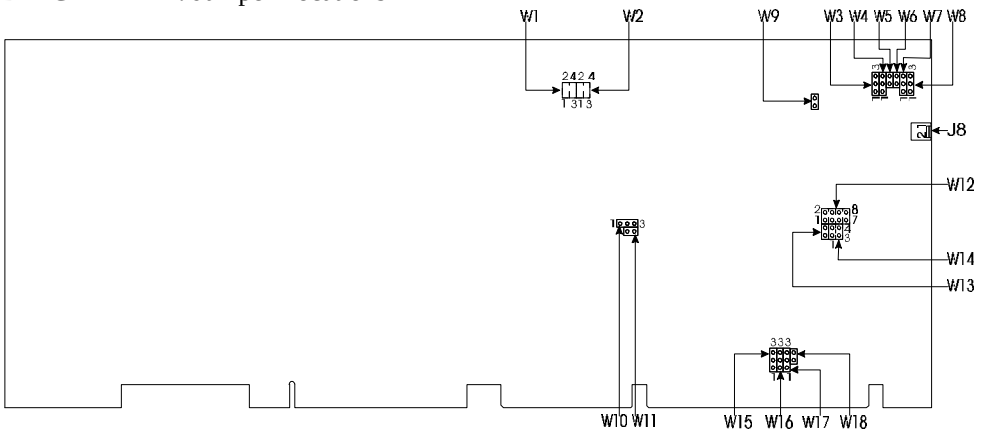


TABLE 2-1a: Jumper Settings: W1-W4, W7-W8

NAME	FUNCTION	CONFIGURATION (INITIAL SETTING: *)
W1 & W2	2.88 MB High Density Floppy, EDOUT signal 2.88 MB High Density Floppy, HDOUT signal	EDOUT left to software*  HDOUT left to software*  OR: 1-3: EDOUT to Pin 29 (J2); 2-4: Ground to Pin 17 (J2)  1-3: HDOUT to Pin 33 (J2); 2-4: Ground to Pin 27 (J2)  OR: 1-2: EDOUT to Pin 17 (J2); 3-4: Ground to Pin 29 (J2)  1-2: HDOUT to Pin 27 (J2); 3-4: Ground to Pin 33 (J2) 
W3 W4 W7 W8	Serial Port 2 Configuration Serial Port 2 Configuration Serial Port 2 Configuration Serial Port 2 Configuration	 RS232 *  RS485/RS422  RS232 *  RS485/RS422  RS232 *  RS485/RS422  RS232 *  RS485/RS422

TABLE 2-1b: Jumper Settings: W5-W6, W9-W12

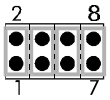
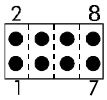
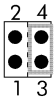
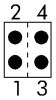
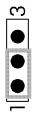
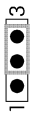
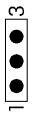
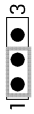
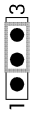
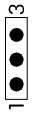
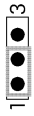
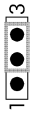
NAME	FUNCTION	CONFIGURATION (INITIAL SETTING: *)
W5	RTS2-CTS2 Serial Port 2 RS485/RS422 Loopback	 Loopback  Normal *
W6	DSR2-DTR2 Serial Port 2 RS485/RS422 Loopback	 Loopback  Normal *
W9	VBAT Internal Battery	 Enabled  Disabled *
W10	Pixel Clock Polarity	Positive * Negative
W11	PS/2 Mouse Interrupt (IRQ12)	 Enabled  Disabled *
W12	Extended BIOS Modes (These jumpers are configured separately, even though they are grouped together here)	1-2: Serial Download Mode 3-4: VT100 Mode 5-6: Disable TEKNOR Extension * 7-8: Disable Onboard VGA Controller  1-2: Normal Mode * 3-4: Standard Mode * 5-6: Enable TEKNOR Extension 7-8: Enable Onboard VGA Controller * 

TABLE 2-1c: Jumper Settings: W13-W18, J8

NAME	FUNCTION	CONFIGURATION (INITIAL SETTING: *)
W13	Power fail monitoring (Non Maskable Interrupt on Power Fail Output)	 Enabled  Disabled *
W14	Supervisor I/O: Base address	 190H *  390H  290H  390H
W15	Interrupt Signal from onboard Parallel Port	 IRQ5 (Normally used for LPT2)  IRQ7 (Normally used for LPT1) *  NONE: IRQ5 & IRQ7 are free
W16 & W17	DMA Request Signal for ECP Mode / DMA Acknowledge Signal for ECP Mode	 DRQ1 OR:  DRQ3 OR:  NONE *  DACK1  DACK3  NONE *
W18	IOCHRDY signal to IDE interface	 Enabled  Disabled *
J8	BIOS boot selection	 Emergency boot (from EPROM BIOS)  Normal boot (from Flash EPROM BIOS) *

3 INSTALLING TEK932 IN PASSIVE BACKPLANE

The TEK932 Pentium™ PCI-ISA Single Board Computer will work on any PCI-ISA passive backplane, provided it complies with the PCI INDUSTRIAL COMPUTER MANUFACTURERS GROUP, Revision 2.0 specification. Therefore, the board may be installed on the TEK950 PCI-ISA Passive Backplane, which has three PCI slots, three or five ISA slots, and a PCI-ISA connector where you can insert the TEK932 (for more information, see the TEK950 TECHNICAL REFERENCE MANUAL).

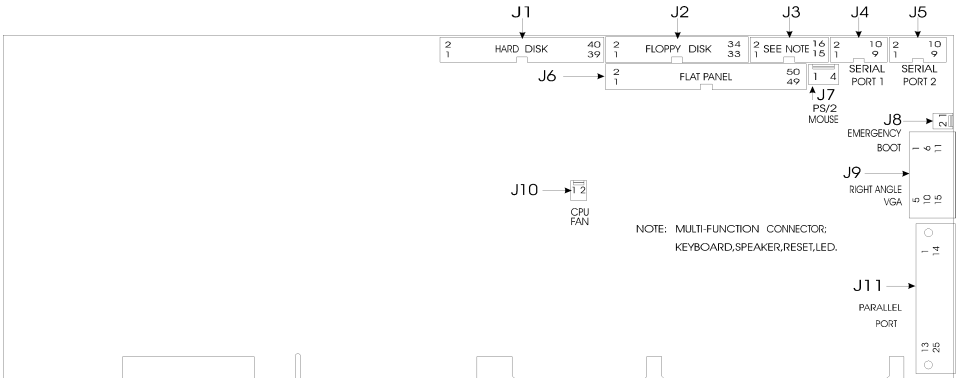
Since the TEK932 is also fully IBM AT compatible, it can also be installed on any standard ISA passive backplane, if PCI expansion slots are not needed.

4 CONNECTOR LOCATIONS & PIN-OUTS

4.01 LOCATION OF CONNECTORS ON THE BOARD

The connectors are labeled J1 to J11. They appear on the diagram below.

DIAGRAM 4-1: Connector Locations



4.02 CONNECTOR PIN-OUTS

Consult the tables on the following pages for the J1-J11 connector pin-outs. This information will help you wire all devices and mating connectors to the TEK932 board. For additional information, consult the appropriate section:

Connector	Section which deals with it
J1 - Hard Disk	9 IDE & FLOPPY
J2 - Floppy Disk	9 IDE & FLOPPY
J3 - Multi-Function (Keyboard, Speaker, Reset, Led)	6 SYSTEM
J4 - Serial Port 1	10 SERIAL & PARALLEL PORTS
J5 - Serial Port 2	10 SERIAL & PARALLEL PORTS
J6 - Flat Panel	12 VIDEO
J7 - PS/2 Mouse	6 SYSTEM
J8 - Emergency BIOS Boot Selection	6 SYSTEM
J9 - VGA	12 VIDEO
J10 - Fan	6 SYSTEM
J11 - Parallel Port	10 SERIAL & PARALLEL PORTS

TABLE 4-1: Hard Disk Connector (J1) - Pin-Out

Pin Number	Signal Flow	Signal	Pin Number	Signal Flow	Signal
1	I	RESET*	2	-	GND
3	I/O	SD7	4	I/O	SD8
5	I/O	SD6	6	I/O	SD9
7	I/O	SD5	8	I/O	SD10
9	I/O	SD4	10	I/O	SD11
11	I/O	SD3	12	I/O	SD12
13	I/O	SD2	14	I/O	SD13
15	I/O	SD1	16	I/O	SD14
17	I/O	SD0	18	I/O	SD15
19	-	GND	20	-	Not Used
21	-	Not Used	22	-	GND
23	I	IOW*	24	-	GND
25	I	IOR*	26	-	GND
27	O	IOCHRDY	28	I	BALE
29	-	Not Used	30	-	GND
31	O	IRQ14	32	O	IOCS16*
33	I	SA1	34	-	Not Used
35	I	SA0	36	I	SA2
37	I	CS0*	38	I	CS1*
39	O	ACTIVE*	40	-	GND

* Active low signal

TABLE 4-2: Floppy Disk Connector (J2) - Pin-Out

Pin Number	Signal Flow	Signal	Pin Number	Signal Flow	Signal
1	-	GND	2	O	RPM/LC
3	-	GND	4	-	Not Used
5	-	GND	6	-	Not Used
7	-	GND	8	I	INDEX*
9	-	GND	10	O	MOTOR ON 0,1*
11	-	GND	12	O	DRIVE SELECT B*
13	-	GND	14	O	DRIVE SELECT A*
15	-	GND	16	O	MOTOR ON 2*
17	-	N. C. [1]	18	O	DIR CONTROL
19	-	GND	20	O	STEP*
21	-	GND	22	O	WRITE DATA*
23	-	GND	24	O	WRITE ENABLE*
25	-	GND	26	I	TRACK0*
27	-	N. C. [1]	28	I	WRITE PROTECT*
29	-	N. C. [1]	30	I	READ DATA*
31	-	GND	32	O	HEAD SELECT*
33	-	N. C. [1]	34	I	DSKCHG*

* Active low signal

[1] By default, these pins are not connected, however, by installing the W1 and W2 jumpers, these configurations are possible (see also page 9-10 in the manual):

1)		Or: 2)	
17	GND	17	EDOUT (2.88 MB)
27	GND	27	HDOUT (2.88 MB)
29	EDOUT (2.88 MB)	29	GND
33	HDOUT (2.88 MB)	33	GND

TABLE 4-3: Multi-Function Connector - Keyboard, Speaker, Reset, LED - (J3) - Pin-Out

Pin Number				Pin Number		
Signal Flow					Signal Flow	
Signal						Signal
KBDCLK	I/O	1		2	-	GND
KBDDATA	I/O	3		4	-	GND
VCC	-	5		6	-	VCC
SPKR	O	7		8	-	VCC
KBDINH	I	9		10	-	GND
DOWNLD*	I	11		12	-	GND
PBRES*	I	13		14	-	GND
ACT*	O	15		16	-	VCC

* Active low signal

TABLE 4-4: Serial Port 1 - COM1 (J4) RS232 - Pin-Out

Pin Number				Pin Number		
Signal Flow					Signal Flow	
Signal						Signal
DCD	I	1		2	I	DSR
RX	I	3		4	O	RTS
TX	O	5		6	I	CTS
DTR	O	7		8	I	RI
GND	-	9				

TABLE 4-5: Serial Port 2 - COM2 (J5) RS232 - Pin-Out

Pin Number	Signal Flow			Pin Number	Signal Flow	
Signal						Signal
DCD	I	1		2	I	DSR
RX	I	3		4	O	RTS
TX	O	5		6	I	CTS
DTR	O	7		8	I	RI
GND	-	9				

TABLE 4-6: Serial Port 2 - COM2 (J5) RS485/RS422 - Pin-Out

Pin Number	Signal Flow			Pin Number	Signal Flow	
Signal						Signal
DCD	I	1		2	I	DSR
RXD(-)	I/O	3		4	I/O	RXD(+)
TXD(-)	O	5		6	I	TXD(+)
DTR	O	7		8	I	RI
GND	-	9				

TABLE 4-7: Flat Panel Connector (J6) - Pin-Out

Pin Number	Signal	Pin Number	Signal
1	ENAVDD	2	VCC (+5V)
3	ENAVEE	4	STNDBYE*
5	ENABLK	6	GND
7	M/DE	8	ACTI
9	GND	10	LP/DE
11	FLM	12	GND
13	SHFCLK	14	GND
15	P0	16	P1
17	GND	18	P2
19	P3	20	GND
21	P4	22	P5
23	GND	24	P6
25	P7	26	GND
27	P8	28	P9
29	GND	30	P10
31	P11	32	GND
33	P12	34	P19
35	GND	36	P14
37	P17	38	P18
39	P18	40	P17
41	GND	42	P18
43	P19	44	GND
45	P20	46	P21
47	GND	48	P22
49	P23	50	GND

* Active low signal

TABLE 4-8: PS/2 Mouse Connector (J7) - Pin-Out

Pin Number	Signal
1	MCLK
2	GND
3	MDATA
4	VCC

TABLE 4:9: Emergency BIOS Boot (J8) - Pin- Out

Pin Number	Signal
1	EMER*
2	GND

* Active low signal

TABLE 4-10: VGA Connector (J9) - Pin-Out

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
1	RED	6	GND	11	Not Used
2	GREEN	7	GND	12	Not Used
3	BLUE	8	GND	13	HSYNC
4	Not Used	9	Not Used	14	VSYNC
5	GND	10	GND	15	Not Used

TABLE 4-11: Fan Connector (J10) - Pin-Out

Pin Number	Signal
1	+12V
2	GND

TABLE 4-12: Parallel Port Connector (J11) - Standard Mode - Pin-Out

Pin Number				Pin Number		
Signal Flow					Signal Flow	
Signal						Signal
STROBE*	O	1		14	O	AUTOFD*
D0	I/O	2		15	I	ERROR*
D1	I/O	3		16	O	INIT*
D2	I/O	4		17	O	SELECTIN*
D3	I/O	5		18	-	GND
D4	I/O	6		19	-	GND
D5	I/O	7		20	-	GND
D6	I/O	8		21	-	GND
D7	I/O	9		22	-	GND
ACK*	I	10		23	-	GND
BUSY	I	11		24	-	GND
PE	I	12		25	-	GND
SELECT	I	13				

* Active low signal

TABLE 4-13: Parallel Port Connector (J11) - EPP Mode - Pin-Out

Pin Number				Pin Number		
Signal Flow					Signal Flow	
Signal						Signal
WRITE*	O	1		14	O	DATASTB*
D0	I/O	2		15	-	Not Used
D1	I/O	3		16	-	Not Used
D2	I/O	4		17	O	ADDRSTRB*
D3	I/O	5		18	-	GND
D4	I/O	6		19	-	GND
D5	I/O	7		20	-	GND
D6	I/O	8		21	-	GND
D7	I/O	9		22	-	GND
INTR	I	10		23	-	GND
WAIT*	I	11		24	-	GND
Not Used	-	12		25	-	GND
Not Used	-	13				

* Active low signal

TABLE 4-14: Parallel Port Connector (J11) - ECP Mode - Pin-Out

Pin Number				Pin Number		
Signal Flow					Signal Flow	
Signal						Signal
STROBE*	O	1		14	O	AUTOFD*, HOSTACK[3]
D0	I/O	2		15	I	FAULT*[1], PERIPHRQST*[3]
D1	I/O	3		16	O	INIT*[1], REVERSERQST*[3]
D2	I/O	4		17	O	SELECTIN*[1,3]
D3	I/O	5		18	-	GND
		6		19	-	GND
		7		20	-	GND
	I	8		21	-	GND
	O	9		22	-	GND
ACK*	I	10		23	-	GND
BUSY, PERIPHACK[3]	I	11		24	-	GND
PERROR, ACKREVERSE[3]	I	12		25	-	GND
SELECT	I	13				

* Active low signal
[1] Compatible Mode
[3] High Speed Mode

6 SYSTEM

This section deals with various components of the system board.

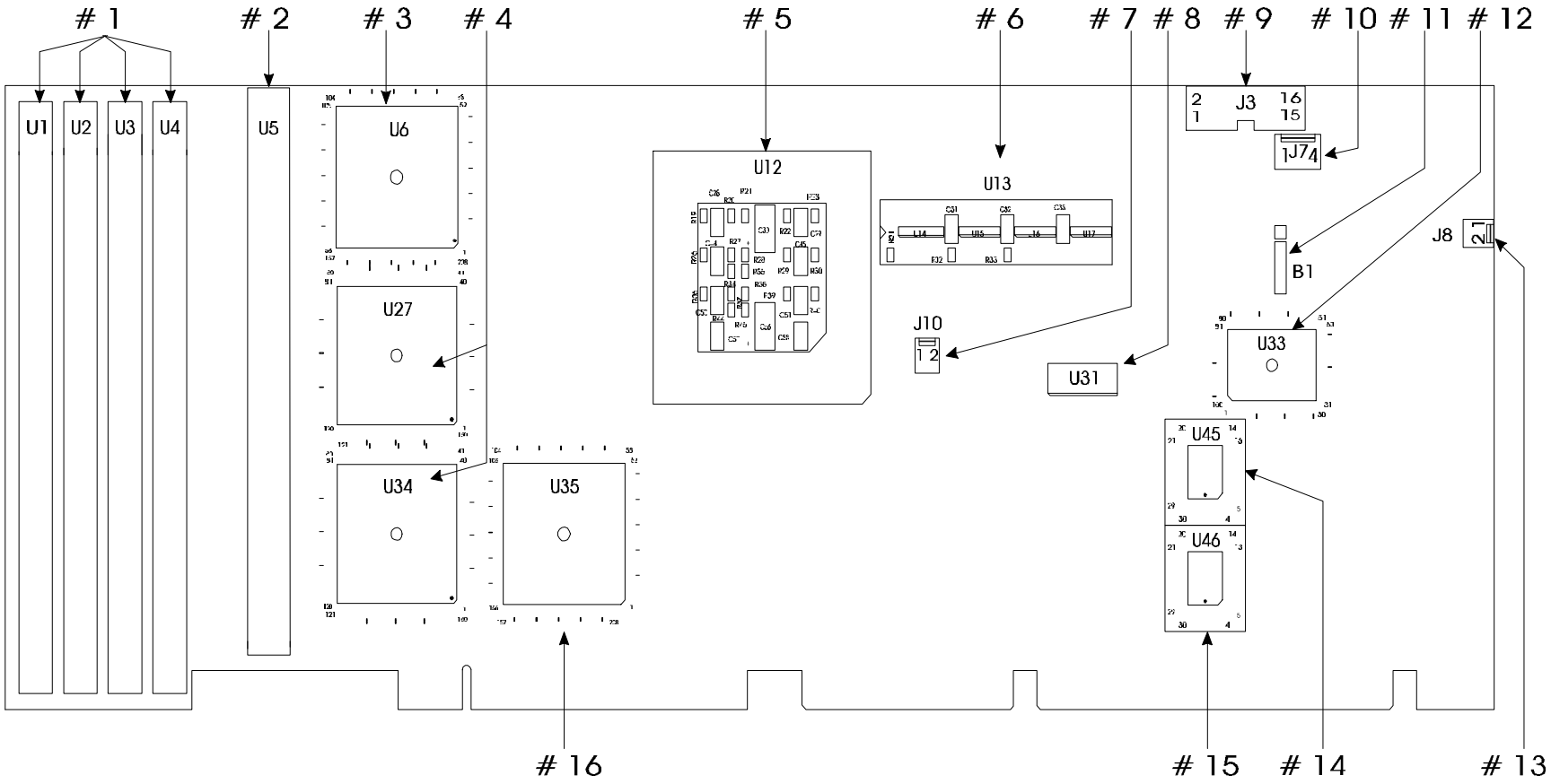
6.01 LOCATION OF SYSTEM COMPONENTS

Diagram 6-1 shows the location of the system components described in sections 6.02 to 6.13.

System components are numbered in Diagram 6-1. The following list shows which components these numbers correspond to, as well as the sub-section in which they are explained:

#	COMPONENT	SECTION
1	System Memory (DRAM)	6.06 - SYSTEM MEMORY (DRAM)
2	System Cache	6.05 - CACHE
3	PCI, Cache & Memory Controller (PCMC)	6.04 - SYSTEM CONTROLLER
4	(Two) Local Bus Accelerator (LBX)	6.04 - SYSTEM CONTROLLER
5	Microprocessor	6.02 - MICROPROCESSOR
6	AT Keyboard & PS/2 Mouse Controller	6.10 - AT KEYBOARD & PS/2 MOUSE CONTROLLER
7	Fan Connector	6.03 - FAN CONNECTOR
8	Real Time Clock	6.08 - BATTERY
9	Multi-Function Connector (Keyboard, Speaker, Reset, LED)	6.11 - MULTI-FUNCTION CONNECTOR (KEYBOARD, SPEAKER, RESET, LED)
10	PS/2 Mouse Connector	6.12 - PS/2 MOUSE CONNECTOR
11	VBAT Internal Battery	6.08 - BATTERY
12	Field Programmable Gate Array (FPGA)	6.09 - SUPERVISOR UTILITIES
13	Emergency BIOS Boot Selection	6.07 - BIOS (FLASH EPROM & EPROM)
14	Flash EPROM BIOS	6.07 - BIOS (FLASH EPROM & EPROM)
15	EPROM BIOS	6.07 - BIOS (FLASH EPROM & EPROM)
16	ISA Bridge (System I/O)	6.04 - SYSTEM CONTROLLER

DIAGRAM 6-1: System Components Location



As seen on page 6-2, each component shown in the diagram is explained in a section. These sections are grouped and ordered as follows:

• CPU Related:	6.02 - MICROPROCESSOR
	6.03 - FAN CONNECTOR
• Chipset Related:	6.04 - SYSTEM CONTROLLER
	6.05 - CACHE
	6.06 - SYSTEM MEMORY (DRAM)
• BIOS Related	6.07 - BIOS (FLASH EPROM & EPROM)
• Real Time Clock Related	6.08 - BATTERY
• Field Programmable Gate Array	6.09 - SUPERVISOR UTILITIES
• Keyboard & Mouse Related	6.10 - AT KEYBOARD & PS/2 MOUSE CONTROLLER
	6.11 - MULTI-FUNCTION CONNECTOR (KEYBOARD, SPEAKER, RESET, LED)
	6.12 - PS/2 MOUSE CONNECTOR

6.02 - MICROPROCESSOR

The TEK932 board has an interchangeable microprocessor design; the following **supported microprocessors** are available (maximum internal CPU clock speed indicated):

- Pentium™ iCOMP™ Index 610 running at 75 MHz,
- Pentium™ iCOMP™ Index 815 running at 100 MHz.

The **Pentium** processor family contains all of the features of the Intel486 CPU family, with the addition of the following **features**:

- Superscalar architecture,
- Dynamic Branch Prediction,
- Pipelined floating-point unit,
- Improved instruction execution time,
- Separate 8KB Code and 8KB Data Caches,
- Write-back MESI protocol in the Data Cache,
- 64-bit data bus,
- Bus cycle pipelining,
- Address parity,
- Internal parity checking,
- Functional redundancy checking,
- Execution tracing,
- Performance monitoring,
- IEEE 1149.1 boundary scan,
- System Management Mode,
- Virtual mode extensions.

In addition to the above features of the Pentium processor family, the **iCOMP™ Index 610**, **iCOMP™ Index 735** and the **iCOMP™ Index 815** offer these **enhancements**:

- iCOMP performance rating of 610 at 75 MHz in single processor configuration,
- iCOMP performance rating of 815 at 100 MHz in single processor configuration,
- Dual processing support,
- SL power management features,
- Upgradable with a future Pentium overdrive processor,
- Fractional bus operation,
- On-chip local APIC device.

6.03 - FAN CONNECTOR

The # 7 component on Diagram 6-1 is for connecting a CPU fan. Its pin-out is as follow:

TABLE 6-1: Fan Connector (J10) - Pin-Out

Pin Number	Signal
1	+12V
2	GND

6.04 - SYSTEM CONTROLLER

The TEK932 board uses Intel's 82430NX PCIset, which consists of the following components:

- The 82434NX PCI, Cache and Memory Controller (PCMC) located at U6 (#3) on Diagram 6-1,
- The two 82433NX Local Bus Accelerator (LBX) located at U27 and U34 (#4), and
- The 82378ZB System I/O (SIO), referred in this manual as the ISA Bridge, located at U35 (#16).

Each of the above components are described below.

The **PCI, Cache and Memory Controller (PCMC)** integrates a Cache controller, a DRAM controller, and a Bus controller for transfers between the CPU, Cache, System Memory and the PCI Local Bus. The PCMC has the following features:

- Support for the Pentium ™ processor at 60 Mhz and 66 Mhz,
- Supports the Pentium processor's pipelined addressing capability,
- Drives 3.3 V signal levels on the CPU and Cache interfaces,
- High performance CPU/PCI/Memory interfaces via posted write and read prefetch buffers,
- Fully synchronous PCI interface with full bus master capability:
  - Supports PCI Configuration Access Mechanisms #1 and #2,
- Supports write-back Cache policy,
- Programmable attribute map of DOS and BIOS regions,
- Integrated low skew clock driver for distributing Host clock,
- Integrated second level Cache controller:
  - Supports standard SRAMs
  - 256 KB and 512 KB sizes
- - Cache hit cycle of 3-2-2-2 on reads and writes using standard SRAMs,

- Integrated DRAM controller:
  - Supports CPU and PCI master aceesses to System Memory,
  - Supports 2 MB to 128 MB of Cacheable System Memory (DRAM),
- Host/PCI Bridge:
  - Translates CPU cycles into PCI bus cycles
  - Burst mode writes to PCI in zero PCI wait-states (i.e., data transfer every cycle).

The two **Local Bus Accelerator (LBX)** provide a 64-bit data path between the Host CPU/Cache and System Memory, a 32-bit data path between the Host CPU bus and PCI Local Bus, and a 32-bit path between the PCI Local Bus and System Memory. The LBX has the following features:

- Support for the Pentium processor's 64-bit data bus at frequencies up to 66 Mhz,
- Drives 3.3 V signal levels on the CPU data and address buses,
- Provides a 64-bit interface to DRAM and a 32-bit interface to PCI,
- Incorporates three write posting buffers and two read prefetch buffers to increase CPU and PCI performance,
- CPU-to-Memory and CPU-to-PCI write posting buffers accelerate write performance,
- Dual-port architecture allows concurrent operations on the Host and PCI buses,
- Operates synchronously to the CPU and PCI clocks,
- Supports Memory burst read and writes from the Host and PCI buses,
- Sequential CPU writes to PCI converted to zero wait-state PCI bursts with optional TRDY# connection
- Byte parity support for the Host and Memory buses.

The **ISA Bridge (System I/O)** provides the bridge between the PCI bus and the ISA expansion bus. It integrates many of the common I/O functions found in today's ISA based PC systems. The ISA bridge has the following features:

- 100% PCI and ISA compatible,
- Enhanced seven channel DMA controller (see Table 6-2): Supports fast DMA transfers,
- Integrated data buffers to improve performance,
- Integrated 16-bit BIOS timer,
- Non-Maskable Interrupts (NMI),
- Arbitration for ISA devices,
- Four dedicated PCI interrupts,
- Arbitration for PCI devices,
- Integrates the functionality of one 82C54 Timer,
- Integrates the functionality of two 82C59 interrupt controllers (see Table 6-3),
- Complete support for enhanced Intel486 CPU (SMI).

TABLE 6-2: DMA Controller Channels

DMA 0	Available
DMA 1	Available (ECP)
DMA 2	Floppy controller
DMA 3	Available (ECP)
DMA 4	Cascade controller # 1
DMA 5	Available
DMA 6	Available
DMA 7	Available

The parallel port's ECP mode can be configured to use Channel 1 or 3. Channel 2 is reserved for the floppy controller and Channel 4 is used to cascade Channels 0 through 7 to the microprocessor.

TABLE 6-3: 8259 Interrupt Controllers Lines

Controller # 1		Controller # 2	
IRQ 0	Timer 0	IRQ 8	Real-time clock
IRQ 1	Keyboard	IRQ 9	Available (ISA/PCI)
IRQ 2	Cascade controller # 2	IRQ 10	Available (ISA/PCI)
IRQ 3	COM 2 *	IRQ 11	Available (ISA/PCI)
IRQ 4	COM 1 *	IRQ 12	Available (PS/2 Mouse)
IRQ 5	Available(LPT2) *	IRQ 13	Coprocessor Error
IRQ 6	Floppy controller *	IRQ 14	IDE *
IRQ 7	LPT 1 *	IRQ 15	Available (ISA/PCI)

* All functions marked with an asterisk (*) can be disabled or reconfigured.

Two 8259 interrupt controllers handle the interrupts on theTEK932. Six interrupt lines are directly linked to the keyboard controller, timer, the real-time clock, both serial ports and the parallel port.

6.05 - CACHE

There are two separate Caches in the Host subsystem: Internal Cache and External Cache. The Cache inside the Pentium processor (Internal Cache) is referred to as the first level Cache (also primary Cache). The External Cache (called System Cache in this manual) comprises the System Controller's Cache control circuitry and associated external memory array; it is referred to as the second level Cache (also secondary Cache). The second level Cache is unified, which means that both CPU data and instructions are stored in the Cache.

6.05.1 SYSTEM CACHE

The System Controller integrates a high performance write-back second level Cache controller, tag RAM and a full first and second level Cache coherency mechanism. The System Controller supports a direct-mapped secondary Cache.

The upgradeable Cache socket is located at U5 (#2) on Diagram 6-1; it accepts either 256 KB or 512 KB of standard asynchronous SRAMs.

System Cache copies the most recently accessed data and places it in an area of high speed memory called SRAM (Static RAM). Cache SRAM is positioned between System Memory (DRAM) and the CPU. Data is transferred from System Memory to Cache and then from Cache to the CPU.

Since most program executions are sequential and repetitive, the likelihood is great that the CPU will find data already stored in either Cache. When the CPU retrieves data from Cache, a **Cache hit** occurs. On the other hand, when the CPU must access data from System Memory, a **Cache miss** occurs.

System Cache is enabled and configured in the AMIBIOS Setup program (see Section 14).

6.06 - SYSTEM MEMORY (DRAM)

A local DRAM controller is integrated in the System Controller. Dynamic Random Access Memory (DRAM) is essential system memory. The memory array is 64-bits wide and ranges in size from 2 MB to 128 MB. The array is implemented using single-sided or double-sided SIMMs (Single In-line Memory Modules). See section 1 for instructions on configuring and installing SIMMs.

The location of the four 72-pin vertical SIMM sockets appears on Diagram 6-1 at U1, U2, U3 and U4 (#).

The DRAM Controller supports CPU and PCI master accesses to System Memory. The PCI, Cache and Memory Controller's DRAM interface supplies the control signals and address lines; the Local Bus Accelerator supplies the data path. DRAM parity is generated for System memory writes and checked for memory reads.

6.07 - BIOS (FLASH EPROM & EPROM)

The Flash EPROM BIOS and the EPROM BIOS are factory installed. The Flash EPROM BIOS appears on Diagram 6-1 at U45 (#14) and the EPROM BIOS at U46 (#15).

By default the TEK932 boots from the Flash EPROM BIOS. This is set by the J8 Emergency BIOS boot selection jumper (# 13 PM Diagram 6-1), as follows:

- J8: Selects the BIOS to boot from:
  - Shorted: Emergency boot (from EPROM BIOS),
  - Or open: Normal boot (from Flash EPROM BIOS): This is the initial setting.

The pin-out for J8 appears below:

TABLE 6-4: Emergency BIOS Boot (J8) - Pin-Out

Pin Number	**Signal**
1	EMER*
2	GND

* Active low signal

6.08 - BATTERY

The TEK932 comes with a 360 mAh TL5186 TADIRAN battery, which is located at B1 (#11 on Diagram 6-1). It powers the Real Time Clock (located at U31, #8) and the CMOS Setup, whenever the board is powered down.

The TL5186 TADIRAN battery has a shelf life of approximately 10 years (under "no-load" conditions). The actual life of the battery depends on environmental (temperature) conditions. The TADIRAN TL5186 has an operating range of -55° to 75°C and discharge characteristics vary with temperature.

The voltage supplied by the battery is 3.6 volts. This can be verified with a standard voltmeter at the battery socket's two extreme pins (if you use the pin on the soldered side, you do not have to remove the battery).

Jumper W9 enables the Internal Battery's power. Removing the W9 jumper has the same effect as putting the battery in storage; TEKNOR always ships its board with battery jumper removed in order to increase the life of the battery. Please refer to Section 2 for jumper location and setting.

The TADIRAN TL5186 is UL recognized. Its UL component recognition is MH12193.

The TEK932 board has a special feature that allows the CMOS RAM Setup to be saved in Flash EPROM memory. This feature eliminates battery dependance by saving and recovering the CMOS RAM Setup from Flash (only the time and date could be lost).

☞ **In order to save your current CMOS RAM Setup in Flash, you must update the VIP-UP Setup (with F10), while the "Use Flash To Store CMOS RAM SETUP" (first screen) is set to "Yes". See section 15.02 for more information.**

6.09 - SUPERVISOR UTILITIES

Component # 11 on Diagram 6-1 is defined on page 6-2 as Field Programmable Gate Array (FPGA); this memory device contains registers, one of which is described below.

TEKNOR computers utilize address space 190H, 290H or 390H (depending on the setting of W14 jumper for I/O base address) to enable special features (see Table 6-3 below).

TABLE 6-5: Register 190H, 290H or 390H

Bit #	**Bit Value (Default)**	**Function:** WRITE	READ
0	0	Enable Watchdog 1=enable, R/W bit	Same
1	1	Watchdog activate 1-0-1 to toggle, R/W bit	Same
2	0	Flash VPP enable	Same
3	0	Enable direction control RS-485 1=enable RS-485 only, write only	Power Detection Output or Battery Low output
4	0	Reserved, ENWF	W12(7-8) Status
5	0	Reserved, ENWB	W12(5-6) Status
6	1	Reserved, B64/16	W12(3-4) Status
7	0	Reserved	W12(1-2) Status

☞ **Not all bits are R/W. Therefore, be certain to keep a mirror image of the register when programming it.**

☞ **All bits are 0 after a hardware RESET or power up condition.**

☞ **Write the values shown in the "Bit Value (Default)" column if you are unsure.**

6.10 - AT KEYBOARD & PS/2 MOUSE CONTROLLER

The AT Keyboard and PS/2 Mouse Controller is located at U13 (or # 6 on Diagram 6-1). Its features are as follows:

- Complete chipset independance.
- Complete operating system independence.
- Works with DOS, Microsoft Windows®, OS/2®, and Unix.
- High-level functional integration.

6.11 - MULTI-FUNCTION CONNECTOR (KEYBOARD, SPEAKER, RESET, LED)

Connector J3 (# 9 on Diagram 6-1) provides all the necessary signals for connecting the keyboard, speaker, reset, and keylock interface devices. The following diagram shows the pin-out at J3:

TABLE 6-6: Multi-Function Connector - Keyboard, Speaker, Reset, LED - (J3) - Pin-Out

Pin Number	Signal Flow			Pin Number	Signal Flow	
Signal						Signal
KBCLK	I/O	1	2	-	GND
KBDDATA	I/O	3	4	-	GND
VCC	-	5	6	-	VCC
SPKR	O	7	8	-	VCC
KBDINH	I	9	10	-	GND
DOWNLD*	I	11	12	-	GND
PBRES*	I	13	14	-	GND
ACT*	O	15	16	-	VCC

* Active low signal

The following functions are available on the J3 Connector:

- Speaker: An 8 ohm speaker can be directly connected to pins 7 and 8 of J3. All necessary drivers are on the board.
- Keyboard Disable: The keyboard can be disabled or locked up by shorting pins 9 and 10 of J3.
- Hard Disk LED: The onboard IDE interface activates an external LED. The LED must be connected anode on pin 16 (J3) and cathode on pin 15 (J3). No external current limiting resistor is required since one is already present on the board.
- Reset: Hand reset the system by driving PBRES* to low state (< 0.8 V).

6.12 - PS/2 MOUSE CONNECTOR

The board supports a mouse, through the PS/2 connector at J7 (# 10 on Diagram 6-1). With the PS/2 Mouse Cable (available from TEKNOR), this feature is compatible with the standard IBM PS/2 mouse. The cable may be ordered by contacting our Sales department.

During installation of the mouse, you must install the driver provided by the mouse manufacturer.

TABLE 6-7: PS/2 Mouse Connector (J7) - Pin-Out

Pin Number	Signal
1	MCLK
2	GND
3	MDATA
4	VCC

The PS/2 mouse is Enabled by default in AMIBIOS through the Advanced Setup Mouse Support option (see section 14.04.2 for more information).

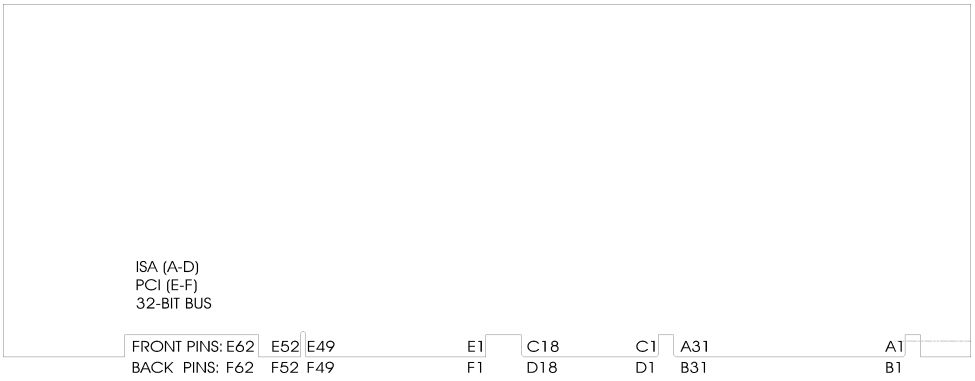
To enable the PS/2 mouse interrupt (IRQ12), which generates an interrupt each time the mouse is moved, short jumper W11 (see section 2 for jumper location and setting).

7 PCI-ISA BUS

7.01 LOCATION OF PCI-ISA BUS CONNECTOR

The PCI-ISA bus connector appears on the diagram below.

DIAGRAM 7-1: PCI-ISA Bus Connector Location



7.02 PCI-ISA CONNECTOR PIN-OUTS

TABLE 7-1a: ISA Bus Connector (A, B)

A SIDE

I/O PIN	Signal Name	I/O
A1	IOCHK*	I
A2	SD7	I/O
A3	SD6	I/O
A4	SD5	I/O
A5	SD4	I/O
A6	SD3	I/O
A7	SD2	I/O
A8	SD1	I/O
A9	SD0	I/O
A10	IOCHRDY	I
A11	AEN	O
A12	SA19	I/O
A13	SA18	I/O
A14	SA17	I/O
A15	SA16	I/O
A16	SA15	I/O
A17	SA14	I/O
A18	SA13	I/O
A19	SA12	I/O
A20	SA11	I/O
A21	SA10	I/O
A22	SA9	I/O
A23	SA8	I/O
A24	SA7	I/O
A25	SA6	I/O
A26	SA5	I/O
A27	SA4	I/O
A28	SA3	I/O
A29	SA2	I/O
A30	SA1	I/O
A31	SA0	I/O

B SIDE

I/O PIN	Signal Name	I/O
B1	GND	-
B2	RESET DRV	O
B3	VCC	-
B4	IRQ9	I
B5	Not Used	-
B6	DRQ2	I
B7	-12 Vdc	-
B8	OWS*	I
B9	+12 Vdc	-
B10	GND	-
B11	SMEMW*	O
B12	SMEMR*	O
B13	IOW*	I/O
B14	IOR*	I/O
B15	DACK3*	O
B16	DRQ3	I
B17	DACK1*	O
B18	DRQ1	I
B19	REFRESH*	I/O
B20	SYSCLK	O
B21	IRQ7	I
B22	IRQ6	I
B23	IRQ5	I
B24	IRQ4	I
B25	IRQ3	I
B26	DACK2*	O
B27	T/C	O
B28	BALE	O
B29	VCC	-
B30	OSC	O
B31	GND	-

* Active low signal

TABLE 7-1b: ISA Bus Connector (C, D)

C Side

I/O PIN	Signal Name	I/O
C1	SBHE*	I/O
C2	LA23	I/O
C3	LA22	I/O
C4	LA21	I/O
C5	LA20	I/O
C6	LA19	I/O
C7	LA18	I/O
C8	LA17	I/O
C9	MEMR*	I/O
C10	MEMW*	I/O
C11	SD08	I/0
C12	SD09	I/O
C13	SD10	I/O
C14	SD11	I/O
C15	SD12	I/O
C16	SD13	I/O
C17	SD14	I/O
C18	SD15	I/O

D Side

I/O PIN	Signal Name	I/O
D1	MEMCS16*	I
D2	IOCS16*	I
D3	IRQ10	I
D4	IRQ11	I
D5	IRQ12	I
D6	IRQ15	I
D7	IRQ14	I
D8	DACK0*	O
D9	DRQ0	I
D10	DACK5*	O
D11	DRQ5	I
D12	DACK6*	O
D13	DRQ6	I
D14	DACK7*	O
D15	DRQ7	I
D16	VCC	-
D17	MASTER*	I
D18	GND	-

* Active low signal

TABLE 7-2a: PCI Bus Connector (E1-E35, F1-F35)

E SIDE

I/O PIN	Signal Name	I/O
E1	Not Used	-
E2	+12 Vdc	-
E3	Not Used	-
E4	Not Used	-
E5	+5 Vdc	-
E6	INTA*	I
E7	INTC*	I
E8	+5 Vdc	-
E9	CLKC	O
E10	+5 Vdc (I/O)	-
E11	CLKD	O
E12	GND	-
E13	GND	-
E14	GNT1*	O
E15	RESET*	O
E16	+5 Vdc (I/O)	-
E17	GNT0*	O
E18	GND	-
E19	REQ2*	I
E20	AD30	I/O
E21	+3.3 Vdc	-
E22	AD28	I/O
E23	AD26	I/O
E24	GND	-
E25	AD24	I/O
E26	GNT2*	O
E27	+3.3 Vdc	-
E28	AD22	I/O
E29	AD20	I/O
E30	GND	-
E31	AD18	I/O
E32	AD16	I/O
E33	+3.3 Vdc	-
E34	FRAME*	O
E35	GND	-

F SIDE

I/O PIN	Signal Name	I/O
F1	-12 Vdc	-
F2	Not Used	-
F3	GND	-
F4	Not Used	-
F5	+5 Vdc	-
F6	+5 Vdc	-
F7	INTB*	I
F8	INTD*	I
F9	REQ3*	I
F10	REQ1*	I
F11	GNT3*	O
F12	GND	-
F13	GND	-
F14	CLKA	O
F15	GND	-
F16	CLKB	O
F17	GND	-
F18	REQ0*	I
F19	+5 Vdc (I/O)	-
F20	AD31	I/O
F21	AD29	I/O
F22	GND	-
F23	AD27	I/O
F24	AD25	I/O
F25	+3.3 Vdc	-
F26	C/BE3*	I/O
F27	AD23	I/O
F28	GND	-
F29	AD21	I/O
F30	AD19	I/O
F31	+3.3 Vdc	-
F32	AD17	I/O
F33	C/BE2*	I/O
F34	GND	-
F35	IRDY*	O

* Active low signal

TABLE 7-2b: PCI Bus Connector (E36-E62, F36-F62)

E Side

I/O PIN	Signal Name	I/O
E36	TRDY*	I
E37	GND	-
E38	STOP*	I
E39	+3.3 Vdc	-
E40	Not Used	-
E41	Not Used	-
E42	GND	-
E43	PAR	I/O
E44	AD15	I/O
E45	+3.3 Vdc	-
E46	AD13	I/O
E47	AD11	I/O
E48	GND	-
E49	AD9	I/O
	CONNECTOR KEY	
	CONNECTOR KEY	
E52	C/BE0*	I/O
E53	+3.3 Vdc	-
E54	AD6	I/O
E55	AD4	I/O
E56	GND	-
E57	AD2	I/O
E58	AD0	I/O
E59	+5 Vdc (I/O)	-
E60	Not Used	-
E61	+5 Vdc	-
E62	+5 Vdc	-

F Side

I/O PIN	Signal Name	I/O
F36	+3.3 Vdc	-
F37	DEVSEL*	I
F38	GND	-
F39	LOCK*	O
F40	PERR*	I/O
F41	+3.3 Vdc	-
F42	SERR*	I/O
F43	+3.3 Vdc	-
F44	C/BE1*	I/O
F45	AD14	I/O
F46	GND	-
F47	AD12	I/O
F48	AD10	I/O
F49	GND	-
	CONNECTOR	
	KEY	
F52	CONNECTOR	I/O
F53	KEY	I/O
F54	AD8	-
F55	AD7	I/O
F56	+3.3 Vdc	I/O
F57	AD5	-
F58	AD3	I/O
F59	GND	-
F60	AD1	-
F61	+5 Vdc (I/O)	-
F62	Not Used	-
	+5 Vdc	
	+5 Vdc	

* Active low signal

7.03 PCI-ISA CONNECTOR DESCRIPTION

The PCI-ISA connector on the TEK932 conforms to the PCI INDUSTRIAL COMPUTER MANUFACTURERS GROUP (PICMG), Revision 2 specification. The general architecture generally follows the PCI Local Bus and the ISA Bus.

The TEK932 PCI-ISA board is designed to interface with both ISA and PCI peripheral boards mounted on a passive backplane via its ISA-bus connector and PCI-bus connector.

The standard 32-bit PCI-ISA connector contains a total of 218 pins.

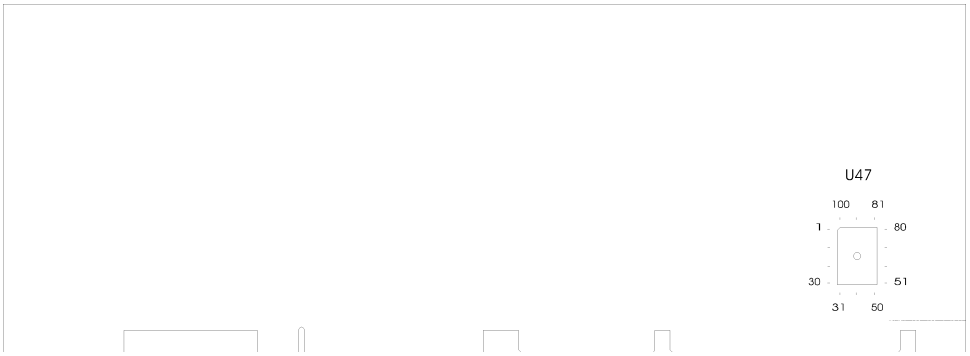
The PCI-ISA connector is defined as an ISA-bus connector followed by a PCI-bus connector. The ISA connector contains all the signals defined for ISA bus interface. The PCI connector contains all the signals defined for PCI bus interface.

8 SYSTEM I/O CONTROLLER

8.01 LOCATION OF SYSTEM I/O CONTROLLER

The System I/O Controller (for Floppy and IDE drives, and Parallel and Serial ports) appears on Diagram 8-1 at U47.

DIAGRAM 8-1: System I/O Controller Location



8.02 SYSTEM I/O CONTROLLER FEATURES

The following features are incorporated in the System I/O Controller:

- Super I/O Floppy Disk Controller:
  - Supports two floppy disk drives, including single, double and high density drives with capacities ranging from 360 KB up to 2.88 MB.
  - Supports vertical recording format.
  - 100% IBM® compatible.
  - Detects all overrun and underrun conditions.
  - 48 mA drivers and Schmitt trigger inputs.
  - DMA enable logic.
  - Data rate and drive control registers.
  - Swap drives A and B.
  - Non-burst mode DMA option.
  - Floppy Disk Controller primary/secondary address selection.
  - 16 byte data FIFO.

- Enhanced Digital Data Separator:
  - Data rates: 1 MB/s, 500 KB/s, 300 KB/s and 250 KB/s.
  - Supports floppy disk drives and tape drives.
  - Programmable precompensation modes.

- Multi-Mode Parallel Port:

  - Standard Mode: IBM PC/XT®, PC/AT®, and PS/2 compatible bidirectional Parallel Port.

  - Enhanced Mode: Enhanced Parallel Port (EPP) compatible.

  - High Speed Mode: Microsoft and Hewlett Packard Extended Capabilities Port (ECP) compatible.

  - Incorporates ChiProtect circuitry for protection against damage due to printer power-on.

  - 24 mA output drivers.

- Serial Ports:

  - Two high speed UARTs with send/receive 16 byte FIFOs.

  - MIDI compatible.

  - Programmable baud rate generator.

  - Modem control circuitry.

- IDE Interface:

  - On-chip decode and select logic compatible with IBM PC/XT and PC/AT embedded hard disk drives.

  - IDE primary/secondary address selection.

- General Purpose 11 Bit Address Decoder.

9 IDE & FLOPPY

9.01 INSTALLING IDE DEVICES

9.01.1 TYPE OF HARD DISK SUPPORTED

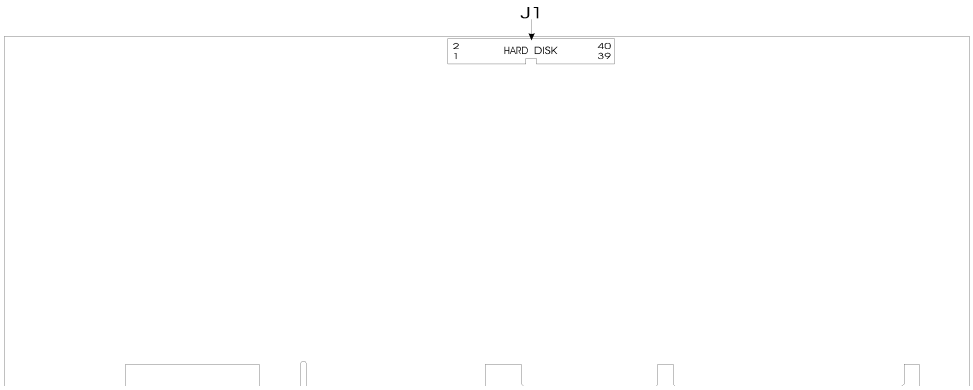
The TEK932 supports AT Integrated Disk Drives. The AT embedded drive architecture incorporates drive electronics and controller circuitry on a single printed circuit board which is mounted directly to the disk drive chassis.

The integration of drive and controller functions increases reliability and performance by eliminating redundant circuitry, thus providing increased performance at reduced cost.

9.01.2 IDE CONNECTOR LOCATION & PIN-OUT

The IDE connector appears on Diagram 9-1 at J1.

DIAGRAM 9-1: IDE Connector Location



The IDE Connector's pin-out appears in Table 9-1.

TABLE 9-1: Hard Disk Connector (J1) - Pin-Out

Pin Number	Signal Flow	Signal	Pin Number	Signal Flow	Signal
1	I	RESET*	2	-	GND
3	I/O	SD7	4	I/O	SD8
5	I/O	SD6	6	I/O	SD9
7	I/O	SD5	8	I/O	SD10
9	I/O	SD4	10	I/O	SD11
11	I/O	SD3	12	I/O	SD12
13	I/O	SD2	14	I/O	SD13
15	I/O	SD1	16	I/O	SD14
17	I/O	SD0	18	I/O	SD15
19	-	GND	20	-	Not Used
21	-	Not Used	22	-	GND
23	I	IOW*	24	-	GND
25	I	IOR*	26	-	GND
27	O	IOCHRDY	28	I	BALE
29	-	Not Used	30	-	GND
31	O	IRQ14	32	O	IOCS16*
33	I	SA1	34	-	Not Used
35	I	SA0	36	I	SA2
37	I	CS0*	38	I	CS1*
39	O	ACTIVE*	40	-	GND

* Active low signal

9.01.3 IDE HOOK-UP

For the hook-up, a 40-pin dual row header signal connector is required. This connector handles all command, data and status I/O lines. Its recommended maximum cable length is 18-24 inches. It connects directly with the onboard 40-pin male header connector at J1.

The drive itself can be mounted in any horizontal or vertical plane.

For a list of recommended devices and connectors, see Appendix D- RECOMMENDED DEVICES & MATING CONNECTORS.

9.01.4 IDE JUMPER

The IDE jumper and its setting appears below:

- W18 IOCHRDY signal to IDE interface:
  - Shorted: Enabled.
  - Or open: Disabled: This is the initial setting.

For location and setting of jumper, refer to Section 2 of this manual.

9.01.5 IDE SOFTWARE SETUP

VIP-UP Setup

In the VIP-UP software utility, the drive letter position C, D and E can be changed, when the first parameter "Disks C: to E: Configuration (BIOS Int 13h)" is set to Enabled.

For more detail on the VIP-UP Setup, refer to Section 15 of this manual.

AMIBIOS Setup

Follow these steps, from the AMIBIOS Setup program's main menu:

- From the Setup window, select the Standard icon.
- From the Standard Setup screen, select the Hard Disk C icon or the Hard Disk D icon.
- An options list displays all valid disk drive types. Select the correct type and press ENTER. If the hard disk drive is an IDE drive, select Detect C: or Detect D: from the Utility window of the main menu to have AMIBIOS automatically detect the IDE drive parameters and report them to this screen.
- You can also enter the hard disk drive parameters: Type, Cylinders, Heads, Write Precompensation, Landing Zone, Sectors, and Capacity.
- Return to the main menu, and select the Advanced icon from the Setup window.
- From the Advanced Setup screen, you can set the IDE BLOCK MODE option in the scroll list: This option enables or disables multiple sector reads and writes for IDE drives.
- Also from the Advanced Setup screen, you can set the following options to support IDE hard disk capacities greater than 500 MB: PRIMARY DRIVES: MASTER LBA MODE; PRIMARY DRIVES: SLAVE LBA MODE; SECONDARY DRIVES: MASTER LBA MODE; and SECONDARAY DRIVES: SLAVE LBA MODE. These options enable or disable the LBA (Logical Block Address) mode for the specified drive; this mode is needed to support IDE partitions greater than 500 MB. IMPORTANT: When you enable LBA mode, your hard drive must not be partitioned; remove partitions before enabling LBA mode (under DOS, use the FDISK command).
- Return to the main menu, and select the Peripheral icon from the Setup window.
- In the Peripheral Setup screen, the ONBOARD IDE option may be set to Enb-PRI (enable primary IDE controller), Enb-SEC (enable secondary IDE controller) or disabled. To modify settings, the PROGRAMMING MODE option must first be set to Manual.

For more detail, refer to Section 14 - AMIBIOS SETUP.

9.02 INSTALLING FLOPPY DEVICES

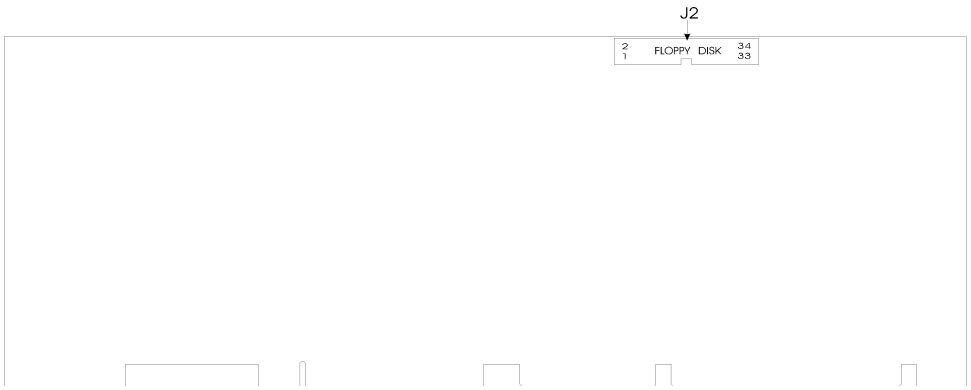
9.02.1 TYPES OF FLOPPY DEVICES SUPPORTED

The floppy disk controller is IBM PC XT/AT compatible (single and double density) and supports Enhanced Floppy Mode (2.88 MB). It handles 3.5 inch and 5.25 inch, low and high density drives. Up to two drives can be supported in any combination.

9.02.2 FLOPPY CONNECTOR LOCATION & PIN-OUT

The Floppy connector appears on Diagram 9-2 at J2.

DIAGRAM 9-2: Floppy Connector Location



The Floppy Connector's pin-out appears in Table 9-2.

TABLE 9-2: Floppy Disk Connector (J2) - Pin-Out

Pin Number	Signal Flow	Signal	Pin Number	Signal Flow	Signal
1	-	GND	2	O	RPM/LC
3	-	GND	4	-	Not Used
5	-	GND	6	-	Not Used
7	-	GND	8	I	INDEX*
9	-	GND	10	O	MOTOR ON 0,1*
11	-	GND	12	O	DRIVE SELECT B*
13	-	GND	14	O	DRIVE SELECT A*
15	-	GND	16	O	MOTOR ON 2*
17	-	N. C. [1]	18	O	DIR CONTROL
19	-	GND	20	O	STEP*
21	-	GND	22	O	WRITE DATA*
23	-	GND	24	O	WRITE ENABLE*
25	-	GND	26	I	TRACK0*
27	-	N. C. [1]	28	I	WRITE PROTECT*
29	-	N. C. [1]	30	I	READ DATA*
31	-	GND	32	O	HEAD SELECT*
33	-	N. C. [1]	34	I	DSKCHG*

* Active low signal

[1] By default, these pins are not connected, however, by installing the W1 and W2 jumpers, these configurations are possible (see also page 9-10 in the manual):

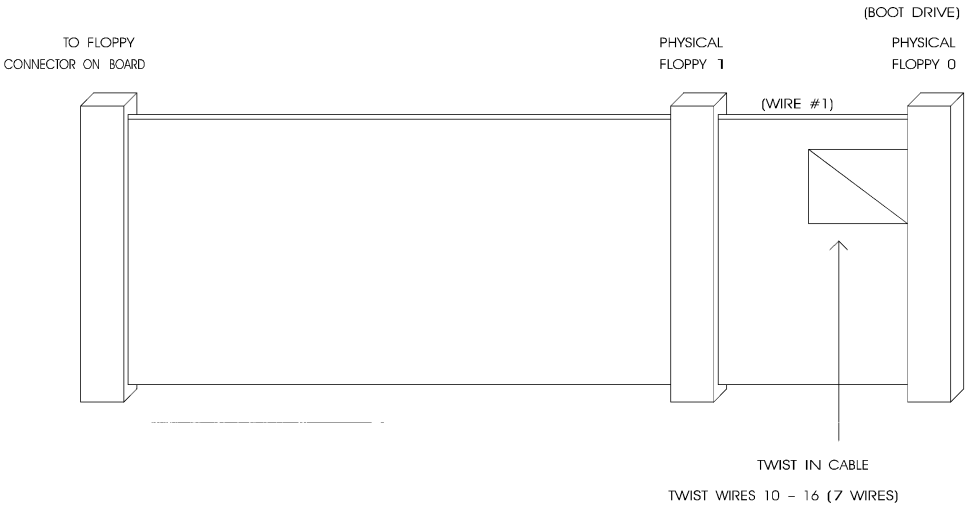
17	GND	Or: 17	EDOUT (2.88 MB)
27	GND	27	HDOUT (2.88 MB)
29	EDOUT (2.88 MB)	29	GND
33	HDOUT (2.88 MB)	33	GND

9.02.3 FLOPPY HOOK-UP

Mechanical Floppy Disk Installation:

The installation of the floppy drives is done via a standard IBM 34-pin flat ribbon cable that connects to J2.

DIAGRAM 9-3: Floppy Disk Cable



Enhanced Floppy Mode:

In order to connect your 2.88 MB floppy drive, simply indicate the proper floppy disk drive in the BIOS Setup program (to be announced); it is not necessary to set the HDOUT and EDOUT media detection signals jumpers.

9.02.4 FLOPPY JUMPERS

There are three possible jumper configurations for the 2.88 MB High Density Floppy EDOUT and HDOUT signals:

(1) W1: No jumper: HDOUT left to software, and
W2: No jumper: EDOUT left to software: This is the initial setting.

(2) W1: Short Pins 1 and 3: HDOUT to Pin 33 (J2), and
Short Pins 2 and 4: Ground to Pin 27 (J2)), and

W2: Short Pins 1 and 3: EDOUT to Pin 29 (J2), and
Short Pins 2 and 4: Ground to Pin 17 (J2).

(3) W1: Short Pins 1 and 2: HDOUT to Pin 27 (J2), and
Short Pins 3 and 4: Ground to Pin 33 (J2), and

W2: Short Pins 1 and 2: EDOUT to Pin 17 (J2), and
Short Pins 3 and 4: Ground to Pin 29 (J2).

These jumpers are optional. Your 2.88 MB Floppy Drive will operate correctly if 2.88 MB is indicated in the BIOS Setup. Not installing these jumpers will work for all floppy disk drives, as long as the proper floppy type is indicated in BIOS SETUP. We recommend you not install these jumpers, for proper operation.

For location and settings of jumpers, refer to Section 2 of this manual.

9.02.5 FLOPPY SOFTWARE SETUP

AMIBIOS Setup

Follow these steps, from the AMIBIOS Setup program's main menu:

- From the Setup window, select the Standard icon.
- From the Standard Setup screen, select the Floppy A icon (or the Floppy B icon).
- The settings are 360 KB 5¼ inch, 1.2 MB 5¼ inch, 720 KB 3½ inch, 1.44 MB 3½ inch, or 2.88 MB 3½ inch.
- Return to the main menu, and select the Peripheral icon from the Setup window.
- In the Peripheral Setup screen, the ONBOARD FDC option may be set to Enabled (enable Floppy Drive Controller) or Disabled. To modify settings, the PROGRAMMING MODE option must first be set to Manual.

For more detail, refer to Section 14 - AMIBIOS SETUP.

10 SERIAL & PARALLEL PORTS

10.01 SERIAL PORTS

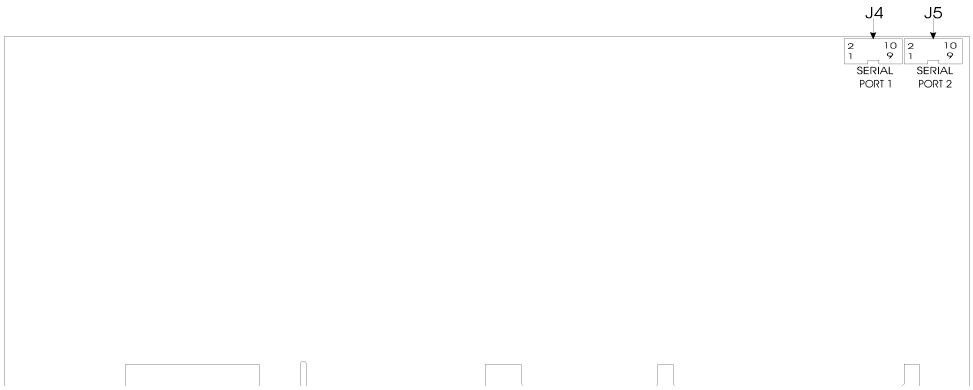
There are two 16C550 compatible serial ports. These have internal 16-byte FIFO buffers for more efficient data transfers.

For information on the programming of serial ports with the use of FIFO buffers, you can ask for Application Note # AN93007 from TEKNOR's Technical Support department.

10.01.1 SERIAL PORTS LOCATION & PIN-OUTS

Serial Port 1 and Serial Port 2 appear on Diagram 10-1 at J4 and J5 respectively.

DIAGRAM 10-1: Serial Ports Location



Serial Port 1 (J4) RS232

The Serial Port 1 is configured as RS232. With the IBM 9-pin DSUB Standard, Serial Port 1 is 100% compatible with the IBM-AT serial port. The following tables show their pin-outs:

TABLE 10-1a: Serial Port 1 (J4) RS232 - Pin-Out

Pin Number / Signal Flow / Signal				Pin Number / Signal Flow / Signal		
DCD	I	1		2	I	DSR
RX	I	3		4	O	RTS
TX	O	5		6	I	CTS
DTR	O	7		8	I	RI
GND	-	9				

TABLE 10-1b: IBM 9-Pin DSUB Standard - Pin-Out

Pin Number / Signal Flow / Signal				Pin Number / Signal Flow / Signal		
DCD	I	1		2	I	RX
TX	I	3		4	O	DTR
GND	-	5		6	I	DSR
RTS	O	7		8	I	CTS
RI	I	9				

TEKNOR offers a 10-pin header to 9-pin DSUB cable for IBM-AT compatibility. This can be purchased from TEKNOR or a cable can be made with a flat cable, a 10-pin flat cable crimp header and a 9-pin DSUB flat cable crimp connector. The use of Taïwanese adapter cables is not recommended, since the pin-out is often incorrect. The direct crimp design offered by TEKNOR allows the simplest cable assembly. All these cables are available from TEKNOR by contacting the Sales department.

Serial Port 2 (J5) RS232

The Serial Port 2 can be configured as RS232 or RS485. As a RS232 port, and with the IBM 9-pin DSUB Standard, Serial Port 2 is 100% compatible with the IBM-AT serial port. The following tables show their pin-outs:

TABLE 10-2a: Serial Port 2 (J5) RS232 - Pin-Out

Pin Number / Signal	Signal Flow			Pin Number / Signal	Signal Flow	
DCD	I	1		2	I	DSR
RX	I	3		4	O	RTS
TX	O	5		6	I	CTS
DTR	O	7		8	I	RI
GND	-	9				

TABLE 10-2b: IBM 9-Pin DSUB Standard - Pin-Out

Pin Number / Signal	Signal Flow			Pin Number / Signal	Signal Flow	
DCD	I	1		2	I	RX
TX	I	3		4	O	DTR
GND	-	5		6	I	DSR
RTS	O	7		8	I	CTS
RI	I	9				

TEKNOR offers a 10-pin header to 9-pin DSUB cable for IBM-AT compatibility. This can be purchased from TEKNOR or a cable can be made with a flat cable, a 10-pin flat cable crimp header and a 9-pin DSUB flat cable crimp connector. The use of Taïwanese adapter cables is not recommended, since the pin-out is often incorrect. The direct crimp design offered by TEKNOR allows the simplest cable assembly. All these cables are available from TEKNOR by contacting the Sales department.

Serial Port 2 (J5) RS485/RS422

If Serial Port 2 is configured for RS485 operation, it can support either full-duplex or party line communication.

Full Duplex Operation (RS422): Upon power-up or reset, the COM2 interface circuits are automatically configured for full duplex operation. Pin 3 and 4 of J5 act as the receiver lines and pin 5 and 6 act as the transmitter lines.

Party Line Operation (RS485): In order to enable party line operation, the user must first write "1" to bit 3 at I/O address 190H (or at 290H or 390H depending on W14 jumper). This allows the transceiver (J5: 3,4) to be controlled by the RTS signal. Upon power-up or reset, the transceiver is by default in "receiver mode" in order to prevent unwanted perturbation on the line.

In party line operation, termination resistors R25 and R26 must be installed only on the boards at both ends of the network.

The following table shows this connector's pin-out:

TABLE 10-3: Serial Port 2 (J5) RS485/RS422 - Pin-Out

Pin Number / Signal Flow / Signal				Pin Number / Signal Flow / Signal		
DCD	I	1		2	I	DSR
RXD(-)	I/O	3		4	I/O	RXD(+)
TXD(-)	O	5		6	I	TXD(+)
DTR	O	7		8	I	RI
GND	-	9				

10.01.2 SERIAL PORTS JUMPERS

Serial ports jumpers and their settings appear below:

- W3, W4, W7 & W8 Serial Port 2 Configuration:

    - Pins 1-2 shorted: RS232: This is the initial setting.

    - Or Pins 2-3 shorted: RS485/RS422.

- W5 RTS2-CTS2 &
  W6 DSR2-DTR2:

    - W5 and W6 shorted: Loopback, or

    - W5 and W6 open: Normal: This is the initial setting.

For location and settings of jumpers, refer to Section 2 of this manual.

10.01.3 SERIAL PORTS SOFTWARE SETUP

AMIBIOS Setup

Follow these steps, from the AMIBIOS Setup program's main menu:

- From the Setup window, select the Peripheral icon. To modify settings, the PROGRAMMING MODE option must first be set to Manual.

- In the Peripheral Setup screen, the SERIAL PORT 1 option may be set to Disabled, 3F8h, 2F8h, 3E8h or 2E8h (if one of these is used by SERIAL PORT 2, it will not appear in the scroll list).

- Also in the Peripheral Setup screen, the SERIAL PORT 2 option may be set to Disabled, 3F8h, 2F8h, 3E8h or 2E8h (if one of these is used by SERIAL PORT 1, it will not appear in the scroll list).

- Also in the Peripheral Setup screen, the IRQ ACTIVE option may be set to Low or High: This option specifies whether the Parallel and Serial Port IRQs are active high or active low.

For more detail, refer to Section 14 - AMIBIOS SETUP.

10.02 PARALLEL PORT

10.02.1 MODES

The parallel port is a multi-mode parallel port supporting the following modes:

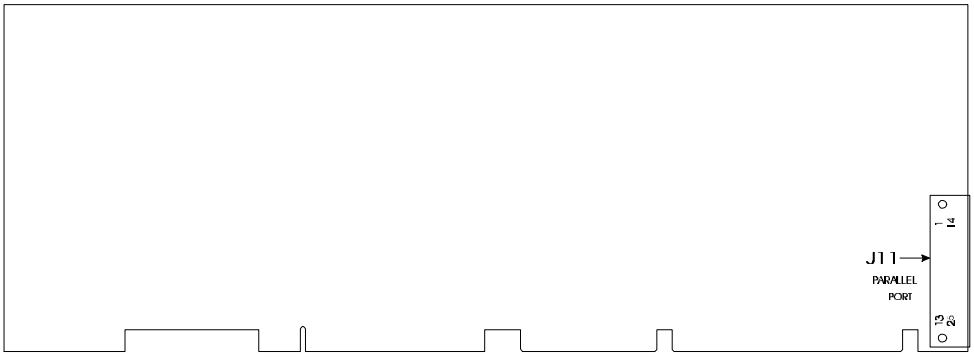
- Standard Parallel Port (SPP): This mode is IBM XT/AT compatible and PS/2 compatible (bi-directional);
- Enhanced Parallel Port (EPP);
- Extended Capabilities Port (ECP).

For more information, on the above modes, the following Application Note is available from TEKNOR's Technical Support department: #AN95001A "Using the FDC37C665/666 Parallel Port".

10.02.2 PARALLEL PORT LOCATION & PIN-OUT

The Parallel Port appears on Diagram 10-2 at J11.

DIAGRAM 10-2: Parallel Port Location



The connection is done through a DB-25 connector located at the edge of the board (J11).

The following table shows the pin-out for this connector, when it is in Standard mode:

TABLE 10-4: Parallel Port Connector (J11) - Standard Mode

Pin Number	Signal Flow			Pin Number	Signal Flow	
Signal						Signal
STROBE*	O	1		14	O	AUTOFD*
D0	I/O	2		15	I	ERROR*
D1	I/O	3		16	O	INIT*
D2	I/O	4		17	O	SELECTIN*
D3	I/O	5		18	-	GND
D4	I/O	6		19	-	GND
D5	I/O	7		20	-	GND
D6	I/O	8		21	-	GND
D7	I/O	9		22	-	GND
ACK*	I	10		23	-	GND
BUSY	I	11		24	-	GND
PE	I	12		25	-	GND
SELECT	I	13				

* Active low signal

The following table shows the pin-out for this connector, when it is in EPP mode:

TABLE 10-5: Parallel Port Connector (J11) - EPP Mode

Pin Number	Signal Flow			Pin Number	Signal Flow	
Signal						Signal
WRITE*	O	1		14	O	DATASTB*
D0	I/O	2		15	-	Not Used
D1	I/O	3		16	-	Not Used
D2	I/O	4		17	O	ADDRSTRB*
D3	I/O	5		18	-	GND
D4	I/O	6		19	-	GND
D5	I/O	7		20	-	GND
D6	I/O	8		21	-	GND
D7	I/O	9		22	-	GND
INTR	I	10		23	-	GND
WAIT*	I	11		24	-	GND
Not Used	-	12		25	-	GND
Not Used	-	13				

* Active low signal

The following table shows the pin-out for this connector, when it is in ECP mode:

TABLE 10-6: Parallel Port Connector (J11) - ECP Mode

Pin Number	Signal Flow			Pin Number	Signal Flow	
Signal						Signal
STROBE*	O	1		14	O	AUTOFD*, HOSTACK[3]
D0	I/O	2		15	I	FAULT*[1], PERIPHRQST*[3]
D1	I/O	3		16	O	INIT*[1], REVERSERQST*[3]
D2	I/O	4		17	O	SELECTIN*[1,3]
D3	I/O	5		18	-	GND
D4	I/O	6		19	-	GND
D5	I/O	7		20	-	GND
D6	I/O	8		21	-	GND
D7	I/O	9		22	-	GND
ACK*	I	10		23	-	GND
BUSY, PERIPHACK[3]	I	11		24	-	GND
PERROR, ACKREVERSE[3]	I	12		25	-	GND
SELECT	I	13				

* Active low signal
[1] Compatible Mode
[3] High Speed Mode

Note: For more information on the ECP protocol, please refer to the Extended Capabilities Port Protocol and ISA Interface Standard (available from Microsoft Corporation) or contact our Technical Support department.

10.02.3 PARALLEL PORT JUMPERS

Parallel port jumpers and their settings appear below:

- W15 Interrupt Signal from onboard Parallel Port:

  - Pins 1-2 shorted: IRQ5 (normally used for LPT2), or

  - Pins 2-3 shorted: IRQ7 (normally used for LPT1): This is the initial setting, or

  - No jumpers: No interrupt signals: IRQ5 and IRQ7 are free.

- W16 DMA Request Signal for ECP mode &
  W17 DMA Acknowledge Signal for ECP mode:

  - No jumpers: This is the initial setting.

  - Or: W16: Pins 1-2 shorted: DRQ1, and
    W17: Pins 1-2 shorted: DACK1.

  - Or: W16: Pins 2-3 shorted: DRQ3, and
    W17: Pins 2-3 shorted: DACK3.

For location and settings of jumpers, refer to Section 2 of this manual.

10.02.4 PARALLEL PORT SOFTWARE SETUP

AMIBIOS Setup

Follow these steps, from the AMIBIOS Setup program's main menu:

- From the Setup window, select the Peripheral icon. To modify settings, the PROGRAMMING MODE option must first be set to Manual.

- In the Peripheral Setup screen, the PARALLEL PORT option may be set to Disabled, 278h, 3FCh or 378h.

- Also in the Peripheral Setup screen, the IRQ ACTIVE option may be set to Low or High: This option specifies whether the Parallel and Serial Port IRQs are active high or active low.

- Also in the Peripheral Setup screen, the PARALLEL PORT MODE option may be set to Normal, EPP (Enhanced Parallel Port), and Extended (ECP - Extended Capabilities Port).

For more detail, refer to Section 14 - AMIBIOS SETUP.

11 VFLASH SOFTWARE

11.01 INTRODUCTION

VFLASH is TEKNOR's Flash EPROM transfer utility program for single board computers. Its main function is to download DOS files to the 2 or 4 MB Flash EPROM disk (U12), also referred to as data Flash.

A Flash EPROM disk created with VFLASH is very much like a hard disk. A partition is created and data is stored in files, just like on a hard disk. The main difference between the two is that this Flash disk is a read-only drive. Therefore, in order to write software to this Flash disk, you must use the VFLASH Transfer Utility.

However, with the FLASH FILE SYSTEM II software from Microsoft, Flash EPROM disks are read/write and may be accessed via DOS commands (this utility is covered in Section 12).

This Section will describe how to use the VFLASH software utility.

11.01.1 VFLASH SOFTWARE OVERVIEW

Depending on your particular configuration, VFLASH can transfer information to the Flash disk in one of two methods:

1. If your VIPer806 is equipped with hard or floppy drives, then VFLASH downloads data directly on the board's Flash EPROM disk.

2. If your VIPer806 does not have floppy or hard disks, then VFLASH must be run from a remote computer which downloads data to the VIPer806 board via a serial link on COM1 or COM2. This mode is recognized in the BIOS extension as Download Mode and is enabled by installing jumper W17 (1-2) on the VIPer806; in this mode, the VIPer806 board waits for signals from the remote computer's VFLASH software.

The first screen of the VFLASH software allows you to choose between direct and serial downloading (the screen is explained in section 11.02 - OUTPUT SELECTION/FIRST SCREEN).

The next screen is where the address and size of the Flash partition to create are determined (explained in section 11.03 - OUTPUT SELECTION/SECOND SCREEN).

The next step is to select the files in the FILE SELECTION screen, which are to be transferred to the Flash EPROM disk (explained in section 11.04 - FILE SELECTION SCREEN).

The next screen is the LIST OF SELECTED FILES; here the file listing can be verified and modified, duplicate files can be renamed or erased, and the Flash disk can be written (explained in section 11.05 - LIST OF SELECTED FILES).

Finally, the last screen to appear is the TRANSFER STATUS OF ONBOARD FLASH PROGRAMMING or the TRANSFER STATUS OF EXTERNAL FLASH PROGRAMMING; this screen displays each of the transfer operations in progress (explained in section 11.06 - TRANSFER STATUS SCREENS).

The above sections explain how to run the program in interactive mode via menus, but it is also possible to run the program without menus by a command which specifies the selected options and files with parameters; this mode is called batch mode (explained in section 11.07 - BATCH MODE).

11.01.2 TYPES OF FLASH EPROM DISKS

With VFLASH, you can create two types of Flash EPROM disks:

1 - Bootable Flash Disk:

This type of Flash EPROM disk must start from the first block and is recognized by the BIOS. Like a hard disk, an active Flash EPROM disk can boot your system. A typical system setup would contain a CONFIG.SYS file to start device drivers, an AUTOEXEC.BAT file to start your software, plus all driver files required (e.g., EMM386.EXE, a MOUSE driver, etc).

To boot from Flash EPROM three conditions must be met:

- You must have the optional 2 MB or 4 MB Flash EPROM installed at U12.
- The bootable Flash EPROM partition must start from the first block.
- The Flash disk must be configured in the VIP-UP Setup as the C: drive (section 11).

2 - Non-bootable Flash Disk:

Unlike bootable Flash disks which must begin at the first Flash block, non-bootable disks can begin anywhere.

11.01.3 VFLASH REQUIREMENTS

VFLASH is designed to operate in an IBM compatible environment.

The MS-DOS operating system has been successfully tested with VFLASH; MS-DOS compatible operating systems such as DR-DOS and PC-DOS should therefore support VFLASH. Operating systems such as QNX and OS-9000 are not supported by VFLASH (other utility programs are available for such operating systems; please contact our Technical Support department for more information).

If you intend to directly program Flash device on the VIPer806, VFLASH must be running on board.

If you need a remote computer to program Flash device on the VIPer806 (host), then the board must be in Download Mode and VFLASH must be running on the remote computer. A serial cable must be connected between the COM1 or COM2 ports, in the same way as in VT100 mode (the remote computer is cabled like a VT100 terminal, see Section 14 - VT100 MODE).

☞ **To properly run VFLASH, you need at least 1 floppy drive, 1 MB of DRAM, MS-DOS® or PC-DOS (version 2 or greater) or DR-DOS (version 3. 41 or greater).**

11.02 OUTPUT SELECTION/FIRST SCREEN

To run VFLASH, simply type "VFLASH" at the DOS prompt and press ENTER.

The first OUTPUT SELECTION FOR THE TRANSFER screen appears with the following options:

On board Flash devices.

External Flash devices via serial link.

Quit VFLASH and return to DOS.

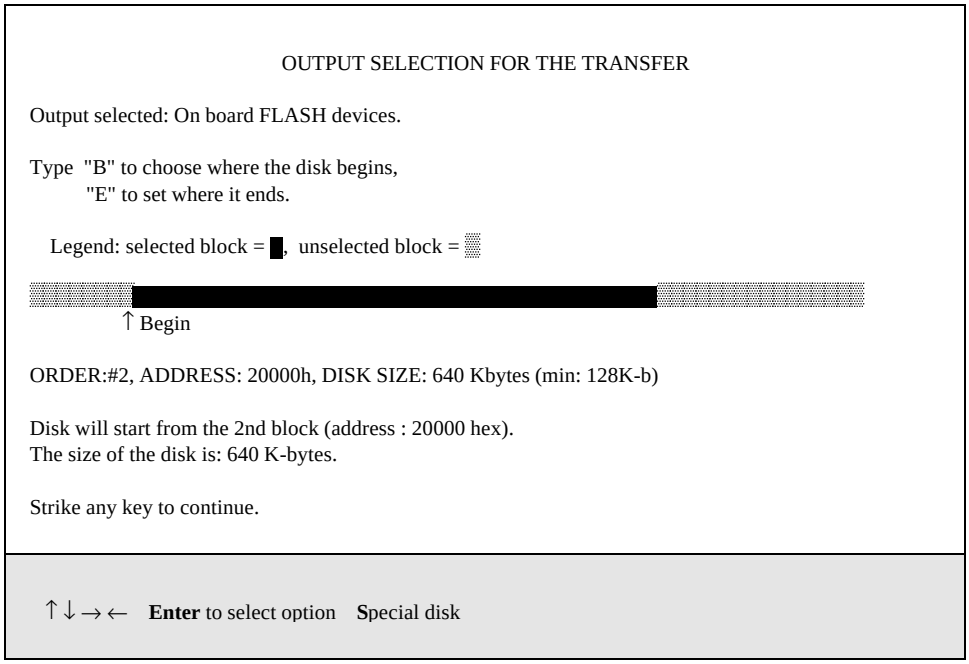
Use the ↑ and ↓ keys to highlight the option and then press ENTER to select.

On board Flash Devices: Use this option when VFLASH is run on a Board with Flash EPROM to be programmed directly on the board.

External Flash Devices via a Serial Link: Use this option when VFLASH is run from a remote computer, or when your VIPer806 has no floppy or hard disks, or simply because the data to transfer is on a different computer than the VIPer806 and Flash EPROM disk. The transfer takes place via a serial link on COM1 (3F8H) or COM2 (2F8H) from the remote computer to the VIPer806.

11.03 OUTPUT SELECTION/SECOND SCREEN

Once onboard or external Flash is selected, a second screen appears as follow.



On the first line, the output selected will be displayed ("On board FLASH devices" or "External FLASH devices via serial link".

The rest of the screen allows you to divide or partition the Flash disk according to your needs. The default disk always starts at the beginning of the Flash space and the size is all Flash selected. Therefore, a full bar will be displayed below the legend.

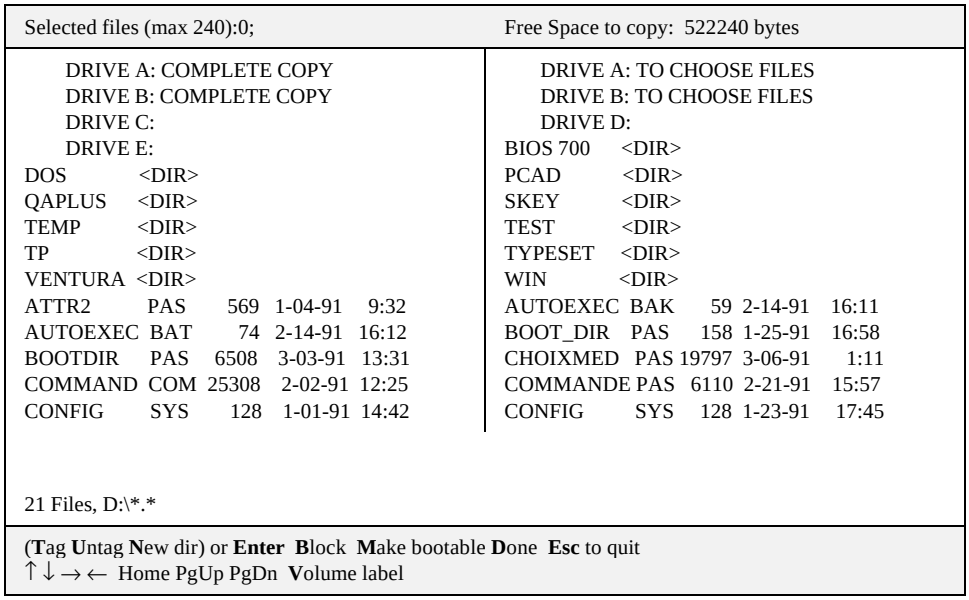
Directly below the bar is a BEGIN pointer. It shows where the Flash partition will begin. The next line shows physical parameters such as the starting block ADDRESS and the DISK SIZE of selected blocks. It also shows the minimal partition size you have available. The minimal disk size can be altered by the /G:x option (for details on this option, please refer to Section 11.07 - BATCH MODE).

Moving the BEGIN pointer with the horizontal arrow keys allows you to select the desired starting block (i.e., address) of the disk.

To set the size of the disk, type "E" and move the END pointer to the end of the disk with the horizontal keys to set the size of the disk.

11.04 FILE SELECTION SCREEN

Once you have selected the output, the following information is displayed on screen:



This menu allows the user to choose the files that will eventually make up the Flash disk. Files can be chosen from the various drives on the system.

The top line in this menu gives size information about the Flash partition. SELECTED FILES indicates how many files have been chosen up to this point. FREE SPACE TO COPY indicates the available Flash space found, minus the space used up by the selected files.

The largest block of information (center screen) is the FILE AREA. It lists the files in the current directory.

Highlighted files are marked for copying to Flash devices.

Entries marked with a "<DIR>" extension indicate a subdirectory. When you select a subdirectory, the first two entries are displayed as ". <DIR>" and ". . <DIR>". As with DOS, "." refers to the actual directory and ". ." to the parent directory. Thus, if you do a "Newdir" command on the ". . <DIR>" you will return to the previous directory.

Entries marked as "Drive A:" or "Drive B:" allow you to change drives/directories or to select files. "DRIVE A/B: TO CHOOSE FILES" is used to select files. "DRIVE A/B: COMPLETE COPY" is used to make an exact copy of a floppy disk to Flash. This last function resembles a DOS DISKCOPY command. When this mode of transfer is chosen, no other files can be sent along with the diskette files. Note that you cannot use a write-protected floppy disk to create a bootable Flash disk.

The bottom of the screen is dedicated to the MESSAGE AREA and MENU COMMANDS.

The MESSAGE AREA gives indications and warnings with respect to file selection operations.

The MENU COMMANDS begin with a highlighted letter or identifier which indicates the key to press in order to execute the desired function. The following commands are available:

TAG: Use this function to select a file from the above file list. Simply move the cursor over the desired field and press T on your keyboard. The file will then be highlighted - indicating it was selected. If you press T again, you deselect the file.

UNTAG: This function is used to deselect a chosen file from the above list of files. To use this function, simply move the cursor over the desired file and press U.

BLOCK: This function is used to mark a group of files for selection or deselection. Move the cursor to the beginning of the first file you wish to select and press on the B key (a "➢" symbol will be displayed after "Block" in the command area to remind you that a block has been entered). Then, move the cursor to the last file of the group and press B again (a "➣" will appear next to the "➢" indicating that a block definition is now complete). The block of outlined files are now ready to be "Tagged" or "Untagged".

MAKE BOOTABLE: Choose this function to move files you wish to make bootable into the FILE SELECTION area (to appear in the LIST OF SELECTED FILES screen). The system will then prompt you for the drive which contains the system files (Note that the source should not be a Flash disk, since these are read-only and write protected). Once the selected files are found, the "Make Bootable" command will be changed to "BOOTABLE DISK". This confirms that the Flash disk will be bootable.

NEWDIR: This function lets you enter or exit a drive or directory. To change directories, place the cursor at the desired entry and press N. The listing will automatically change to the new directory's content.

ENTER: Press ENTER to either tag, untag, or change directory. When the cursor is on a directory, ENTER is equivalent to "Newdir". When the cursor is on a file, pressing ENTER will tag/untag it.

DONE: Use this function when the file selection is terminated. Press D and the next screen will appear (LIST OF SELECTED FILES).

ESC: Press the ESC key to abort VFLASH without modifying any information in the Flash devices. The system will prompt you before exiting to DOS.

VOLUME LABEL: Use this function to include a disk volume label for the Flash EPROM disk. Simply press V on your keyboard to bring the message into the following format:

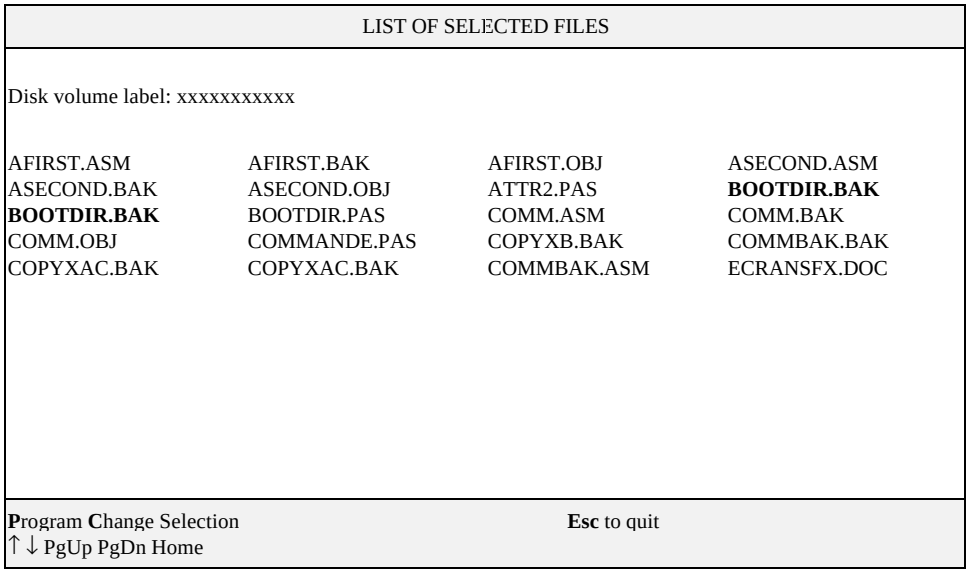
Volume is xxxxxxxxxxx
Volume label (11 characters, ENTER for none)?

The same operating system limitations on volume label names apply.

The cursor can be moved within the FILE SELECTION screen by using the ↑, ↓, →, ←, PAGE UP, PAGE DOWN and HOME keys.

11.05 LIST OF SELECTED FILES SCREEN

The LIST OF SELECTED FILES screen shows you the list of files that the Flash disk will contain.



The list of previously selected files appears in the center of the screen.

You can browse through the list by using the ↑, ↓, PAGE UP, PAGE DOWN and HOME keys.

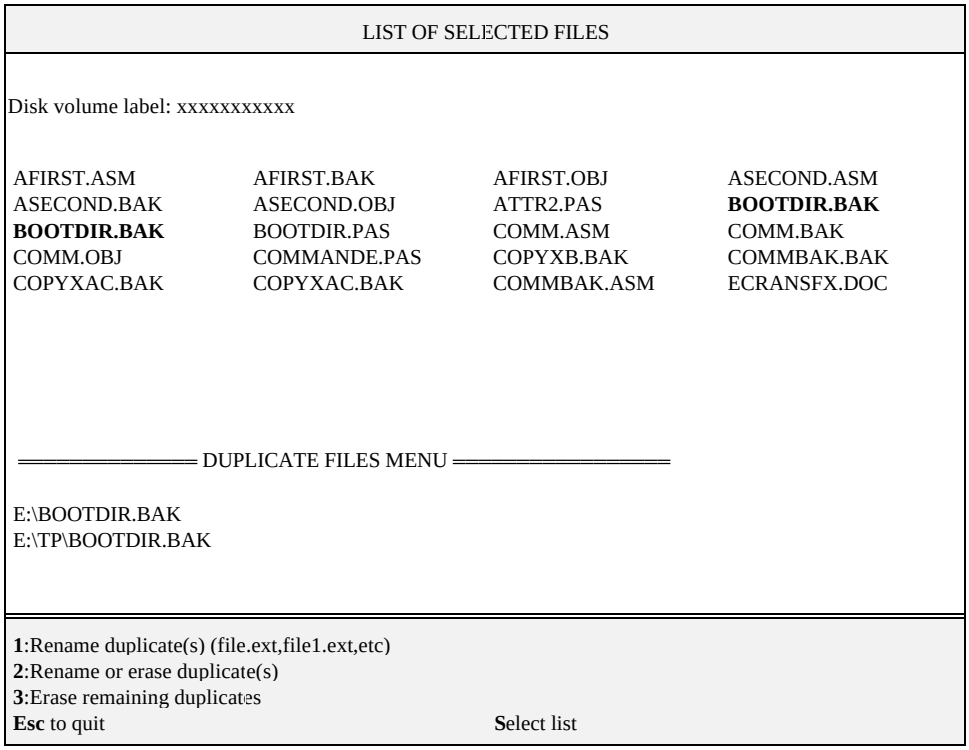
The following commands are also available:

CHANGE SELECTION: This option allows you to return to the FILE SELECTION screen by pressing C.

PROGRAM: Press P to enter the Programming (TRANSFER STATUS ...) screen. This will begin programming the Flash devices - according to the transfer mode selected (on board or external Flash).

ESC: This allows you to abort VFLASH and exit to DOS without modifying the contents of the Flash devices.
If duplicate files are found, the DUPLICATE FILES MENU section appears below the list of selected files. This section will appear only if two or more files with the same

name are found. When this occurs, a menu will automatically appear in the bottom section to solve the conflict:



Make a selection by choosing the corresponding number. Choosing:

1. Will force a rename by appending a numeral at the end of the filename.
2. Will erase or rename files manually.
3. Will erase all duplicates.

When the final selection has been made and the final listing is displayed, the Flash disk can then be written.

11.06 TRANSFER STATUS SCREENS

11.06.1 TRANSFER STATUS OF ONBOARD FLASH PROGRAMMING SCREEN

TRANSFER STATUS OF ONBOARD FLASH PROGRAMMING
Erasing of all Flash devices installed, please wait. . . Erasing nth device. . . Erase completed Creating a bootable flash disk Transferring the BOOT sector, FAT and root DIR . . . Completed Copying selected files. . . Transfer completed: XX. X% Transferring: FILENAME Transfer complete

This screen displays each of the transfer operations in progress:

1. First, the Flash devices are erased. This operation can take some time to complete. Only the Flash devices of the actual disk to be programmed will be erased, however.

2. The base system information is then transferred. This is followed by the file data itself.

3. The transfer in progress is displayed by XX%, and the actual file being copied is also shown (unless a complete diskette copy is performed).

Restart the system if the disk is to be recognized by the TEKNOR BIOS extension. Although rebooting is not necessary if Flash disks were not created, it is a recommended procedure in all circumstances.

11.06.2 TRANSFER STATUS OF EXTERNAL FLASH PROGRAMMING SCREEN

When a serial link is used, the following screen will be displayed:

TRANSFER STATUS OF EXTERNAL FLASH PROGRAMMING
Erasing of all Flash devices installed, please wait. . . Erase completed Creating a bootable flash disk Transferring the BOOT sector, FAT and root DIR. . . Completed Copying selected files. . . Transfer completed: XX. X% Transferring: FILENAME Elapsed time: Xmin XXsec Transfer complete

The above screen is used to display the transfer operation status. It shows each step in progress:

1. The devices are erased (this may take some time).

2. The base system information is transferred, followed by the file data itself.

3. The data progress is displayed by XX% up to 100%. The actual file being sent is also shown (unless a complete diskette copy is performed). In addition, the elapsed time of the transfer is displayed.

If an error occurs during transfer, the system beeps twice to warn the user.

To signal the end of a successful transfer, a single beep is heard.

☞ **The transfer operation can be time consuming in Serial Mode due to the serial transfer speed and protocol.**

4. When the transfer is 100% complete, the following message is displayed:

    Do you want to Reset the receiving system?

This software command is made available to restart the receiving system by remote. In order for a new Flash disk to be recognized by the BIOS and DOS, the system must be rebooted.

The receiving system can be put in Download Mode by any of the following options:

1. Short Pins 1 and 2 on jumper W17. This forces Download Mode at boot up.

2. Download Mode is automatically enabled when VT100 Mode is activated by shorting Pins 3 and 4 on jumper W17. In this case, the communications port will recognize the Download Mode commands and activate it.

☞ **Reset is the only way to exit from Download Mode which is forced on at setup by the W17(1-2) jumper. If Download Mode was entered by recognition of the code sequence, you can simply exit Download Mode and continue processing.**

11.07 BATCH MODE

While files can be manually selected using the Interactive Mode, automatic transfers of a predefined area (a sub-directory or preferably a diskette) can be achieved through Batch Mode.

In Batch Mode, a user or field technician with no previous knowledge of the system can easily effect a transfer to the Flash disk. This can be done either by calling a batch file (*.bat) or by simply issuing the proper command line parameters directly from DOS.

When the transfer is complete, reset the system. This allows the BIOS and DOS to recognize the new Flash disk.

Keep in mind that Batch Mode can be called directly from a floppy or hard disk, from a remote computer, or from a portable computer. In each case, the selected files can be downloaded to the Flash devices.

Batch Mode returns error codes (errorlevel) that can be read by a DOS batch file or by a high level language program.

11.07.1 BATCH MODE COMMAND LINE PARAMETERS

The command line format is as follows:

VFLASH [drive:] [\directory] [destination] [options]

where:

[drive:] is the source drive from which a complete copy will be made if no directory is specified (see section 11.04, for more information).

[\directory] is the path used to show from which directory the source files will be taken and transferred to the Flash or EPROM files. If you do not specify a directory (for example, VFLASH B:\), only the files in the root directory will be transferred to the Flash disk. Also, if the Flash disk is to be bootable, the /B option must be used.

Each option or switch starts with a '/' character followed by one or more letters. These letters are in uppercase and are used by VFLASH to identify a specific option.

A colon ':' or pound '#' character is also a necessary part of the switch. Lowercase letters represent a variable field that must be entered. Each switch may be separated by a space if you so choose.

The switches may be written in random order except for switches that are linked together. For example a /S must be followed by either /#order or /sizeK or both. Thus, a command line such as VFLASH B: /M /S/#2/128K is valid, however, VFLASH B: /S/M/#2/128K is not. The following list of options provides complete descriptions.

The first three options listed are not required to execute a disk. They can be used either in Interactive Mode or Batch Modes.

[options]

/G:group Specifies how many Flash blocks will be grouped together as a cluster. The Group Factor will set the smallest disk size available. Valid group values are defined as 1, 2, 4, 8, 16... and so on.

/M Instructs VFLASH to use a monochrome display pattern. This option is useful with LCDs since it may be difficult to distinguish colors with such displays.

/VT100 This option allows a visual monitoring of the transfer operation in progress while in VT100 mode. Use this switch when you make an onboard Flash disk.

The following options identify disk or file parameters to be executed in BATCH mode.

/B/bootdrive:
Makes the disk bootable by transferring the bootable files from the 'bootdrive' specified. Note that the source should not be a Flash disk, since these are read-only and write protected.

/E Performs an external transfer by serial link to the remote system. This switch must be present in order to use any of the next three options (/RATE, /COM2 and /R).

/rate The value entered corresponds to the desired baud rate for transfer. Any one of the following can be used: 300, 1200, 2400, 9600, 19200, 38400. It is set at 19200 by default.

/COM2 This option instructs COM2 to be used instead of the default value COM1.

/R Instructs VFLASH to reset the VIPer806 upon completion of download operation. This is valid only in VT100 Mode. In Download Mode, the remote system is always reset.

/S Used to create a special disk or partition. This option precedes the starting device number option (/#order) or the disk size option (/sizeK), or both.

/#order Specifies the Flash block to be used as the starting point for a disk partition (default setting is #1).

/sizeK Specifies a special disk size, in KB, for the Flash disk. The default setting is the largest disk size following the designated starting disk as selected in the /#order option).

/V:volume label

This switch specifies a volume label for the disk to be created. This option will report an invalid command line error if it is used while transferring a complete copy of a floppy disk. Since it is acceptable to have spaces in a volume label, do not place this switch before [drive:], [\directory] or [destination] since VFLASH would not be able to determine when the label ends and when these options begins.

To get a summary of the Batch Mode options from VFLASH, simply run VFLASH with the command line '/?' or '/HELP' (type 'VFLASH/?' or 'VFLASH/HELP'). Either command will display a Batch options summary and some examples of valid VFLASH command lines. The same help information will also be displayed each time VFLASH detects an error in the command line.

11.07.2 BATCH MODE ERROR CODES

The following error messages are returned by the VFLASH Batch Mode function. They can be detected with a DOS errorlevel condition.

ERROR (HEX)	NUMBER (DECIMAL)	DESCRIPTION
0	0	No error.
1	1	Bad command line.
2	2	Invalid drive choice for recovering boot information.
3	3	Unable to establish communication (serial download mode only).
4	4	No Flash memory found (verify jumper).
5	5	Mixed memory types detected in Flash bank.
6	6	Unable to find system files on specified disk.
7	7	Specified output file already exists.
8	8	Error reading transfer source drive.
9	9	Insufficient data space or directory space to copy all desired files.
A	10	Bad checksum (problem with serial link).
B	11	Non Hex code received (problem with serial link).
C	12	Error transferring data. Unusable Flash drive.
D	13	No files to transfer in selected directory.
E	14	Unable to open a file to be copied.
F	15	Media not yet supported.
10	16	Communications or device error while transferring files. Unusable flash drive.
11	17	Unable to read transfer source drive.
12	18	Insufficient Flash space to store files.
13	19	Unrecognized Flash device type.
14	20	Programming failure on devices.
15	21	Cannot select any file from actual Flash disk.
16	22	Unable to find sourcefiles.
17	23	Cannot specify starting device on remote system.
18	24	Cannot find starting flash bank address.
19	25	Communication error while reading Flash bank content.
1A	26	External device cannot be erased properly.
1B	27	Unsupported serial download function.

ERROR (HEX)	NUMBER (DECIMAL)	DESCRIPTION
1C	28	Flash content does not verify with source.
1D	29	No device found in specified starting socket.
1E	30	Cannot create a flash disk of specified size.
1F	31	Communication error when reading flash identification code.
20	32	Cannot use 8086 or 8088 CPU with flash memory.
21	33	No serial port or card attached for transfer.
22	34	/S switch not supported with this BIOS.
23	35	/G:group value on command line is invalid.
24	36	Insufficient Flash or EPROM space to include the volume label entry.
25	37	Cannot make EPROM with same [source] and [destination] path.
26	38	EPROM filename already exist.
27	39	EPROM filename path not found.
28	40	Selected drive for EPROM files not ready.
29	41	Invalid EPROM filename or disk error.
2A	42	Not enough disk space to copy EPROM files.
2B	43	Not enough memory for data buffer.
2C	44	Command line option "/TEKXXX" is invalid.
2D	45	486SLC internal registers are different from BIOS setup.
2E	46	The 486SLC cache is not disabled over the Flash device(s).
2F	47	Unable to erase the nth device.
30	48	No VIPer BIOS found.
31	49	The source diskette must be DOS Version 4 and up.
32	50	Flash ID command to BIOS or data Flash must be issued first.

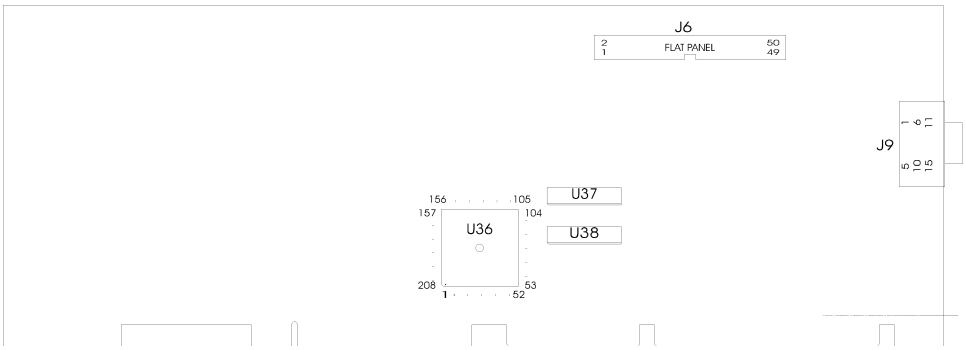
12 VIDEO

12.01 LOCATION OF VIDEO COMPONENTS

Video components appear on Diagram 12-1 as follows:

- Flat Panel / CRT VGA Controller at U36;
- Video Memory (1 MB DRAM) at U37 and U38;
- Flat Panel Connector at J6;
- VGA Connector at J9.

DIAGRAM 12-1: Video Components Location



12.02 FLAT PANEL / CRT VGA CONTROLLER

The TEK932's Flat Panel / CRT VGA controller is a single-chip video controller from C&T (F65545). It's highly integrated design includes Flat Panel / CRT controller, RAMDAC and clock synthesizer.

The VGA Flat Panel/ CRT controller provides a low-power solution for high performance, full-featured notebook / sub-notebook and other portable applications that require the highest graphics performance available.

It supports direct interface to color and monochrome Dual-panel, Dual-drive (DD) and Single-panel, Single-drive (SS) passive STN and active-matrix TFT / MIM LCDs, EL and plasma panels.

The controller is fully compatible with the IBM™ VGA standard at the hardware, register, and BIOS level. It also provides enhanced backward compatibility to EGA™ and CGA™ standards.

12.02.1 DISPLAY INTERFACE

The video controller is designed to support a wide range of Flat Panel displays and all types of CRT displays.

Flat Panel Displays:

- Supports plasma, Electro Luminescent (EL) and Liquid Crystal Displays (LCD).
- LCD panel interfaces are provided for single panel-single drive (SS) and dual panel-dual drive (DD) configurations. A single panel sequences data similar to a CRT (sequentially from one area of video memory). A dual panel requires video data to be provided alternating from to separate areas of video memory; it also requires the data from the two areas to be provided to the panel simultaneously.
- No additional components or external hardware, such as a frame buffer, is required.
- Allows interfacing to the widest possible range of flat panel displays; provides direct interface to panels from Sharp, Sanyo, Epson, Seiko Instruments, Oki, Toshiba, Hitachi, Fujitsu, NEC, Matsushita/Panasonic, Planar and others.

CRT Displays:

- Supports high resolution fixed frequency and variable frequency analog monitors in interlaced and non-interlaced modes of operation.
- Supports resolutions up to 1024 x 768 (256 colors), 800 x 600 (256 colors) or 640 x 480 (16,777,216 colors) in 1 MB display memory configurations; 1024 x 768 (16 colors) or 800 x 600 (256 colors) in 512 KB display memory configurations.

Simultaneous Flat Panel / CRT Display:

- Provides simultaneous display operation with Multi-Sync variable frequency or PS/2 fixed frequency CRT monitors and single panel-single dirive LCDs (LCD-SS), dual panel-dual drive LCDs (LCD-DD), and plasma and EL panels (which employ single panel-single drive interfaces).

12.02.2 DISPLAY ENHANCEMENT FEATURES

"TRUE-GRAY" Gray Scale Algorithm:

A proprietarty algorithm generates a maximum of 61 gray levels on monochrome panels. With this technique, the video controller produces up to 61 flicker-free gray scales on the monochrome STN LCDs.

RGB Color To Gray Scale Reduction:

The 24 bits of color palette data from the VGA standard color lookup table (CLUT) are reduced to 6 bits for 64 gray scales via one of three selectable RGB to gray scale reduction techniques:

- NTSC Weighting: 5/16 Red, 9/16 Green, 2/16 Blue.
- Equal Weighting: 5/16 Red, 6/16 Green, 5/16 Blue.
- Green Only; 6 bits of Green only.

SmartMap™:

SmartMap™ can be invoked to intelligently map colors to gray levels in text mode. It improves legibility of flat panel display by solving a common problem: The variety of colors which can be quite distinct on a color CRT monitor can be illegible on a monochrome flat panel display if the colors are mapped to adjacent gray scale values. SmartMap™ compares and adjusts foreground and background gray scale values to produce adequate display contrast on flat panel displays. This feature can be disabled if desired.

12.02.3 DISABLING VIDEO DISPLAY

The video controller can be disabled by shorting pins 7 and 8 on the W12 jumper. See Section 2 for jumper location and settings.

This feature is useful when an external video card is required for testing or other purposes.

12.03 VIDEO MEMORY (DRAM)

Video RAM is factory installed. The TEK932 is configured with 1 MB of video memory.

12.04 FLAT PANEL CONNECTOR (J6)

12.04.1 FLAT PANEL CONNECTOR PIN-OUT

TABLE 12-1: Flat Panel Connector (J6) - Pin-Out

Pin Number	Signal	Pin Number	Signal
1	ENAVDD	2	VCC (+5V)
3	ENAVEE	4	STNDBYE*
5	ENABLK	6	GND
7	M/DE	8	ACTI
9	GND	10	LP/DE
11	FLM	12	GND
13	SHFCLK	14	GND
15	P0	16	P1
17	GND	18	P2
19	P3	20	GND
21	P4	22	P5
23	GND	24	P6
25	P7	26	GND
27	P8	28	P9
29	GND	30	P10
31	P11	32	GND
33	P12	34	P19
35	GND	36	P14
37	P17	38	P18
39	P18	40	P17
41	GND	42	P18
43	P19	44	GND
45	P20	46	P21
47	GND	48	P22
49	P23	50	GND

* Active low signal

12.04.2 FLAT PANEL INSTALLATION

The myriad of Flat Panel displays available makes it virtually impossible for us to show every type of configuration that exists. For your convenience, we have published the TEK932 FLAT PANEL CONFIGURATION GUIDE; this handy manual charts out the cabling, jumper settings, and other special requirements for some of the most popular displays.

The name of the Flat Panel BIOS file (.BFP extension) that you must use to update the Flash EPROM BIOS is also included in this guide; see Section 18 to learn how to perform a VGA BIOS file update with the UBIOS software.

Most Flat Panel displays require a special adapter board or cabling between them and the TEK932.
Please contact our Sales or Technical Support departments for more information on Flat Panel applications.

12.05 VGA CONNECTOR (J9)

Connecting CRT video to the TEK932 is simple. Merely connect the standard VGA DB15 male connector to the board's J9 high density, right angle, female connector.

The VGA connector's pin-out appears in Table 12-2.

TABLE 12-2: VGA Connector (J9) - Pin-Out

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
1	RED	6	GND	11	Not Used
2	GREEN	7	GND	12	Not Used
3	BLUE	8	GND	13	HSYNC
4	Not Used	9	Not Used	14	VSYNC
5	GND	10	GND	15	Not Used

13 POWER MANAGEMENT

13.01 SYSTEM CONTROLLER'S POWER MANAGEMENT FEATURES

The System I/O chip (located at U35; also referred to as the ISA Bridge) provides a green power management port for controlling desktop sub-systems which may include clock control to the CPU's clock, STPCLK# signal to the CPU, and monitor shutdown.

The chip provides a Green Event Timer (GET) used to activate the SMI_GREEN mode. The GET countdown timer will reload under the following events:

- All IRQs.
- One programmable I/O range.
- All DMA requests.
- Keyboard access: I/O ports 60h and 64h.
- Video access:
  - 0A0000-0BFFFF address trap (graphics buffer);
  - I/O port 3B0h-3DFh (VGA command registers).
- Hard/Floppy access:
  - I/O port 1F0h-1F7h and/or 3F6h, 170h-177h (Hard Disk);
  - I/O port 3F5h (Floppy).
- External EPMI source: Additional input pin to the Controller from external PMI source.
- All interrupt vector addresses (00h to 0ffh, corresponding to address 00h to 3ffh) with two maskable vector addresses.

Any of the following conditions will allow the system to return to the normal state, if the event was programmed to allow the system to go into SMI_GREEN mode:

- All IRQs.
- External EPMI.
- One programmable I/O.
- Keyboard access.

- Video access.
- Hard/Floppy access.
- External EPMI source.
- All interrupt vector addresses.

In normal state, the system is running at full speed; no power management features are activated.

In the SMI_GREEN mode state, power management is allowed through the SMI# protocol. After the GET expires, SMI# will be generated from the chipset to the CPU. The chipset will flush the Internal Cache Memory, and then remap all 3XXXX memory accesses with the assertion of SMIACT#. The CPU will save all of its internal registers and then begin executing the SMI code. In the SMI code, the System I/O's green power management port will be writtren from registers A0h through AEh. This register can control the STPCLK#.

The system can resume out of SMI_GREEN mode by any event previously programmed IRQ or EPMI in the system activity register.

13.02 RESET CIRCUIT

13.02.1 EXTERNAL RESET CIRCUIT SWITCH

The TEK932 can be reset by activating an external reset switch.

This switch should be connected between pin 13 (PBRESET) and pin 14 (GND) on the Multi-Function Connector (J3).

This provides an easy and effective way of resetting the system.

See Section 6.11 for more information.

13.02.2 ONBOARD POWER DETECTION

An onboard device which is part of the reset circuit constantly monitors the voltage which powers the board. Normally, the board is powered with 5 V; if the supply voltage drops below 4.65 V (a typical threshold), the onboard circuitry will reset the board and the system. This reset has the same effect on the system as the reset button.

13.03 POWER FAIL DETECTION CIRCUIT

The Power Failure Detector monitors:

- The backup battery to warn of a low battery condition, and
- The +5 V power supply to detect when it falls below 4.75 V.

If either of the two above conditions occur, the PFO (Power Fail Output signal) goes low. In turn, the PFO is connected to the IOCHK* line to generate a non-maskable interrupt (NMI).

Power fail monitoring is enabled by shorting the W13 jumper. The jumper's location and setting are illustrated in Section 2.

13.04 WATCHDOG TIMER

The Watchdog Timer is extremely useful in embedded systems where human supervision is not required. Following a reset, the Watchdog is always disabled. The Watchdog is enabled once you write "1" in bit "0" at address 190H the first time (or at 290H or 390H depending on the W14 jumper setting). When enabled, the microprocessor must refresh the Watchdog. This is done by writing alternatively "0" and "1" to bit 1 at address 190H (or at 290H or 390H), once every 1.6 seconds to verify proper software execution.

If a hardware or software failure occurs such that the Watchdog is not refreshed, a reset pulse is generated by the Watchdog to restart the processor.

☞ **The user program must provide the first access to address 190H (or at 290H or 390H depending on the W14 jumper setting), and must also include the refresh routine. In addition, be certain to keep a mirror image of register 190H (or 290H or 390H) when programming it. This is necessary since the register is a write-only user register and, as a result, is not used by the system BIOS.**

TABLE 13-1: Watchdog Timer Register

ADDRESS		REGISTER
190H, 290H OR 390H: Bit 0	Read/Write	Watchdog enable
190H, 290H OR 390H: Bit 1	Read/Write	Watchdog refresh

A TEK932 SPECIFICATIONS

A.01 BOARD SPECIFICATIONS

Operating Temperature: 0° to 50°C (with airflow)

Noncondensing Relative Humidity: 5% to 75%.

Electrical: Conforms to the electrical specifications in IEEE P996 Bus Specification (PC/AT), the PCI Local Bus Specification, Revision 2.1 and the PICMG, Revision 2.0.

Supply Voltage: VCC =+ 5V ±5%
±12V ±5%.

Supply Current:

TABLE A-1: Supply Current

SUPPLY CURRENT	iCOMP Index 610 (75 MHz)	iCOMP Index 735 (90 MHz)	iCOMP Index 815 (100 MHz)
ICC Typical * (+5V)	3.30 A	4.00 A	4.10 A
ICC (SMI)	1.85 A	2.05 A	2.14 A
IPP (+12V)	10 mA	10 mA	10 mA
IPP (-12V)	5 mA	5 mA	5 ma

* Measured with 8 MB System Memory (DRAM), 256 KB System Cache, 2 MB Flash EPROM and 1 MB Video Memory (DRAM)

Mechanical:

- Conforms to the mechanical specifications in IEEE P996 Bus Specification (PC/AT), the PCI Local Bus Specification, Revision 2.1, and the PICMG, Revision 2.0.
- 4.80 in. x 13.33 in. / 121.9 mm x 338.5 mm.

A.02 MTBF

The reliability analysis performed on the TEK932 reflects all available options and has resulted in the following predicted reliability:

TABLE A-2: Reliability Prediction

Standard Configuration		CPU	MTBF (Hours)	Failure Rate ($x10^{-6}$)
Option 1:	Basic board	Pentium 75 MHz	39083	25.5863
		Pentium 90 MHz	38801	25.7726
		Pentium 100 MHz	38524	25.9576
Option 2:	Option 1 plus 256 MB Cache memory	Pentium 75 MHz	35110	28.4817
		Pentium 90 MHz	34882	28.6680
		Pentium 100 MHz	34658	28.8530
Option 3:	Option 1 plus 512 MB Cache memory	Pentium 75 MHz	34702	28.8165
		Pentium 90 MHz	34479	29.0028
		Pentium 100 MHz	34261	29.1878
Option 4:	Option 1 plus 16 MB Flash EPROM memory	Pentium 75 MHz	38006	26.3117
		Pentium 90 MHz	37739	26.4980
		Pentium 100 MHz	37477	26.6831
Option 5:	Option 2 plus 16 MB Flash EPROM memory	Pentium 75 MHz	34238	29.2071
		Pentium 90 MHz	34021	29.3934
		Pentium 100 MHz	33808	29.5785
Option 6:	Option 3 plus 16 MB Flash EPROM memory	Pentium 75 MHz	33850	29.5419
		Pentium 90 MHz	33638	29.7283
		Pentium 100 MHz	33430	29.9133
Option 7:	Option 1 plus 32 MB Flash EPROM memory	Pentium 75 MHz	37854	26.4170
		Pentium 90 MHz	37589	26.6033
		Pentium 100 MHz	37330	26.7883
Option 8:	Option 2 plus 32 MB Flash EPROM memory	Pentium 75 MHz	34115	29.3123
		Pentium 90 MHz	33900	29.4986
		Pentium 100 MHz	33689	29.6837
Option 9:	Option 3 plus 32 MB Flash EPROM memory	Pentium 75 MHz	33730	29.6472
		Pentium 90 MHz	33519	29.8323
		Pentium 100 MHz	33313	30.0185

The MTBF is estimated using the prediction data from MIL-HDBK-217F, Reliability Prediction of Electronic Equipment (Dec. 1991).

The TEK932 board is considered functioning in a Ground Fixed environment as defined in MIL-HDBK-217F. The calculations are performed at 20°C with a temperature rise of 10°C which is due to heat dissipated by active components.

It is assumed that only one failure at a time can occur and that the failure of any component will result in the system becoming inoperative or, as a minimum, resulting in a degraded mode of operation requiring repair action. All components are considered as having an exponential distribution of time to failure, with a constant failure rate. A failure rate is attributed to each component called in the parts list, according to the stress levels it is submitted during normal operation.

The components with the highest calculated failure rate in the TEK932 reliability prediction are: the chipset (82434NX/82433NX), the four 74HCT245, the T932_1 PCB and the Pentium CPU.

A.03 MEETING INDUSTRY STANDARDS

TEKNOR Quality Standards insist that our products meet or exceed industry standards set by such respected agencies, organizations and associations as UL and CSA.

As a result, the TEK932 has the following built-in features to help ensure that the conditions required for approval are met:

- A current block diode on the battery circuit,
- A current limiter resistor on the battery,
- A protection fuse on the keyboard controller.

TEKNOR computer cards are designed to meet industry standards for customers requiring approval for their equipment.

B MEMORY & I/O MAPS

In this appendix, the Memory Map Diagram, as well as the Memory Map and I/O Map tables, are included.

DIAGRAM B-1: Memory Map Diagram

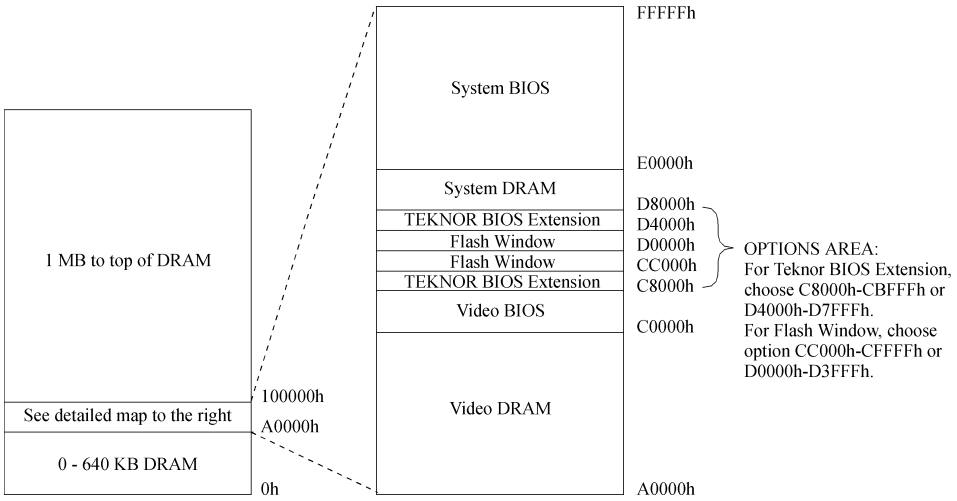


TABLE B-1: Memory Map

ADDRESS	OPTIONAL ADDRESS	FUNCTION
00000-9FFFF		0-640 KB DRAM
A0000-BFFFF		Video DRAM
C0000-C7FFF		Video BIOS
C8000-CBFFF	D4000-D7FFF	TEKNOR BIOS Extension
CC000-CFFFF	D0000-D3FFF	Flash-SRAM Window
D8000-DFFFF		System DRAM
E0000-FFFFF		System BIOS
100000-Top of DRAM		1 MB - Top of DRAM

TABLE B-2: I/O Map

ADDRESS	OPTIONAL ADDRESS	OPTIONAL ADDRESS	OPTIONAL ADDRESS	FUNCTION
000-00F				DMA Controller 1
020-03F				Interrupt Controller 1
040-043				Timer
060-064				Keyboard (8742)
070-071				Real-time clock, NMI mask
080-09F				DMA Page Register
0A0-0BF				Interrupt Controller 2
0C0-0DF				DMA Controller 2
190-193	290-293	390-393		TEKNOR Control Port
0F0-0FF				Math Coprocessor/ Configuration Registers
1F0-1F7, 3F6, 3F7	170-177, 376, 377			IDE Hard Disk
3F0-3F7	370-377			Floppy Disk
378-37A	3BC-3BE	278-27A		Parallel Port (LPT1 by default)
3F8-3FF (COM1)	2F8-2FF (COM2)	3E8-3EF (COM3)	2E8-2EF (COM4)	UART1 (COM1 by default)
2F8-2FF (COM2)	3F8-3FF (COM1)	3E8-3EF (COM3)	2E8-2EF (COM4)	UART2 (COM2 by default)
3C0-3CF, 3D0-3DF, 3B0-3BB				Graphics Controller

C TEK932 BOARD DIAGRAMS

Four diagrams are included in this appendix:

DIAGRAM C-1: TEK932 Assembly

DIAGRAM C-2: TEK932 Configuration

DIAGRAM C-3: TEK932 Mechanical Specifications

DIAGRAM C-4: TEK932 Block Diagram

DIAGRAM C-1: TEK932 Assembly

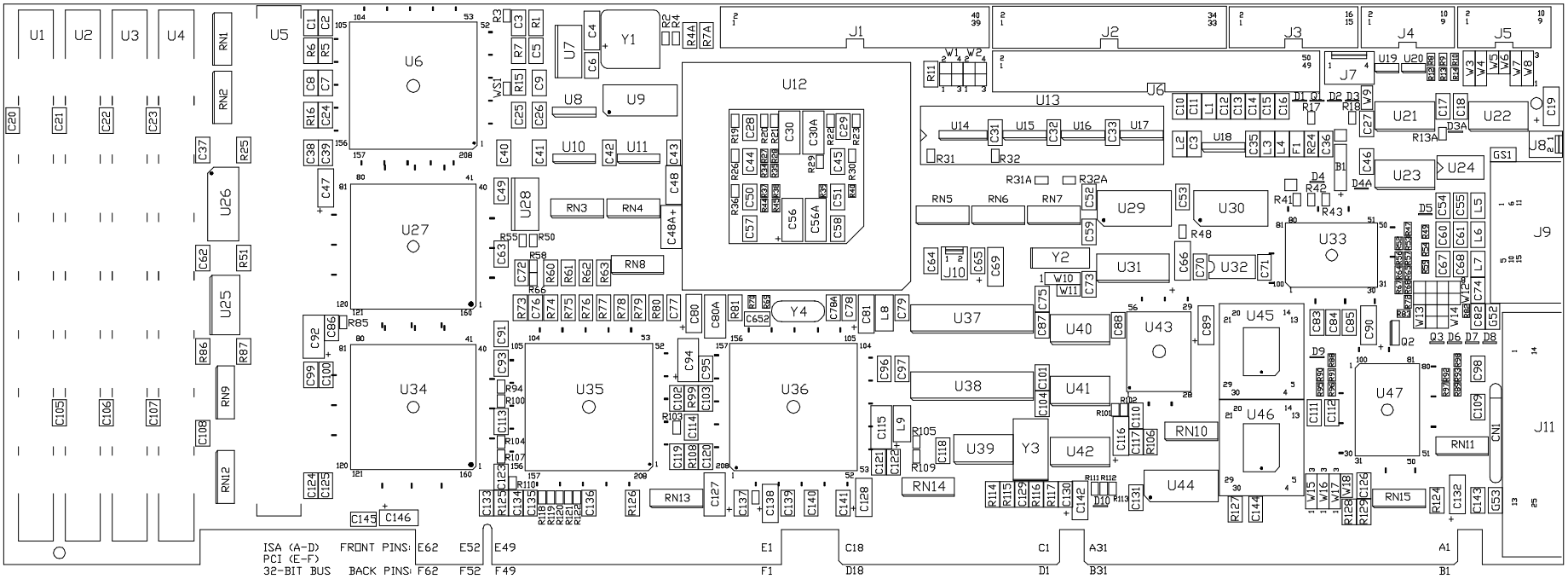


DIAGRAM C-2: TEK932 Configuration

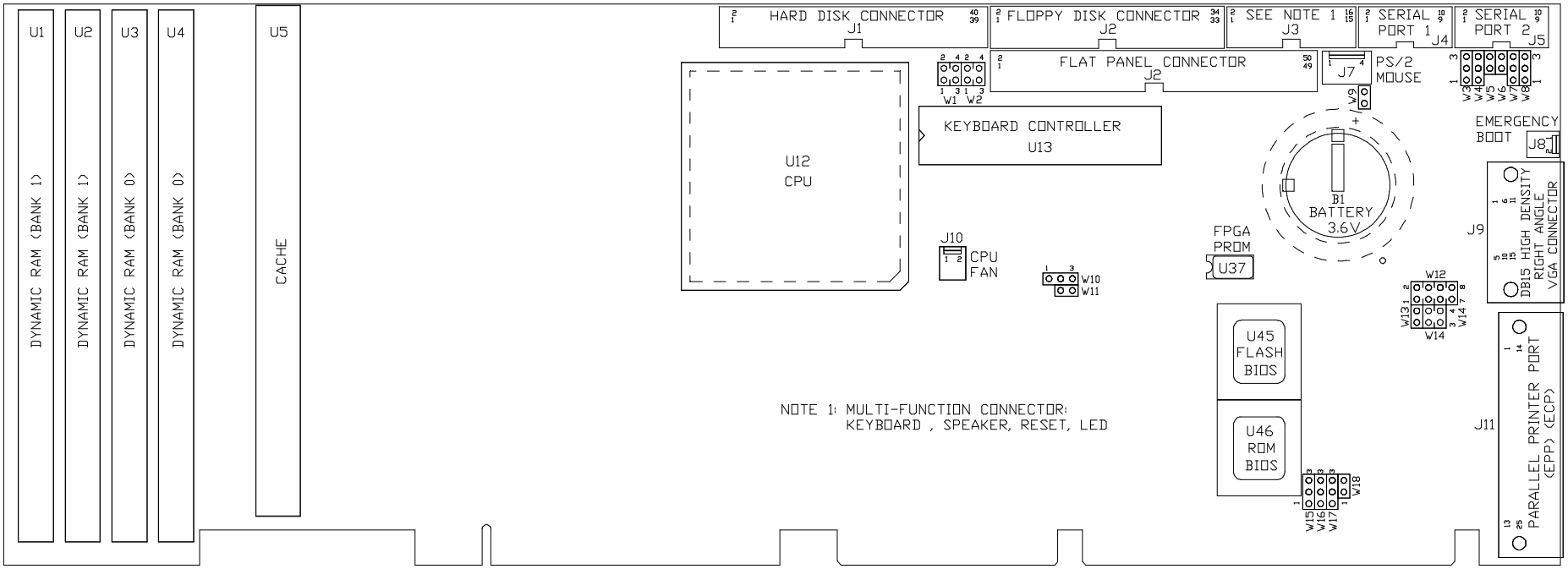


DIAGRAM C-3: TEK932 Mechanical Specifications

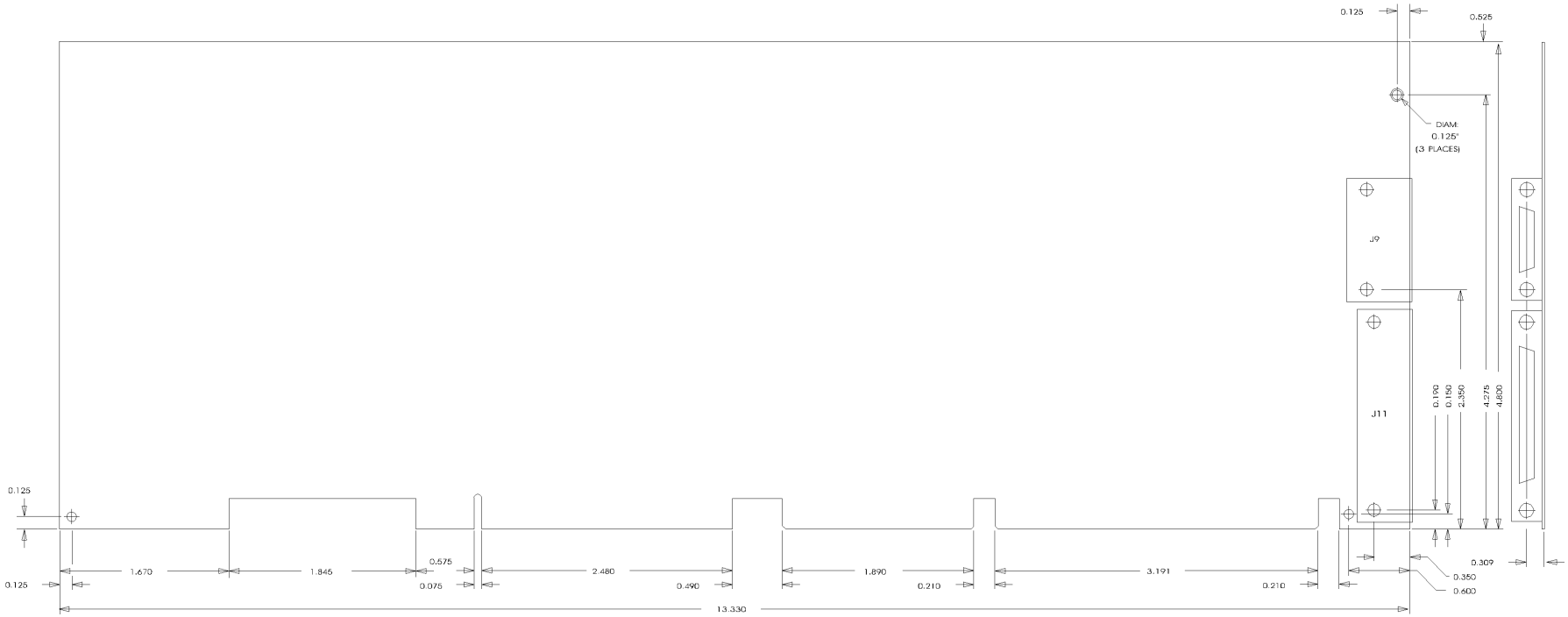
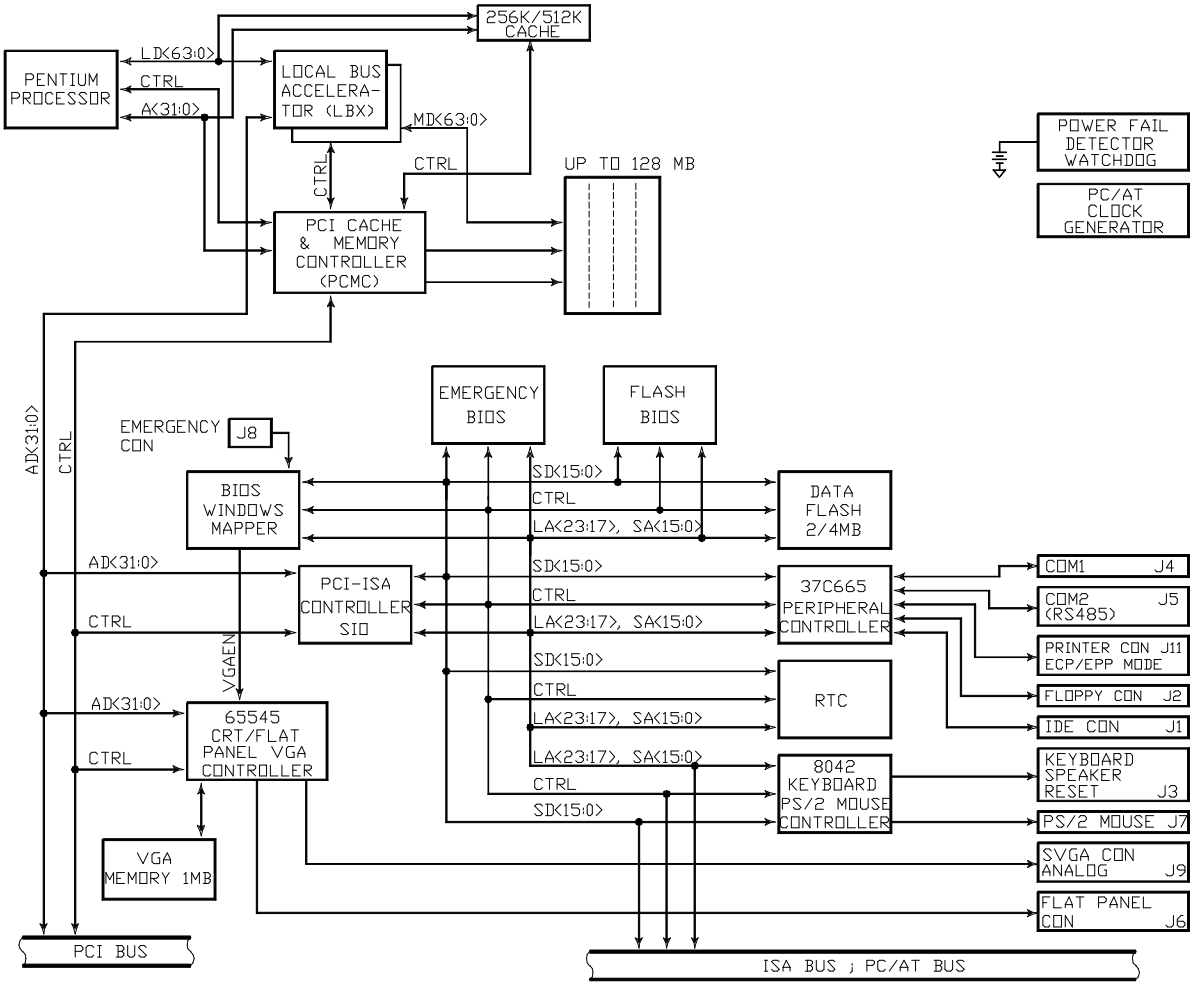


DIAGRAM C-4: TEK932 Block Diagram



D RECOMMENDED DEVICES & MATING CONNECTORS

The following is a list of recommended devices and connectors for use on the TEK932. Many other models are available and function equally well. Users are encouraged to check with their local distributors for comparable substitutes.

DRAM (U1, U2, U3 and U4)

DRAM devices with page mode at 70 ns maximum access time is recommended. For example:

MICRON	MT10D25636M-7	(256K*36)
NEC	MC-42255A36B-70	(256K*36)
SAMSUNG	KMM536256C-7	(256K*36)
TOSHIBA	THM362500AS-70	(256K*36)
MICRON	MT18D51236M-7	(512K*36)
MICRON	MT9D136M-7	(1M*36)
NEC	MC-421000A36B-70	(1M*36)
SAMSUNG	KMM5361000B-7	(1M*36)
TI	TM124MBK36R-70	(1M*36)
TOSHIBA	THM361020AS-70	(1M*36)
HITACHI	HB56D236B2-7C	(2M*36)
HITACHI	HB56D236BS-7BC	(2M*36)
HITACHI	HB56D236BW-7B	(2M*36)
HITACHI	HB56D236BW-7C	(2M*36)
MICRON	MT18D236M-7	(2M*36)
NEC	MC422000A36B-70	(2M*36)
SAMSUNG	KMM5362000B-7	(2M*36)
TOSHIBA	THM362040AS-60	(2M*36)
TOSHIBA	THM362040AS-70	(2M*36)
MITSUBISHI	MH4M36ANXJ-7	(4M*36)
NEC	MC-424000A36BH-70	(4M*36)
NEC	MC-424000A36BJ-70	(4M*36)
SAMSUNG	KMM5364100-7	(4M*36)

TOSHIBA	THM364020S-70	(4M*36)
HITACHI	HB56D836BR-70A	(8M*36)
TOSHIBA	THM368020S-70	(8M*36)
TOSHIBA	THM368020SG-70	(8M*36)

INTERFACE CONNECTORS

The following connectors are recommended for interfacing with the I/O devices. The parts shown here do not have a strain relief but one may be added.

Connector	Recommended Mating Part
Hard Disk (J1)	Amp 746286-9 (499252-1*) Robinson Nugent IDS-C40PK-TG Thomas & Betts 609-1041 (40-pin flat cable connector)
Floppy Disk (J2)	Amp 746286-8 (499252-6*) Robinson Nugent IDS-C34PK-TG Thomas & Betts 609-3441 (34-pin flat cable connector)
Keyboard (J3)	Amp 746286-3 (499252-8*) Robinson Nugent IDS-C16PK-TG Thomas & Betts 609-1641 (16-pin flat cable connector)
Serial Port 1 & 2 (J4 & J5)	Amp 746286-1 (499252-5*) Robinson Nugent IDS-C10PK-TG Thomas & Betts 609-1041 (10-pin flat cable connector)
PS/2 Connector (J7)	Amp 22-01-3047 (connector) Amp 08-50-0114 (crimps)

* optional Amp strain relief part number shown in brackets

Connector	Recommended Mating Part
Fan Connector (J10)	Leoco 2530 S020013 (housing) Leoco 2533 TCB00A0 (pins)
Parallel Port (J11)	Amp 747321-2 (747275-2*) Amphenol 841-17-DBFR-B25P Robinson Nugent IDD-C25PM-440-TG30 Thomas & Betts 609-25P (25-pin flat cable connector)

* optional Amp strain relief part number shown in brackets