S895

SYSTEM BOARD

Version 1 .O

USER'S MANUAL

S895
SYSTEM
BOARD

Ver 1.0

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INTRODUCTION

Congratulations on your purchase of the S895 system board. The S895 is a next generation motherboard supporting Level 1 processor Write-Back Cache and the Intel SL enhanced "power saving" interface. The S895 supports all standard 5V 486 CPUs as well as newer 3.45V CPUs (Intel DX4, P24cT). Built in "Green" power saving features allow the system to conserve energy during periods of inactivity. The following lists gives an overview the S895 features:

* Supports CPU with Level 1 Write-Back Cache:
  Pentium Overdrive Processor and the Write-Back Enhanced Intel DX2 processor.

* supports 3.45v CPU: Intel DX4, Pentium Overdrive Processor (P24cT)

* supports 5v CPU: 486DX2,486DX, 486SX.
  Pentium Overdrive Processor (P24T)

* Power saving "Green" features: BIOS and hardware support
  - Intel System Management Mode supported.
  - Stopclock supported.
  - Intel SL Enhanced Interface

* Onboard adjustable Voltage Regulator to derive 3.45V from 5V power.

* Integrated Cache controller:
  16Kbytes of cache memory (IntelDX4)
  8 Kbytes of cache memory (486SX, 486DX and 486DX2)
  16Kbyte code and data caches (Pentium Overdrive Processor)

* Burst Mode Write-Back Cache Controller

* Secondary Cache from 0 to 256KB using SRAM (32 Kb x 8)

* DRAM controller supports both Single Density and Double density SIMM modules using 72 pin SIMM modules in 4 SIMM sockets.

* Supports up to 128 MB of memory on board (using 256 Kb x 32/36,1Mb x 32/36,2 Mb x 32/36,4 Mb x 32/36,8 Mb x 32/36,16 Mb x 32/36 SIMM)

* AWARD BIOS

* OPTi 82C895 and OPTi 82C602 surface-mounted chipset

* Three 16 bit ISA expansion slots

* Three 32-bit VESA Local Bus Slots (includes three 16-bit ISA)

* Speed switched by both hardware and software.

* Real Time Clock integrated in 82C602, comes with 3.0V Lithium Cell Backup.

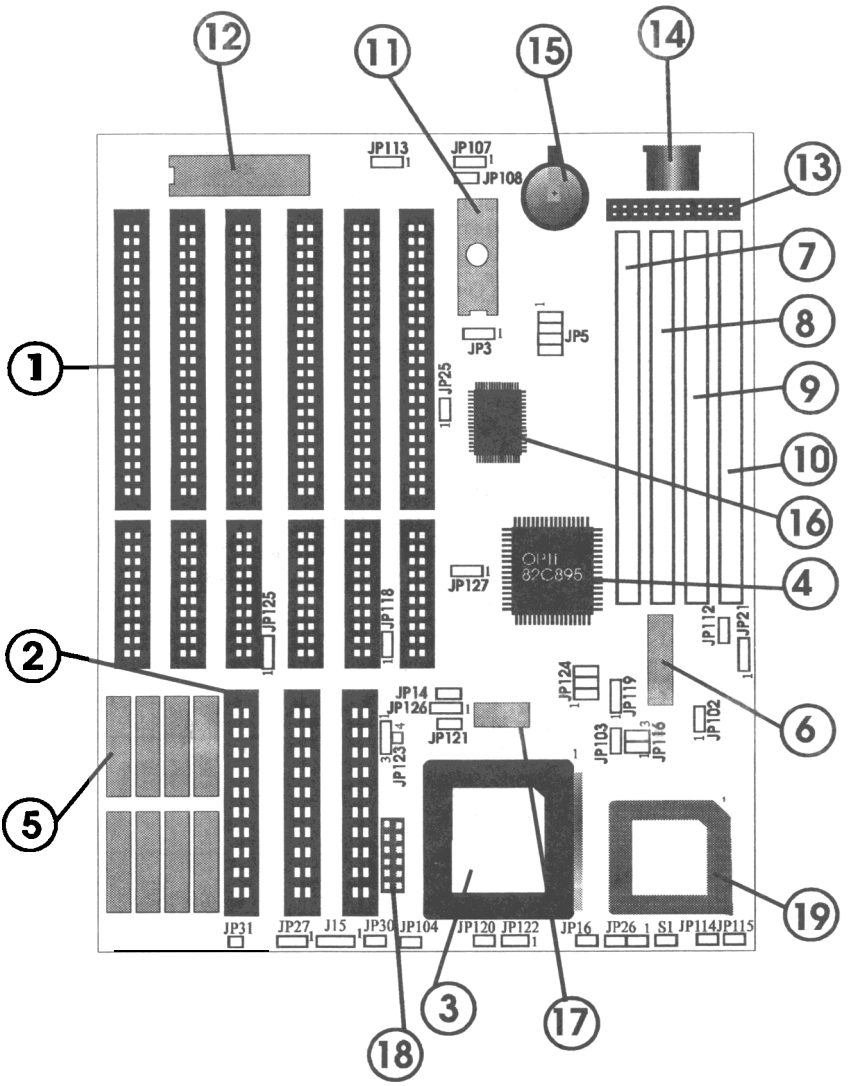
* Onboard Clock Generator facilitates CPU upgrades. Simply change jumpers to change CPU speed (no oscillators required).

A) Board Layout & Jumpers

This section provides an indication of the location of main system board components as well as a list of the jumpers on the motherboard.

Number	Item
1	16-bit ISA Slots
2	32-bit VESA Slots
3	486 / Overdrive ZIF Socket
4	OPTi 82C895 Chip
5	SRAM Memory
6	TAG/DIRTY SRAM
7	SIMM Memory Socket 0
8	SIMM Memory Socket 1
9	SIMM Memory Socket 2
10	SIMM Memory Socket 3
11	BIOS EPROM
12	Keyboard Controller
13	Power Connector
14	Keyboard Connector
15	Battery
16	OPTi 82C602 Chip
17	Clock Generator
18	PAL Socket for Second VL Master Option.
19	PQFP CPU

Board Layout



Jumpers

The following list is an overview of the system jumpers. More details on certain settings can be found in later sections. Please be aware that depending on the particular configuration of the motherboard that you have purchased, some jumpers may NOT be available.

POSITION		COMMENTS
JP3	1-2	Flash Programming Enabled
	2-3	Flash Programming Disabled
JP5	1-2	Always ON
JP14		For Level 1 Write Back CPU ON = P24T, P24D Write Back Level 1 OFF = Write Through CPU (Default)
JP16		Pentium Overdrive Level 1 ON = Burst Write OFF = Disable Blen#
JP21	2-3	Always ON
JP25	2-3	On - for Intel SL CPU (STPCLK#)
JP26	1-2,3-4	486DX, 486DX2/66, P24T, Intel DX4
	2-3	486SX
JP107	1-2	+12V Programming Voltage
	2-3	+5V Programming Voltage
JP108	ON	1Mbit Flash with 512Kbit file at 00000
	OFF	1Mbit Flash with 512Kbit file at 10000
JP112		Always OFF
JP116	1-2,3-4	For PPEN & SMIACT (Intel SL enhanced)
	OFF	For CPU which are NOT Intel SL-enhanced
JP119	1-2	Intel/AMD CPU
	2-3	Cyrix M7
JP120	ON	Cyrix 2x
	OFF	All Other CPU
JP125	1-2	128KB Cache
	2-3	256KB Cache
JP126	1-2	128KB Cache
	2-3	256KB Cache
JP127		2-3 = Always

S1	Reset Connector
J15	Keylock Connector
JP115	Turbo LED Connector
JP27	Speaker connector
JP114	Turbo Switch Connector
JP118	Fan Header

B) Level 1 Write-Back Support

The S895 supports Level 1 Write-Back CPU. Most standard 486DX/DX2 processors support Level 1 Write-Through Cache only. Level 1 refers to the cache internal to the CPU and not the secondary (level 2) cache which is available on the motherboard. Performance gains will vary depending upon the processor and the amount of level 2 cache. Processors such as the Pentium Overdrive Processor and the Write-Back Enhanced Intel DX2 processor support Level 1 Write Back. Most CPU support Level 1 Write through only.

C) POWER SAVING

The S895 is environmentally friendly. The S895 is a second generation "power saving" systemboard. The "green" functionality is built in to the chipset to support the Intel SL enhanced interface (STPCLK , SMI#). The Intel System Memory Management Mode is fully supported as well as the Stopclk interface to statically stop the internal clock of the CPU. Note that power saving on the S895 ver2.0 is only valid for Intel SL enhanced CPU such as the current IntelDX4,486DX2, etc or CPU that support the Intel SL enhanced interface.

After an extended period of inactivity, the S895 systemboard will power down in several stages to conserve energy. When the first timer expires, (after the preset period of time with no hard disk access) the hard drive is powered down. If the system is truly idle, the second timer will expire and the STPCLK interface will be used to statically control the CPU clock. Finally when maximum power saving mode is entered the screen is blanked. System Memory Management Mode allows programs to dynamically interface to the power saving hardware.

The amount of power savings will depend on the configuration of the system. Base configurations will easily meet the EPA requirements for a "Green PC", (less than 30Watts of power consumption when idling).

All timers can be set via the system BIOS . Also the system can be configured to selectively monitor different types of system activity (various Interrupt Requests, etc) for further "green" customization. Consult the section on BIOS. We recommend that you experiment with the power saving features and become aware of their effects on your system. You will find that it operates much like a screen saver. The power saving can also be totally disabled via the system BIOS.

For smoother operation of the power saving features, your should configure your software:

* In a MS-DOS environment, install power.exe for more flexibility.

* In a Windows environment, install “MS-DOS System with APM” through the windows Setup utility. This will install an APM icon in Windows. Set this option to advanced for better system response.

To exit power saving, press the “Shift” key or move the mouse (if installed). Pressing a key or moving the mouse will restore the system, however, the hard drive will not spin back up until it is accessed. You will probably have to wait several seconds as the hard drive spins up before it can be accessed. Once the hard drive spins up, full operation is restored and all timers are reset to their initial values.

D) CPU Installation / Upgrade

The Central Processing Unit (CPU) is the brain of a computer. The CPU interprets and executes instructions and thereby controls the computer system. In micro-computers, the CPU is designed as a highly integrated chip called the micro-processor. The S895 incorporates only the best in micro-processor speed and technology. The following are CPUs and speeds available for the S895.

PENTIUM OVERDRIVE PROCESSOR - The S895 supports Intel overdrive Processor technology, with the 5V P24T or the 3.3V P24cT CPUs. These processors use Pentium technology and include separate 16 KB code and data caches. Internally they may be clock doubled or tripled. A 237 pin ZIF socket is included to house these processors.

IntelDX4 CPU - To the standard 486 core, several special features have been added. This CPU is clock tripled, requires a voltage of 3.3V, and has 16KB of internal cache. Available speeds of 75MHz and 100MHz internal are supported.

The Write-Back Enhanced Intel DX2 processor - This CPU is similar to the popular 486DX2 described below except that it supports the added feature of Level 1 Write-Back.

486DX2 CPUs - Otherwise identical to the 486DX CPU, it includes speed doubling technology which allows the CPU to run twice as fast as the system bus. Available internal speeds of 50MHz and 66MHz are supported.

486DX CPU - The standard 486DX CPU, it requires a voltage of 5V supports an integrated paged memory management, floating point co-processor, and 8 KB internal cache. Internal/external speeds of 25,33,40, and 50 MHz are supported.

486SX CPU - The 486SX CPU is identical to the 486DX except that it lacks an integrated floating point co-processor. Internal/external speeds of 25 and 33 MHz are supported.

For installation of a new CPU, or upgrade of an existing CPU, observe the following procedure **(ALWAYS** use a CSA approved grounding strap or other anti-static device):

1) Turn off and unplug the system.

2) Upgrading an existing CPU is easy with the ZIF (Zero Insertion Force) socket. Open the ZIF socket by moving the handle to the upright position, the old CPU is now free. Lift it straight out of the socket.

3) Align the new CPU with the socket (be sure all the pins on the CPU are aligned with the holes). One corner of the CPU is notched and marked with a round dot and you should align it with the pin one mark (white triangle on the board or missing pins on the socket).
Note: 486Dx/DXZ/SX *have fewer pins than the socket, leave the outside rows of pins empty.*

4) With the ZIF socket handle in the upright position set the CPU straight into the socket, it should drop in easily requiring no force. Make sure that all pins are fully inserted in the appropriate holes. Gently hold the CPU in place and push the handle to the closed position.

5) Change the appropriate jumpers to set the CPU type.

Jumper	5V CPU (486SX/486DX/486DX2)	3.45V CPU (IntelDX4)
JP101	ON	OFF
JP102	ON	OFF
JP103	ON	OFF
JP104	ON	OFF

6) The S895 uses a clock generator to produce the system clock. Simplifying processor upgrades. Set the jumpers to select the appropriate frequency, as outlined in the table on the following page. For a 486DXKX CPU set the frequency the same as the labeled CPU speed (e.g. select 50MHz for 486DX-50 CPU). For the 486DX2 CPU set the frequency to half the labeled CPU speed (e.g. select 33MHz for a 486DX2-66 CPU).

Jumper JP124	Frequency (MHz)			
	25	33.3	40	50
1-2	ON	ON	OFF	OFF
3-4	OFF	ON	OFF	ON
5-6	ON	OFF	ON	OFF

7) For an Intel DX4 the following jumper should also be set.

JP123	Intel DX4 Internal speed select
2-3	2X (double of external speed)
l-2	2.5X
OFF	3X (triple of external speed)
2-4	Cyrix (HITM)

8) If installing a VESA local bus card, set the jumpers for the appropriate external CPU clock speed according to the chart below,

Jumper	Position	CPU Maximum Clock Speed
JP31	OFF	OWS for VL
	ON	1 WS for VL
JP30	OFF	< 25MHz
	ON	>=33MHz

E) Cache Installation / Upgrade

CACHE MEMORY - In addition to the CPU internal cache, the S895 system board supports an optional, user-upgradeable. secondary cache of 0 KB, 128 KB, or 256 KB. The increased speeds of microprocessors during the last few years have outpaced the development of DRAMS (DRAMS are used for system memory). Cache memory utilizes SRAM which is much faster than the DRAM used for system memory. Cache memory provides fast local storage for frequently accessed codes and data. Cache memory (SRAM) is used in tandem with main memory (DRAM) to enhance motherboard performance. Frequently used codes and data are transferred from main memory and placed in cache memory (SRAM) thus allowing the system to function at a much higher rate of performance. System performance is improved by reducing bus cycles and increasing instruction throughput. The actual realized performance increase will depend on the particular applications used.

The S895 utilizes a Direct Map caching scheme with a Burst Mode Write-Back Cache controller. Direct Map is a common caching scheme whereby a segment of DRAM memory is directly reproduced in cache memory. Write-Back cache architecture is a scheme whereby the system will write modified data to the cache only. Main memory will NOT be updated until the system requires some new data that is NOT available in the cache. Standard Write-Through architecture is penalized during Writes because every time the system writes to cache it must also update the slower main memory. Therefore Write-Back is preferable to Write-Through.

The secondary cache utilizes SRAM (Static Random Access Memory) chips. There are a total of nine sockets for the secondary cache chips. Sockets U39,U41,U43, and U45 comprise bank 0. Sockets U4O,U42,U44, and U46 comprise bank 1. Socket U36

is the shared tag RAM and Dirty RAM. On the S895 systemboard the Tag RAM and Dirty RAM functions are implemented using one chip only.

Tag RAM is used to store the address of the information that is in cache memory. The CPU looks at the tag RAM to see if the memory address for its required information is them. If the address is not found in the tag RAM, then the data is not in cache memory and the CPU must go to system memory for the data.

The Dirty RAM is used as a status indicator for true Write-Back cache. The system will poll the Dirty RAM when it needs to move new data into the cache. If it polls a set or ON status, then it will write the information out of the cache to main memory before loading new data. Otherwise OFF status indicates that the data in main memory is equivalent or just as current as that in cache and the system will directly load the new data that it requires.

For installation of cache memory, observe the following procedure **(ALWAYS** use a CSA approved grounding strap or other anti-static device):

1) Select the size of the cache desired and consult the following table to determine the size and quantity of chips required. The speed required will depend on the speed of the CPU. We recommend using top quality 20ns or faster SRAM for a 486 CPU and 15ns SRAM for the IntelDX4.

SRAM REQUIREMENT

Total Cache	Bank 0	Bank 1	Tag /DirtyRAM
OKB			1,32Kxx
128KB	4,32 Kb x 8		1,32KBx8
256KB	4,32Kbx8	4,32Kbx8	1,32 Kb x 8

2) **Turn off and unplug the system.**

3) Set the appropriate jumpers according to the size of cache to be installed.

Jumper		128KB	256KB
JP125		1-2	2-3
JP126		1-2	2-3

4) Insert the SRAM chips into the appropriate sockets. The notches in the chip must be aligned with the notches in the sockets.

5) Update the BIOS settings using the advanced CMOS setup program. Enable the cache, select the proper Burst rate and SRAM read and write wait states according to the instructions in the BIOS section.

F) Memory Installation / Upgrade

Memory is used to hold information and programs while they are being accessed by the micro-processor. The S895 system board uses DRAM (Dynamic Random Access Memory) memory modules. The system board can support memory from 2MB to 128MB using various combinations of 256 Kb x 32/36 (1 MB), 512 Kb x 32/36 (2 MB), 1 Mb x 32/36 (4 MB), 2 Mb x 32/36 (8 MB), 4 Mb x 32/36 (16 MB), 8 Mb x 32/36 (32 MB), 16 Mb x 32/36 (64 MB) SIMMS.

There are a total of four SIMM sockets on the system board. The DRAM controller supports both single density and double density SIMMs. The socket closest to the expansion slots is Bank 0/1 (Refer to Board Layout). The second socket is Bank2/3. The third socket is Bank 4 and the fourth socket is Bank 5

The following chart describes available memory configurations and the module type and quantity required for each configuration.

Total	Socket 0 Bank 0/1	Socket 1 Bank 2/3	Socket 2 Bank 4	Socket 3 Bank 5
2MB	512 Kb x 32/36			
4MB	512 Kb x 32/36	512 Kb x 32/36		
4MB	1 Mb x 32/36			
6MB	512 Kb x 32/36	512 Kb x 32/36	256 Kb x 32/36	256 Kb x 32/36
6MB	512 Kb x 32/36	1 Mb x 32/36		
8MB	1 Mb x 32/36	1 Mb x 32/36		
8MB	2 Mb x 32/36			
10MB	512 Kb x 32/36	2 Mb x 32/36		
12MB	1 Mb x 32/36	1 Mb x 32/36	1 Mb x 32/36	
12MB	1 Mb x 32/36	2 Mb x 32/36		
12MB	512 Kb x 32/36	512 Kb x 32/36	1 Mb x 32/36	1 Mb x 32/36
14MB	512 Kb x 32/36	1 Mb x 32/36	1 Mb x 32/36	1 Mb x 32/36
16MB	2 Mb x 32/36	2 Mb x 32/36		
16MB	1 Mb x 32/36	1 Mb x 32/36	1 Mb x 32/36	1 Mb x 32/36
16MB	4 Mb x 32/36			
18MB	512 Kb x 32/36	2 Mb x 32/36	1 Mb x 32/36	1 Mb x 32/36
20MB	1 Mb x 32/36	4 Mb x 32/36		
20MB	1 Mb x 32/36	2 Mb x 32/36	1 Mb x 32/36	1 Mb x 32/36
24MB	2 Mb x 32/36	2 Mb x 32/36	1 Mb x 32/36	1 Mb x 32/36
24MB	1 Mb x 32/36	1 Mb x 32/36	4 Mb x 32/36	
32MB	2 Mb x 32/36	2 Mb x 32/36	4 Mb x 32/36	
32MB	8 Mb x 32/36			
32MB	4 Mb x 32/36	4 Mb x 32/36		
36MB	1 Mb x 32/36	4 Mb x 32/36	4 Mb x 32/36	

40MB	1 Mb x 32/36	1 Mb x 32/36	4 Mb x 32/36	4 Mb x 32/36
48MB	4 Mb x 32/36	4 Mb x 32/36	4 Mb x 32/36	
48MB	2 Mb x 32/36	2 Mb x 32/36	4 Mb x 32/36	4 Mb x 32/36
64MB	8 Mb x 32/36	8 Mb x 32/36		
64MB	4 Mb x 32/36	4 Mb x 32/36	4 Mb x 32/36	4 Mb x 32/36
64MB	16 Mb x 32/36			
96MB	8 Mb x 32/36	8 Mb x 32/36	4 Mb x 32/36	4 Mb x 32/36
128MB	16 Mb x 32/36	16 Mb x 32/36		

512Kb x 32/36=2MB
2Mb x 32/36=8MB
8Mb x 32/36=32MB
1Mb x 32/36=4MB
4Mb x 32/36=16MR
16Mb x 32/36=64MB

Use the following chart to select the appropriate DRAM speed (the table refers to row address strobe access times). The wait state setting is set using the advanced CMOS setup program.

CPU	DRAM Write wait states	DRAM Read wait states	Speed
486-25/DX2-50	0	3-2-2-2	70ns
486DX-33	0	3-2-2-2	70ns
486DX2-66	0	4-3-3-3	70ns
486DX-50	1	5-4-4-4	70ns
IntelDX4 33/100	0	4-3-3-3	70ns

SIMM INSTALLATION:
To install a SIMM, observe the following procedure(ALWAYS use a CSA approved grounding strap or other anti-static device):

1) **Turn off and unplug the system.**

2) Align the module with the socket so that pin 1 on the module is toward the keyboard connector and the edge connector is facing the socket.

3) Keep the module at a 70 degree angle to the board and carefully insert the edge connector into the socket. Confirm that the SIMM is evenly seated in the socket.

4) Carefully push the module to a vertical position, until it clips into the locking tabs on the socket assembly. The locking tabs will hold the module firmly in place. Double check that the module is properly installed.
NOTE: Excessive force will damage the SIMM sockets, and void the warranty.

5) To remove a SIMM module, carefully pry the locking tabs away from each end of the module. The module should flip forward and can be lifted out.
NOTE: Excessive force will damage the SIMM sockets, and void the warranty.

The system board will automatically recognize the memory. No jumper changes are necessary but you must save the changes using the advanced CMOS setup program. Simply to acknowledge and save the new configuration.

G) Connectors

After setting the jumpers, installing CPU, cache SRAM, and Memory DRAM, the next step is to install the systemboard in the case and make the proper case connections. There are six connectors on the S895 system board. Refer to the figure on the next page.

Connectors		Pin	Description
Reset	S1	1	**Ground**
		2	Reset in
Power LED / Keylock	J15	1	+5v
		2	NC
		3	Ground
		4	Keylock
		5	Ground
Turbo LED	JP 115	1	LED power
		2	LED ground
Speaker	JP27	1	Dam out
		2	NC
		3	Ground
		4	+5v
Turbo Switch	JP114	1	Ground
		2	Turbo
Power Connectors	J7/J8	1	Power good
		2	+5v
		3	+12v
		4	-12v
		5	Ground
		6	Ground
		7	Ground
		8	Ground
		9	+5v
		10	-5v
		11	+5v
		12	+5v

Keyboard Connectors . . ..Jl	1	Keyboard clock
	2	Keyboard data
	3	NC
	4	Ground
	5	KBD power

NOTES:

i) The hardware turbo switch is used to change the speed of the system. Engaging the turbo switch will cause a speed change from low to high speed. The speed can also be software switched using key sequence: CTRL ALT +/- or CTRL ALT SHIFT +/-. Always remember that down-turbo with one sequence can only be changed via the same type of sequence but using "+" instead of "-".

ii) It is imperative that the power connectors be secured in the proper configuration. Failure to do so could cause damage to the board at power up.

H) OTHER FEATURES:

LOCAL BUS DEVICE - S895 has three 32-bit VESA Local Bus slots (includes 3 16bit ISA slots), three additional 16-bit ISA slots. The ISA bus offers an 8 or 16-bit data path and is normally run at 8 MHz. The Local Bus provides full 32-bit data path and operates at the same speed as the system speed. Local Bus peripheral devices can be bus-master or bus-slave. Local bus offers a significant performance advantage over the standard 8/16-bit ISA Bus.
Note that many local bus peripherals run at a maximum of 33MHz.

CHIPSET - For optimal control in interfacing or processing, the S895 system board features the 82C895 chipset for OPTi Inc. Highly integrated, this chipset minimizes the clutter and maximizes the integrity of the S895 system board. Featuring only a single surface-mounted ASIC apart from the OPTi 82C602:

The 82C895 controls the following functions:

- CPU selection
- Reset and shutdown logic
- Clock Generation and Selection Logic
- Burst Mode Control
- Non-Cacheable Memory Regions control
- DMA and Master Cycle control
- Data Bus conversion
- ISA Bus Conversion and Arbitration Logic
- Local Bus Arbitration Logic
- Interrupt and DMA interfacing
- CMOS information storage
- Cache Control
- Page Mode DRAM Controller

I) BIOS Setup

After the board has been properly upgraded, configured, and connected and all peripherals have been installed (I/O controller, VGA card, floppy drives, hard drives etc.), then it is time to power up.
At power up, press DEL if you want to run setup utility.
After hitting the "DEL" key, the BIOS setup program main menu will be displayed.
Choose the following options:

1) Standard CMOS Setup

Choose the "Standard CMOS Setup" option from the main menu. Hit "Return" key to clear the warning screen. Use the "Page Up" and "Page Down" and arrow keys to move around and make modifications to the information. The available options for configuration are:

a) Set the Time and Date

b) Set the hard disk parameters
- If you have no hard disk, choose NONE.
- If you have one hard disk, configure Hard Disk C: for the correct type of the drive that you are using.
- If you have two hard disks, both Hard Disk C: and D: must be configured.

Consult your dealer/supplier for the hard disk(s) type(s) or parameter(s).

c) Choose your floppy drive(s):
The available options are: 36OKB, 1.2KB, 720KB, 1.44KB, 2.88KB, and not installed.

d) Set the display type:
VGA/PGA/EGA, Color80X25, Monochrome, and not installed.

e) Set the error type:
Set this to ALL ERRORS

After you have selected the necessary options for your particular configuration, hit 'ESC' key to return to the main menu.

The information in the following two sections are to fine tune the system board's performance. Most of the options will be standard across all possible motherboard configurations.

2) BIOS Feature Setup

ROM ISA BIOS (2C4UK000)
BIOS FEATURES SETUP
AWARD SOFTWARE. INC.

Virus Waming	Disabled	System BIOS Shadow	Enabled
CPU Internal Cache	Enabled	Video BIOS Shadow	Enabled
External Cache	Enabled	C8000-CBFFF Shadow	Disabled
Quick Power On Self Test	Disabled	C000-CFFFF Shadow	Disabled
Boot Sequence	A,C	D0000-D3FFF Shadow	Disabled
swap Floppy Drive	Disabled	D4000-D7FFF Shadow	Disabled
Boot Up Numlock Status	On	D800-DBFFF Shadow	Disabled
Boot Up System Speed	High	DC000-DFFFF Shadow	Disabled
IDE HDD Block Mode	Disabled	E0000-E3FFF Shadow	Disabled
Gate A20 Option	Fast	E4000-E7FFF Shadow	Disabled
Memory Parity Check	Disable	E8000-EBFFF Shadow	Disabled
Typematic Rate Setting	Disabled	ECOOO-EFFFF Shadow	Disabled
Typematic Rate (Chars&x)	6		
Typematic Delay (T&x)	250		
Security Option	Setup		

ESC	: Quit	↑↓→←	Select Item
Fl	Help	PU/PD/+/-	: Modify
F5	: Old Value	(Shift)F2	: Color-
F6	Load BIOS Defaults		
F7	Load Setup Defaults		

Virus Warning: This can be enabled to assist in the detection of computer virus which may be hazardous to your data. Default is disabled.

CPU Internal Cache: This refers to enabling and disabling the cache which is internal to the processor. For faster performance, this should always be enabled.

External Cache: External cache enabling refers to the secondary cache which was installed on the system board. Default is enable unless there is no cache on the systemboard.

Quick power on self Test: The power on self-test does several system diagnostics including testing the system DRAM. For faster boot up, this should be enabled.

Boot Sequence: Here, you can set the boot sequence of which drive to check first. eg A,C means check the floppy drive A: for a bootable disk and if no disk found then boot from drive C:

Swap floppy drive: Allows you to exchange the floppy designators.

Boot up numlock status: If enabled causes the numeric keypad to be active rather than the cursor control functions.

Boot up system speed: set to high for fastest speed

IDE HDD block mode: disabled is default.

Gate A20 option: This is refers to control of the A20 handler line that allows access to the protected mode memory area Default is Fast.

Memority parity check: Set to disabled for x32 SIMM. (default)
Set to enabled or disabled for x36 SIMM

Typematic Features: These control the rate at which information entered via the keyboard is accepted by the system:
Recommend:
Typematic Rate Setting: Disabled
Typematic Rate (Chars&~): 6
Typematic Delay (Msec): 250

Security Option: This is for configuring the password access. Set to setup it will allow you to password protect the CMOS BIOS settings. Set to system it will allow you to password protect the entire system.

Shadow RAM Setup: Programs that reside in ROM (Read-Only-Memory) can be sped up if they are copied to faster main memory and then executed from this location. This technique is called shadowing and is usually used for System BIOS and VGA adapters. **System** and **Video** BIOS should always he shadowed. Certain adapter ROMs can be shadowed but this will require experimentation when the adapter is installed.

3) **Chipset Feature Setup**

ROM ISA BIOS (2C4UKOOO)
CHIPSET FEATURES SETUP
AWARD SOFTWARE, INC.

Auto Configuration	: Disabled		
AT Clock Option	: CLK/4		
DRAM Read Wait State:	: 3-2-2-2		
DRAM Write Wait State	: ows		
Cache Read Burst	:2-l-l-l		
Cache Write Wait State	: o w s		
Hidden Refresh Option	: Enable		
Slow Refresh Enable	: Disable.		
Single ALE Enable	: Enable		
Extra AT Cycles WS	: Disable		
Fast AT Cycle	: Disable		
Back To Back I/O Delay	: Disable		
Master Mode Byte Swap	: Disable		
System BIOS Cacheable	: Enable	ESC	: Quit ↑↓→← Select Item
Video BIOS Cacheable	: Enable	Fl	: Help PU/PD/+/- : Modify
		F5	: Old Value (Shift)F2 : Color
		F6	: Load BIOS Defaults
		F1	: Load Setup Defaults

Auto Configuration: This is usually set to disabled. When disabled the system can be fine tuned for the particular options installed on the systemboard.

AT Clock Option: This allows selection of the ISA Clock. Please refer to the chart below.

OSCILLATOR SPEED	ATCLK SETTING
25MHz	CLK/3
33MHz	CLK/4
40MHz	CLK/5
50MHZ	CLK/6

DRAM Read Wait State: This will depend on CPU type and speed. Set according to the table on page 15.

DRAM Write Wait State: Refer to page 15.

Cache Read Burst: This refers to the speed at which data can be read from the system secondary cache. In particular it refers to the rate at which a line of information (i.e. 16 bytes) will be read into the CPU from the secondary cache. This setting is CPU, SRAM speed, and SRAM size dependent. In general for 128KB

cache always set to 3-2-2-2. For 256KB cache and CPU speeds 33Mhz and slower set to 2-l-l-l. For 50Mhz set to 3-2-2-2.

Hidden Refresh Option: DRAM must be pulsed periodically in order to retain the information stored in its cells. This method of pulsing the DRAM is called refreshing. Hidden Refresh refers to sneaking in refresh cycles without disturbing the CPU and thereby improving system performance. Default is enabled.

Slow Refresh: Set to disabled.

Single ALE Enable: Default is enabled. ALE is short for Address Latch Enable. This one is particular to certain network adapters.

Extra AT Cycles WS: Allows you to slow down the ISA Bus for peripheral adapters that can NOT meet the normal timing. Default is Disabled.

Fast AT Cycle: This instructs the system to faster timings on the ISA Bus.

Back to Back I/O delay: Default is disabled. Some peripherals may require a delay time to recover from the current cycle before another cycle is started.

Master Mode Byte Swap: Set to disabled.

System BIOS Cacheable: Similar to the concept described earlier as shadowing, however, in this case parts of the ROM code are copied into cache in order to increase performance.

Video BIOS Cacheable: Refer to above. This can usually be enabled for faster access but is highly dependent on the installed video adapter. Some video adapters do NOT function properly when this is enabled. This has no effect unless the ROM has already been shadowed (see Shadow). However, the default is usually enabled.

4) Power Management Setup

ROM ISA BIOS (2C4UKOOO)
POWER MANAGEMENT SETUP
AWARD SOFTWARE, INC.

PM Mode	: SMI GREEN	Sleep Button	: Disable
Power Management	: Disable	LDEV Detection	: Disable
Doze Timer	: Disable	LREQ Detection	: Disable
Sleep Timer	: Disable	Video Detection	: Disable
HDD Standby Timer	: Disable	HDD Detection	: Disable
Sleep Clock	: Slow Clock	FDD Detection	: Disable
CRT Sleep	: Disable	DRQO Dectection	: Disable
PM wait for APM	: Disable	DRQl Dectection	: Disable
IRQ3 Detection	: Disable	DRQ2 Dectection	: Disable
lRQ4 Detection	: Disable	DRQ3 Dectection	: Disable
IRQ5 Detection	: Disable	DRQ4 Dectection	: Disable
IRQ6 Detection	: Disable	DRQ5 Dectection	: Disable
IRQ7 Detection	: Disable	DRQ6 Dectection	: Disable
IRQ8 Detection	: Disable	DRQ7 Dectection	: Disable
IRQ9 Detection	: Disable		
IRQl0 Detection	: Disable	ESC : Quit	↑↓→← Select Item
lRQl1 Detection	: Disable	F1 : Help	PU/PD/+/- : Modify
IRQ12 Detection	: Disable	F5 : Old Value	(Shift)F2 : Color
IRQ14 Detection	: Disable	F6 : Load BIOS Defaults	
IRQl5 Detection	: Disable	F7 : Load Setup Defaults	

As indicated in section lC, the S895 supports the Intel SL enhanced power management interface. Timers can be customized for personal preference. The time corresponds to idle time before system is powered down. If the system senses no activity then the timer will begin to count. If the system timer expires, the system will power down. This section allows a high degree of customization for the power management. The first 8 items turn the power management on. For the S895, Sleep Clock set to SLowClk means disabled. Set to Stopclk enables this option.

The rest of the items vary the sensitivity to system activity. Enabling all the options causes the systemboard to wake up when any kind of activity occurs on the system.

Troubleshooting

This section is intended as a general guide to solve configuration problems and to help pinpoint possible component failures. If after reading this section, an issue still can NOT be resolved, please contact your dealer.

AWARD BIOS performs various diagnostic tests at the time the system is powered up. Whenever an error is encountered during these tests, there will be either a few short beeps or an error message displayed on the monitor. If the error occurs before the display device is initialized, the system reports the error with several short beeps only.

If the error is fatal, the system halts after reporting the Fatal error. If the error is Non-fatal, the process continues after reporting the error.

Suggested courses of action are included in every section. Remember that these suggestions are guidelines only and are based on general experience. Also, ALWAYS power down and unplug the system before attempting any hardware changes.

Errors usually reported by BIOS

The following codes are reported by port 80 debug cards. If the system has a problem, a port 80 card will halt at the current attempted function. This information can be used to debug a problem system. Note that this is not recommended but only provided for reference.

Note: ISA POST coded are typically output to port address 80h.

POST (hex)	Name	Description
C0	Turn Off Chipset Cache	OEM Specific-Cache control
1	Processor Test 1	Processor Status Verification. Tests the following processor status flags carry zero, sign overflow. The BIOS will set each of these flags verify they are set, then turn each flag off and verify it is off.
3	Initialize Chips	Disable NMI, PIE, AIE, UEI, SQWV Disable video, parity checking DMA Reset math coprocessor Clear all page registers CMOS shutdown by byte Initialize timer 0, 1 and2 initialize DMA controllers 0 and 1 initialize interrupt controllers 0 and 1

4	Test Memory Refresh Toggle	RAM must be periodically refreshed in order to keep the memory from decaying. This function assures that the memory refresh function is working properly.
5	Black video. Initialize keyboard	Keyboard controller initialization.
7	Test CMOS Interface and Battery Status	Verifies CMOS is working correctly, detects bad battery.
BE	Chipset Default Initialization	Program chipset registers with power on BIOS defaults.
C!	Memory presence test	OEM Specific-Test to size on-board memory
C5	Early Shadow	OEM Specific-Early Shadow enable for fast boot
C6	Cache presence test	External cache size detection
8	Setup low memory	Early chip set initialization Memory presence test OEM chip set routines Clear low 64K of memory Test first 64K memory
9	Early Cache Initialization	Cyrix CPU initialization Cache initialization
A	Setup Interrupt Vector Table	Initialize first set interrupt vectors with SPURIOUS-INT_HDLR and initialize INT 00h-1fh according to INT_TBL
B	Test CMOS RAM Checksum	Test CMOS RAM checksum, if bad or insert key pressed load defaults
C	Initialize keyboard	Detect type of keyboard controller (optional) Set NUM LOCK status
D	Initialize Video Interface	Detect CPU clock Read CMOS location 14h to find out type of video in use Detect and initialize Video Adapter
E	Test Video Memory	Test video memory, write sign-on message to screen Setup shadow RAM - Enable shadow according to Setup
F	Test DMA Controller 0	BIOS checksum test Keyboard detect and initialization
10	Test DMA Controller	
11	Test DMA Page Registers	Test DMA Page Registers

14	Test Timer Counter 2	Test 8254 Timer 0 Counter 2
15	Test 8259-Mask Bits	Verify 8259 Channel 1 masked interrupts by alternately turning off and on the interrupt lines
16	Test 8259-2 Mask Bits	Verify 8259 Channel 2 masked interrupts by alternately turning off and on the interrupt lines
17	Test Stuck 8259's Interrupt Bits	Turn off interrupts then verify no interrupt mask register is on
18	Test 8259 Interrupt Functionality	Force an interrupt and verify the interrupt occurred
19	Test Stuck NMI Bits (Parity I/O Check	Verify NMI can be cleared
1A		Display CPU clock
20	Enable Slot 0	Initialize slot 0 (System Board)
21-2F	Enable Sits 1-15	Initialize slots 1 through 15
30	Size Base and Extended Memory	Size base memory from 256K to 640K and extended memory above 1MB
31	Test Base and Extended Memory	Test base memory from 256K to 640K and extended memory above 1MB using various patterns
3C	Setup Enabled	
3D	Initialize & Install Mouse	Detect if mouse is present, initialize mouse, install interrupt vectors
3E	Setup Cache Controller	Initialize cache controller.
3F	Chipset Initialization	Program chipset registers with Setup values
40		Display virus protest disable or enable
41	Initialize Floppy Drive & Controller	Initialize floppy disk drive controller and any drives
42	Initialize Hard Drive & Controller	Initialize hard drive controller and nay drives
43	Detect & Initialize Serial/Parallel Ports	Initialize any serial and parallel ports (also game port)
45	Detect & Initialize Math Coprocessor	Initialize math coprocessor
4E	Manufacturing POST Loop or Display Messages	Reboot if Manufacturing POST Loop pin is set. Otherwise display any messages (i.e. any non-fatal errors that were detected during POST) and enter Setup
4F	Security Check	Ask password security (optional)

50	Write CMOS	Write all CMOS values back to RAM and clear screen
51	Pre-boot Enable	Enable parity checker Enable NMI. Enable cache before boot
52	Initialize Option ROMs	Initialize any option ROMs present from C8000h to EFFFFn. Note: When FSCAN option is enabled will initialize from C8000h to F7FFFn
53	Initialize Time Value	Initialize time value in 40h: BIOS area
60	Setup Virus Protect	Setup virus protect according to Setup
61	Set Boot Speed	Set system speed for boot
62	Setup NumLock	Setup Numlock status according to Setup
63	Boot Attempt	Set low stack Boot via INT 19b
B0	Spurious	If interrupt occurs in protected mode
B1	Unclaimed NMI	If unmasked NMI occurs, display Press F1 to disable NMI, F2 reboot
E1-EF	Setup Pages	E1-Page 1, E2-Page 2 etc
FF	Boot	

The preceding list is quite extensive. In most cases, running the setup program and configuring with the proper settings will resolve this issue. However, sometimes further action will be required:

Verify that all components, memory, CPU, cache, BIOS chips, etc. are properly installed and properly seated. If the problem persists, try another VGA adapter and try replacing the memory.

GENERAL DESCRIPTIONS:

CMOS battery state low: indicates failure of CMOS battery or failure in set and checksum tests

CMOS system options not set: indicates failure of CMOS battery, or failure in set and checksum tests.

Suggested Action: check and reconfigure the standard and advanced CMOS setups.

CMOS checksum failure: indicates CMOS battery low or a failure in the set and checksum tests

Suggested Action: Once again, run the BIOS setup program.
After changes, press F10 to save and exit.

CMOS display type mismatch: indicates failure of display verification
Suggested Action: Check jumper for proper display setting and also check the CMOS setup for the proper display setting.

Error in Hard Disk Drive setup
Suggested Action: Run tbe standard CMOS setup and check that the parameters are correct for the installed hard drive(s). Also check all cable connections for proper orientation. Verify that the controller is properly seated in its expansion slot.

C:Drive error: indicates hard disk setup error
Suggested Action: Follow the procedure indicated for HDD controller failure.

C:Drive failure: indicates hard disk or hard disk controller failure.
Suggested Action: Follow the procedure indicated for HDD controller failure. Also try different cables.

OTHER PROBLEMS:

Power Supply Fan Stops Running - Turn off the power immediately and check to see if the system power has shorted to ground.

Power is on and the power supply is running but nothing happens: - check that the power supply is properly connected to the motherboard.

Diskette Error message: Try another diskette and check that the CMOS setting is correct.

Error Reading Fixed Disk: If all cables are properly connected and the CMOS is properly configured, then the indication is that the. hard drive has failed.

NO fixed disk present: This error indicates that the hard drive is improperly connected or configured.

DRIVE NOT READY ERROR
Insert BOOT Diskette in A:
Press any key when ready

The above message indicates the motherboard is unable to find a bootable disk (i.e. the motherboard is unable to load an operating system). Consult your operating system manual.

Non-system disk or disk error

Replace and press any key when ready

The above message indicates that the disk in drive A: is not bootable (i.e. it does NOT possess the operating system files). Consult your operating system manual.

DISKETTE BOOT FAILURE
Insert BOOT diskette in A:
Press any key when ready

The above message indicates that the disk in the drive is defective or not formatted.

Consult your operating system manual.

If problems persist, contact your dealer for technical support.

Glossary

BIOS:(Basic Input Output System) Program usually contained in a ROM chip or flash device on the system board that is the interface between the system hardware and the operating system.
The ROM BIOS is a group of low level programs responsible for interfacing the computer to peripheral devices, such as disk drives, serial and parallel ports, keyboard, and video display. Low-level BIOS routines are common to all operating systems and are generally resident in ROM. Higher-level BIOS routines are specific to the particular operating system in use and are therefore generally stored on disk, and loaded only when the operating system is booted.

BIT:A binary digit that is the most reducible element of computer information. Eight bits make one byte.

BOOT or BOOTSTRAP: A small ROM-based program which is automatically loaded when the system is first powered up (or "booted"), in order to load and execute an operating system or other large program from disk. Also, the process of starting the computer, either by turning on the power, hitting the Reset switch or by pressing the CTRL + ALT + DEL keys simultaneously. The latter is known as a "warm boot".

BYTE: Smallest unit of storage required to hold a character of information in memory or on a disk.

BUS CLOCK: The speed at which data is transferred between the microprocessor and the l/O channel

CMOS: Acronym for Complimentary Metal Oxide Semiconductor. CMOS integrated circuitry uses very little electrical power. Hence CMOS RAM is ideal for storing system configuration information that cannot be stored permanently in ROM.

CONFIG.SYS: A file usually located in the root directory of the boot disk that contains information required to load installable device drivers and other system configuration parameters.

CONVENTIONAL MEMORY: System main memory from 0 to 640KB. Many programs run in this area.

CO-PROCESSOR: An auxiliary processor that reduces micro-processor overhead and increases system speed by executing certain math related functions. ln a 486DX system the math coprocessor is built into the micro-processor.

CPU (CENTRAL PROCESSING UNIT): Also called the micro-processor. The "brain" of the computer, where program instructions and arithmetic operations are executed.
CPU CLOCK: The speed at which the microprocessor executes its instructions.

DOS (DISK OPERATING SYSTEM): Software that controls the activities performed by the computer. DOS sets up an environment under which application software can load and function. It is an interface between the system and application software.

DRAM (DYNAMIC RANDOM ACCESS MEMORY): A type of RAM that requires a refresh cycle to keep information valid. Main system memory uses DRAM.

EXPANSION SLOT: a connector on the system board into which an adapter card can be inserted.

EXTENDED MEMORY: memory beyond the 1MB limit that is accessed by programs such as Windows.

INTERFACE: The connection between the system board and a peripheral.

INTERLEAVING: A technique for improving system performance by speeding up memory access. Successive memory locations are assigned to different memory banks. Then when the system requires the information it accesses both banks in less clock cycles and therefore, the system runs faster.

ISA: Industry Standard Architecture.

JUMPER: A patch cable, wire or other such device used to establish a circuit.

MEMORY: RAM and ROM are devices used to hold information and programs while they are being accessed by the system.

MICROPROCESSOR: Also known as the CPU. The "brain" of the system, which contains the circuitry used for calculation and communication with the rest of the system.

PAGE MODE: Special function in DRAM that saves cycle time by not reloading the Row Address strobe bits.

PARITY BIT: An additional non-informational bit appended to a group of 8 bits to make the number of ones in the group of bits either even or odd. This is an elementary error correction mechanism. Example: During a subsequent read from a memory location, and using odd parity, the system will check the sum of ones. If the sum of ones is NOT

still odd then system knows that the information at that location has been corrupted.

PGA (Pin Grid Array): This refers to CPU**,** and other similar components, that are installed in sockets on the system board. PGA CPU have rows of pins sticking out underneath.

SHADOW RAM: Refers to the technique of copying BIOS routines from slower ROM chips to faster RAM, thereby increasing system performance.

VESA: Video Electronics Standard Association.

VL-BUS: VESA local bus. An architectural, timing, electrical and physical interface that allows high-speed peripheral device to interface, either directly or indirectly, to the local bus of the host CPU. The specification of VL-BUS is available from VESA.

WRITE BACK CACHE: Cache architecture in which wires of new information by the CPU to cache are NOT accompanied by writes to update system memory. The advantage over Write-Through cache is that the system does not have to wait for the slower main memory. However, main memory has not been updated, therefore a penalty will be incurred during read misses. A read miss occurs when the CPU can not find the information it requires in cache memory and must go to system memory for another block of information. However, before trausfer of new information into the cache, the current content of the cache must be saved to system memory or the updated information in the cache will be lost.

WRITE THROUGH CACHE: Cache architecture in which writes by the CPU to system cache are accompanied by writes to update system DRAM memory as well. The penalty is that the system must wait for the slow system memory to receive and store the data. The advantage of this architecture is that during read misses no penalty is incurred as in Write Back cache.