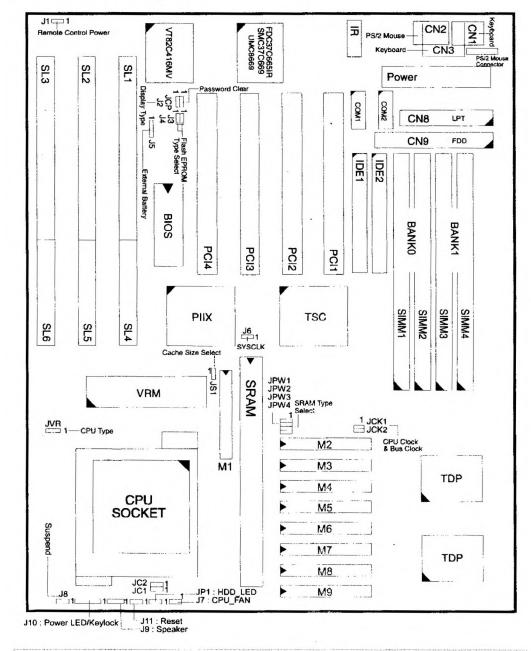
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NOTE : When plugging your processor into the CPU (ZIF) socket, make sure that pin 1 matches that of the CPU socket.

PT-2003

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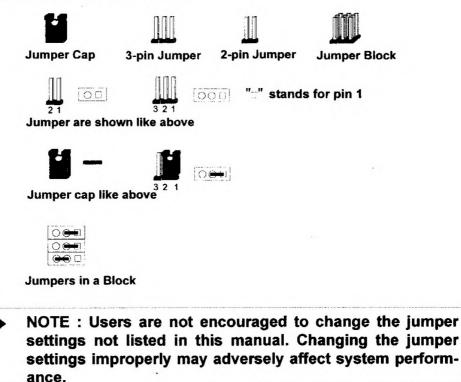
# **Mainboard Settings**

Chapter 2

The PT-2003 has several user-adjustable jumpers on the board that allow you to configure your system to suit your requirements. This chapter contains information on the various jumper settings on your mainboard.

# **Jumpers**

Jumpers are used to select the operation modes for your system. Some jumpers on the board have three metal pins with each pin representing a different function. To "set" a jumper, a black cap containing metal contacts is placed over the jumper pin/s according to the required configuration. A jumper is said to be "shorted" when the black cap has been placed on one or two of its pins. The types of jumpers used in this manual are shown below:

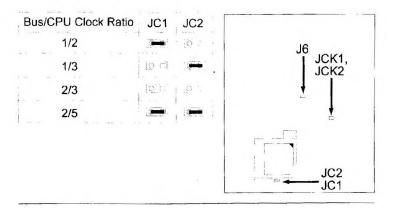


### CPU Speed Select: JCK1, JCK2, J6

The table below shows the jumper settings for the CPU based on its internal clock speed.

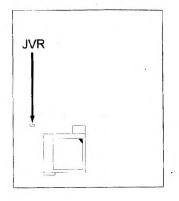
CPU	External		Louis	CPU CI	ock Ra	ite	Bus Clock Rate
Speed	Clock	JCK1	JCK2	Int. Multiple	JC1	JC2	J6
166 MHz	66 MHz	iQ		2.5 x Ext.	- <u>3-6</u> -	()	
150 MHz	60 MHz	() ()	00	2.5 x Ext.	<u></u>	( <b>()</b>	
133 MHz	66 MHz	l <u>o</u> il		2 x Ext.		(G Q)	(3-6 0)
120 MHz	60 MHz	(300)	<u>a</u> cal	2 x Ext.	(general)	<u>c a</u> i	( <del></del>
100 MHz	66 MHz			1.5 x Ext.	0.01	0.0	
90 MHz	60 MHz		10,55	1.5 x Ext.		10.2	i <del>300 ()</del>
75 MHz	50 MHz			1.5 x Ext.	1 <u>0 5</u>	0°0	0.00

### Bus / CPU Clock Ratio: JC1, JC2

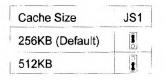


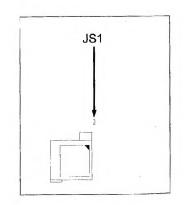
### CPU Voltage Mode Select: JVR

CPU Voltage Mode	JVR
STD / VR (Default) 3.38V	<del></del> 0
VRE 3.5V	0.000

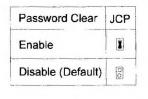


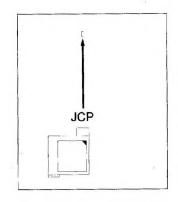
### Cache Size Select: JS1



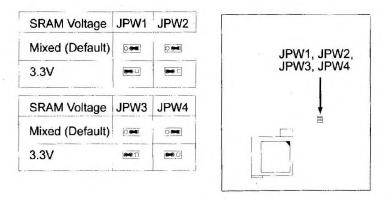


### **Password Clear: JCP**

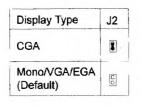


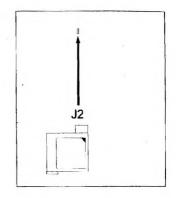


### SRAM Type Select: JPW1, JPW2, JPW3, JPW4

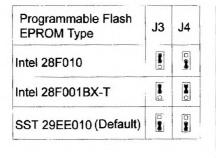


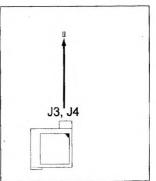
Display Type Select: J2





### Flash EPROM Type: J3, J4

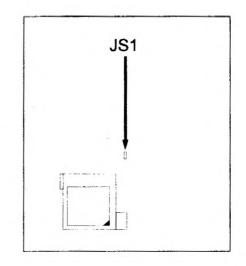






# Cache Size Select: JS1

Cache Size	JS1
256KB (Default)	
512KB	



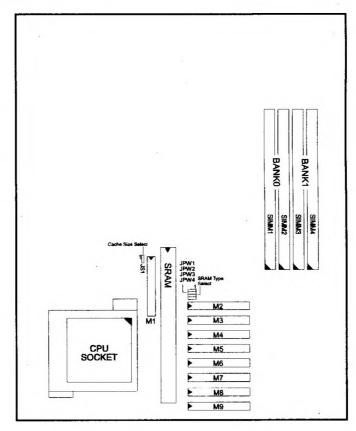
# **System Memory**

Chapter 3

The PT-2003 can be equipped with sufficient memory for running even the most advanced software applications. Memory comes in the form of DRAM (SIMMs) and cache SRAM. This chapter describes these two types of memory and gives instructions on how to install each type on the mainboard.

### **Memory Locations**

The board layout below shows the locations of the DRAM memory banks and the cache SRAM:



### Installing DRAM

### **SIMM Banks**

The PT-2003 can accommodate onboard memory from 8 to 128MB using SIMMs (Single-In-Line Memory Modules). The mainboard has two memory banks — Bank 0 and Bank 1. Each bank has two SIMM sockets which can accept either a 4MB, 8MB, 16MB or 32MB SIMM in each socket.

### **DRAM** Configuration

Memory can be installed in a variety of configurations, as shown in the following table:

TOTAL MEMORY	BANK 0 (72-PIN x 2)	BANK 1 (72-PIN x 2)
8MB	4MB & 4MB	
16MB	8MB & 8MB	
24MB	8MB & 8MB	4MB & 4MB
32MB	8MB & 8MB	8MB & 8MB
40MB	16MB & 16MB	4MB & 4MB
48MB	16MB & 16MB	8MB & 8MB
64MB	16MB & 16MB	16MB & 16MB
041015	32MB & 32MB	
72MB	32MB & 32MB	4MB & 4MB
80MB	32MB & 32MB	8MB & 8MB
96MB	32MB & 32MB	16MB & 16MB
128MB	32MB & 32MB	32MB & 32MB

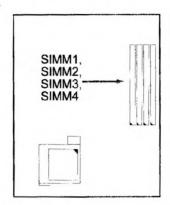
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NOTE : All memory banks use 72-pin memory modules.

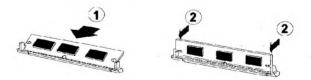
### **Installation Instructions**

NOTE : Always observe static electricity precautions. See "Handling Precautions" at the start of this manual.

1. Locate the SIMM banks on the mainboard.



2. Insert the SIMM edge connector onto the socket.



3. Carefully push the SIMM down and back into the socket until the retaining clips of the socket snap, holding the SIMM in place. The holes in the SIMM should match the pins on the socket's retaining clips.

To remove the SIMM/s, pull the retaining latch on both ends of the socket and reverse the procedure above.

### **Cache Memory**

The PT-2003 can accept either onboard SRAMs or a SRAM module. If the onboard SRAMs are installed, the SRAM module can not be used. On the otherhand, if the SRAM module is implemented, the onboard SRAMs, including tag SRAM, must be pulled out. The onboard SRAMs support asynchronous 3.3V/mixed voltage SRAMs. The SRAM module can support synchronous SRAMs.

NOTE : Use the correct chips for the amount of cache memory you want to add. Install both the correct Cache and Tag SRAM.

#### **Installing Onboard Cache Memory**

NOTE : Always observe static electricity precautions. See "Handling Precautions" at the start of this manual.

If you do not have the confidence to make the installation, you should consult a service technician for assistance.

- 1. Locate the cache memory on the mainboard.
- 2. Be guided by the Cache SRAM settings depending on your desired SRAM configuration.

Correct orientation of the chip is necessary for the cache to operate properly. Normally, the chips have either a curved notch or a dot. This marker on the chip must be matched to the marker on the socket for correct alignment.

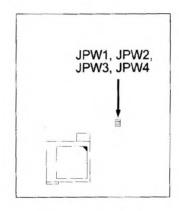
Install the chips individually as follows:

- Align the chip with the marker on the socket. Press the chip onto the socket, ensuring that the pins on the chip are aligned with the corresponding connections on the socket.
- Press the chip completely into the socket so that the pins are properly seated.

#### Using Various Voltage Onboard SRAMs

Cache sockets M2 to M9 can take 3.3V or mix-voltage SRAMs. The jumper settings are listed below.

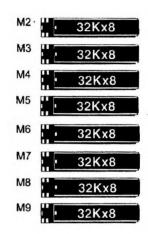
-			
JPW1			
JPW2			
JPW3	OPE		
JPW4	OPE		
	1		
IPIA/1	- C -		
JPW1 JPW2		•	
		•	

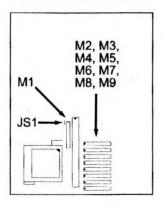


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### **Onboard 256KB Cache SRAM**

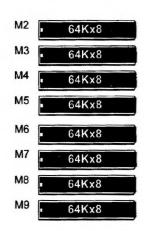


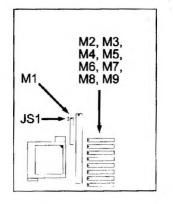












## Installing Cache Memory Module

The PT-2003 allows the installation of either the 256KB or 512KB cache module. The jumper settings of JPW1, JPW2, JPW3, and JPW4 will not affect it.

Locate the slot SRAM on the mainboard, then insert your SRAM module for installation.

