

User's Manual

for 486DX/SX

VL-Bus with Deep Green Main Board

WE SPEED YOUR WORLD

MB 455/456

**80486 VL-BUS MAIN BOARD
with Deep Green PC**

470-024551990

USER'S MANUAL

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Chapter 1

Feature

CPU TYPE :

Intel 486SX,486DX,486DX2,486DX4,
Overdrive P24T,P24D,P24C
and S-series SMM CPU
AMD 486DX,DX2,DXL,DXL2/66
Cyrix M6, M7
UMC 486 CPU

Cache memory : 64KB/128KB/256KB 2nd CACHE
memory selectable Write-back direct mapped
CACHE operation
Supports SRAM type 8Kx8, 32Kx8, 64Kx8

Main Memory : 64MB max on board Using 256K, 1M,
4M and 16M SIMM DRAM
Supports 30pin and 72pin SIM module and auto
- banking of every DRAM banks

I/O Slot : 3 VL-BUS Slots, Seven 16-bit ISA Slots,

BIOS : Award, AMI or other

Dimension : 25 cm x 22 cm

CPU Vcc Input : MB 455 for 5V only
MB 456 supports 5V, 3.45V, 3V
Voltage

Green Function

Supports the EPA Energy Star PC specification with Deep Green system Design. It supports the advanced SMM CPU. Accommodated with Intel S series CPU or AMD DXL, DXL2 CPU, system performs stop clock mode. The function for power saving options are:

. HDD Standby Timer :

The Hard disk entering power down mode.

. Display Power Down :

The display screen will be closed.

. System power down mode :

Full-on : System runs in full speed CPU clock

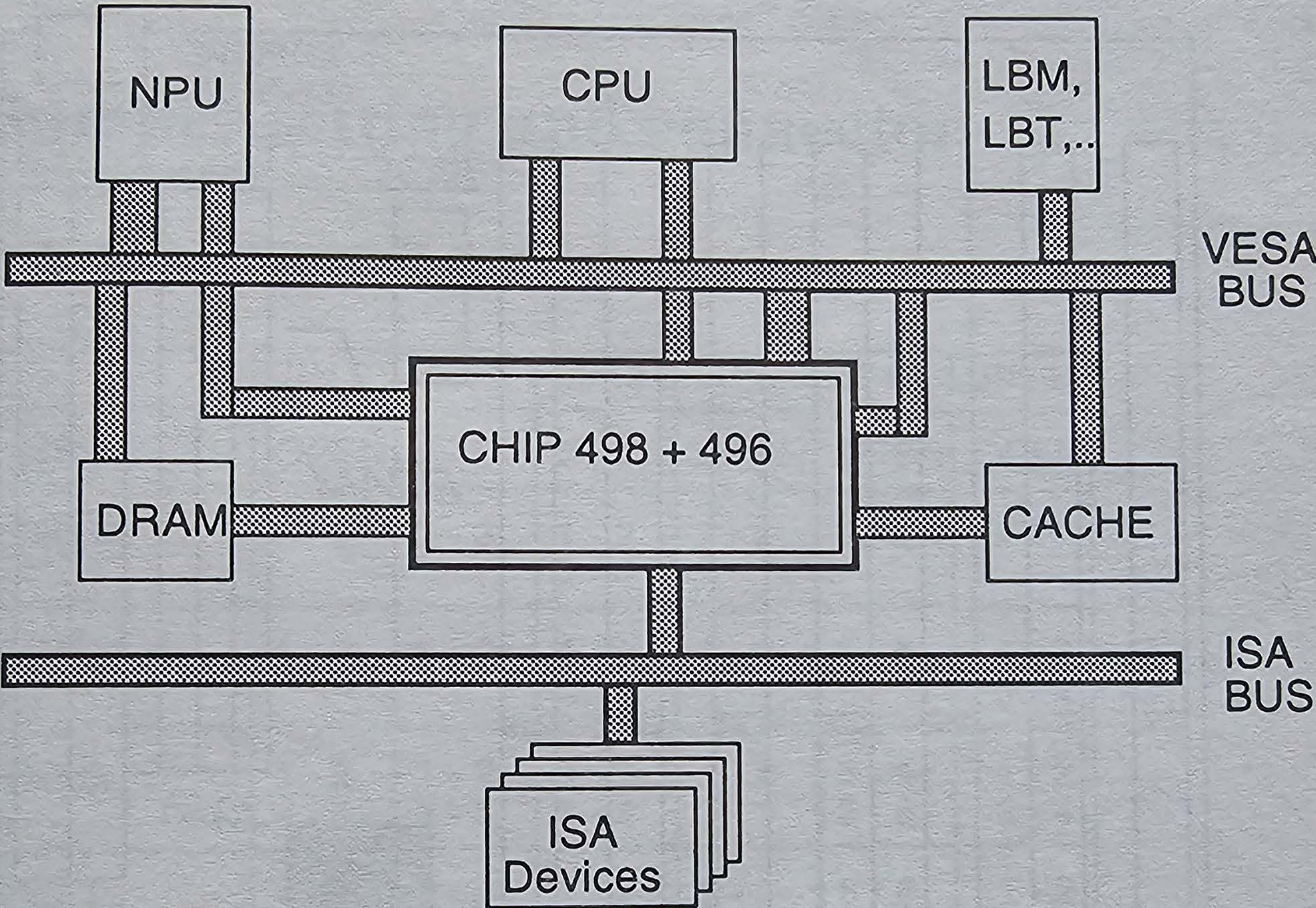
Doze : Sytem runs in lower CPU clock

Standby : System scales-down the CPU clock

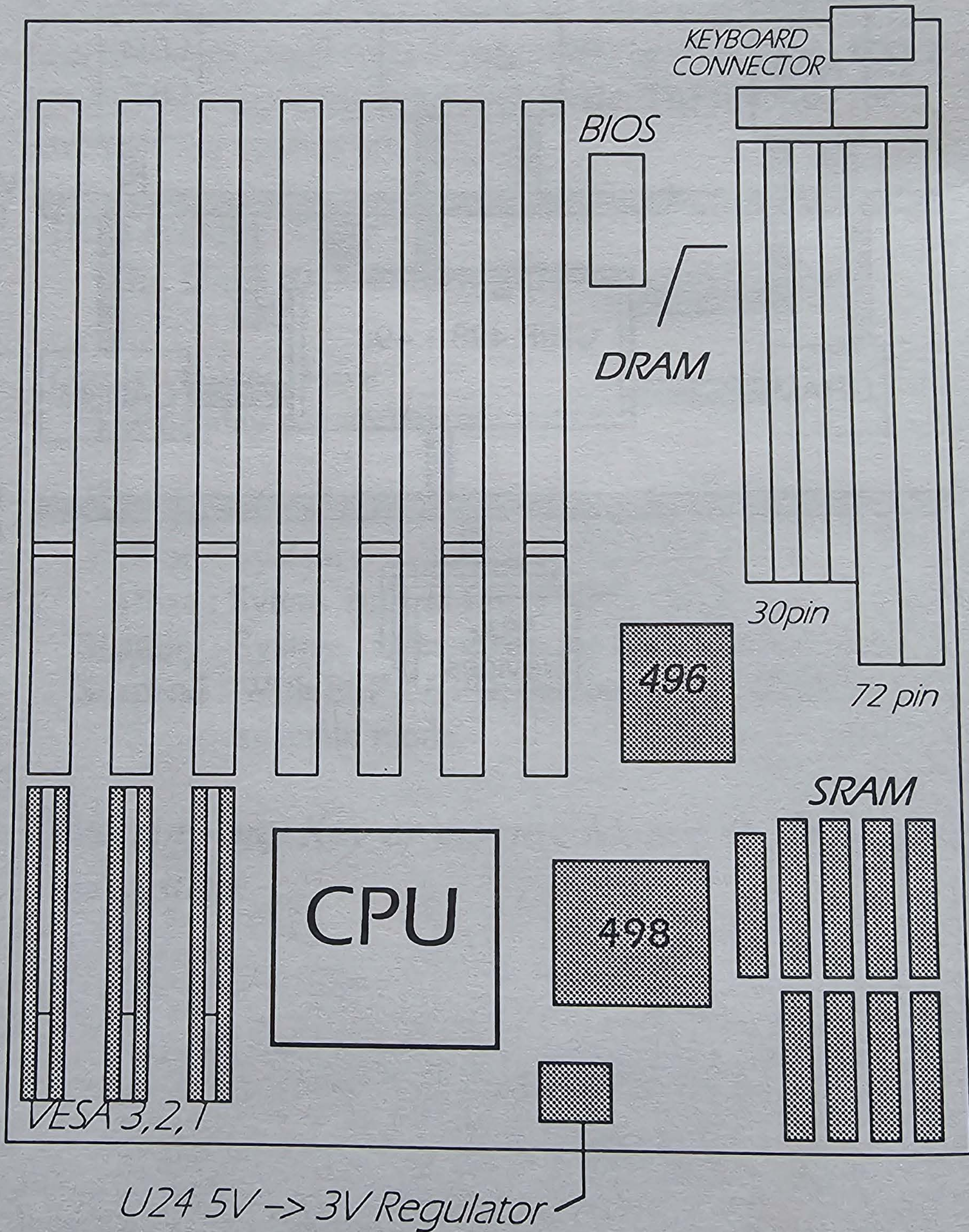
Suspend : With SMM CPU, performs stop clock in suspend mode

Pressing any Key or moving Mouse to Wake up the system.

System Block Diagram



System Board Layout



Chapter 2

Jumper setting and connector

2-1 CPU TYPE SELECT:

	JP11	JP12	JP13	JP17	JP18	JP19
486SX	OPEN	2 - 3	2 - 3	OPEN	OPEN	OPEN
486DX	OPEN	2 - 3	1 - 2 3 - 4	1 - 2	OPEN	OPEN
486DX-SL	1 - 2	1 - 2	1 - 2 3 - 4	1 - 2	5 - 6	1 - 2 3 - 4
P24D	1 - 2 4 - 5	1 - 2 4 - 5	1 - 2 3 - 4	1 - 2	3 - 4 5 - 6	1 - 2 3 - 4
P24T	1 - 2	1 - 2	1 - 2 3 - 4	2 - 3	5 - 6	1 - 2 3 - 4
M6 Cyrix	1 - 2 3 - 4 5 - 6 #	1 - 2 3 - 4 5 - 6	2 - 3	OPEN	2 - 3 4 - 5	2 - 3 4 - 5
M7 Cyrix	1 - 2 3 - 4 5 - 6 #	1 - 2 3 - 4 5 - 6	1 - 2 3 - 4	1 - 2	2 - 3 4 - 5	2 - 3
AMD486DXL	2 - 3	2 - 3	1 - 2 3 - 4	1 - 2 3 - 4	1 - 2	OPEN
UMC486	2 - 3	2 - 3	2 - 3	3 - 4	1 - 2	OPEN

MARK ' #' IS FOR DOUBLE CLOCK

P24C : Jumper setting is same as 486DX-SL

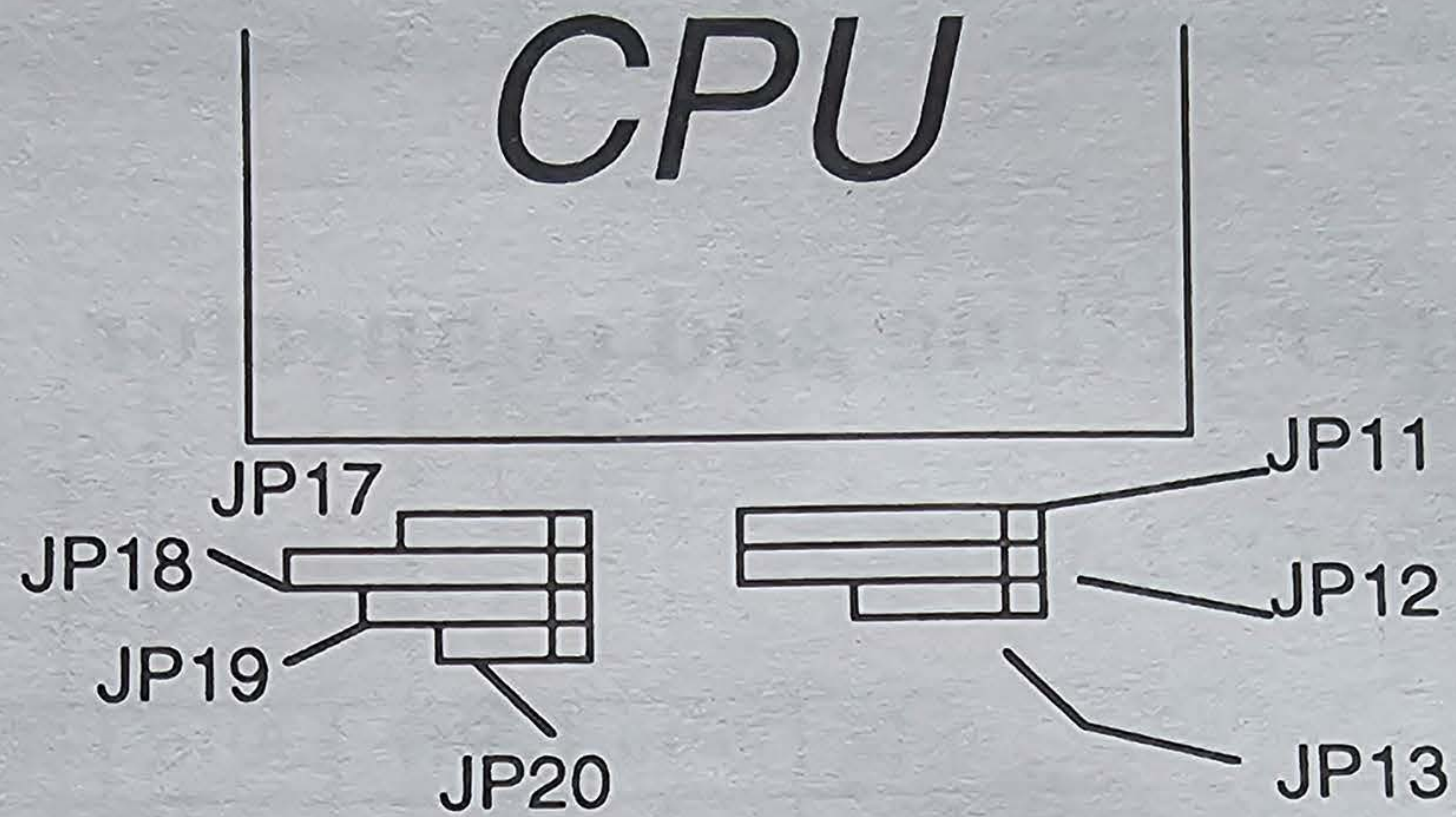
JP20 : OPEN : --> INT. CLK x 3

1 - 2 : --> x 2.5

2 - 3 : --> x 2

Others type CPU this (JP20) is open

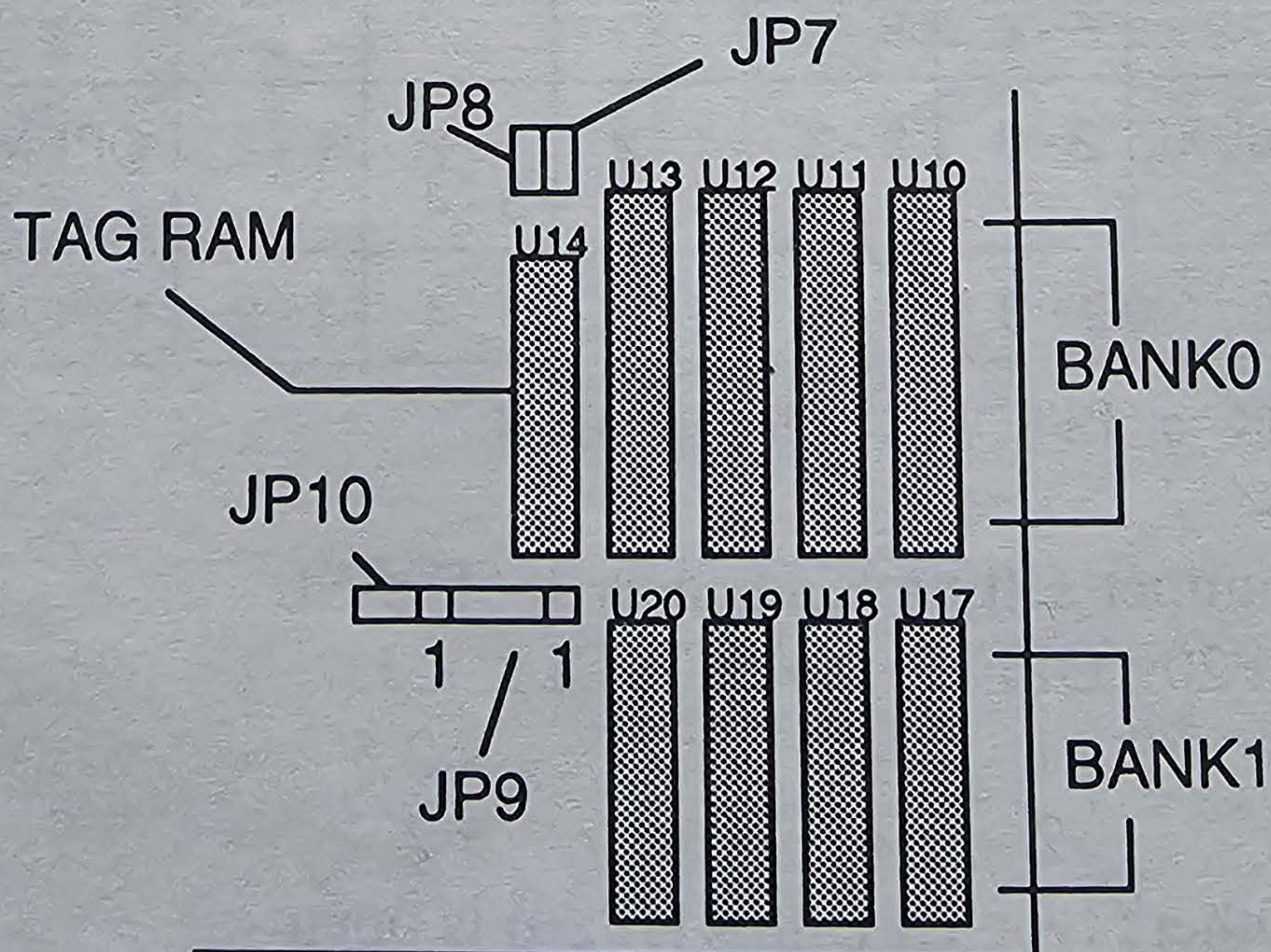
Jumper Location :



2-2 CACHE SIZE SETTING :

	256K TWO BANK 32K x 8	256K ONE BANK 64K x 8	128K	64K
JP7	ON	ON	OFF	OFF
JP8	ON	ON	ON	OFF
JP9	2 - 3	1 - 2, 3 - 4	1 - 2	OPEN
JP10	2 - 3	1 - 2	1 - 2	2 - 3

SRAM Jumper location :

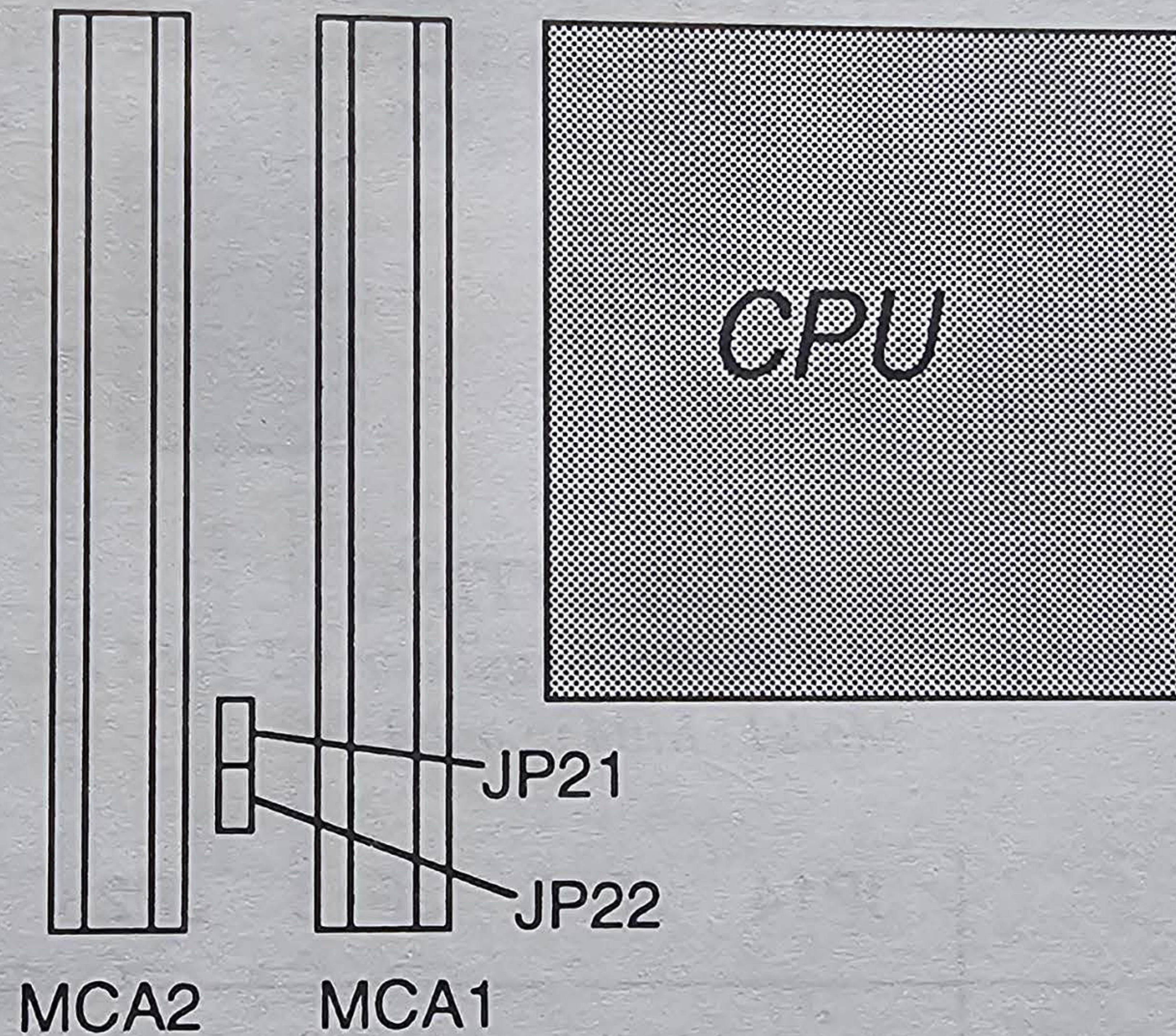


2 - 3 VESA BUS JUMPER

JP21 -- Close for VESA clock > 33 MHz
Open for VESA clock ≤ 33 MHz

JP22 -- Close for VESA 1 wait state
Open for VESA 0 wait state

Jumper location :

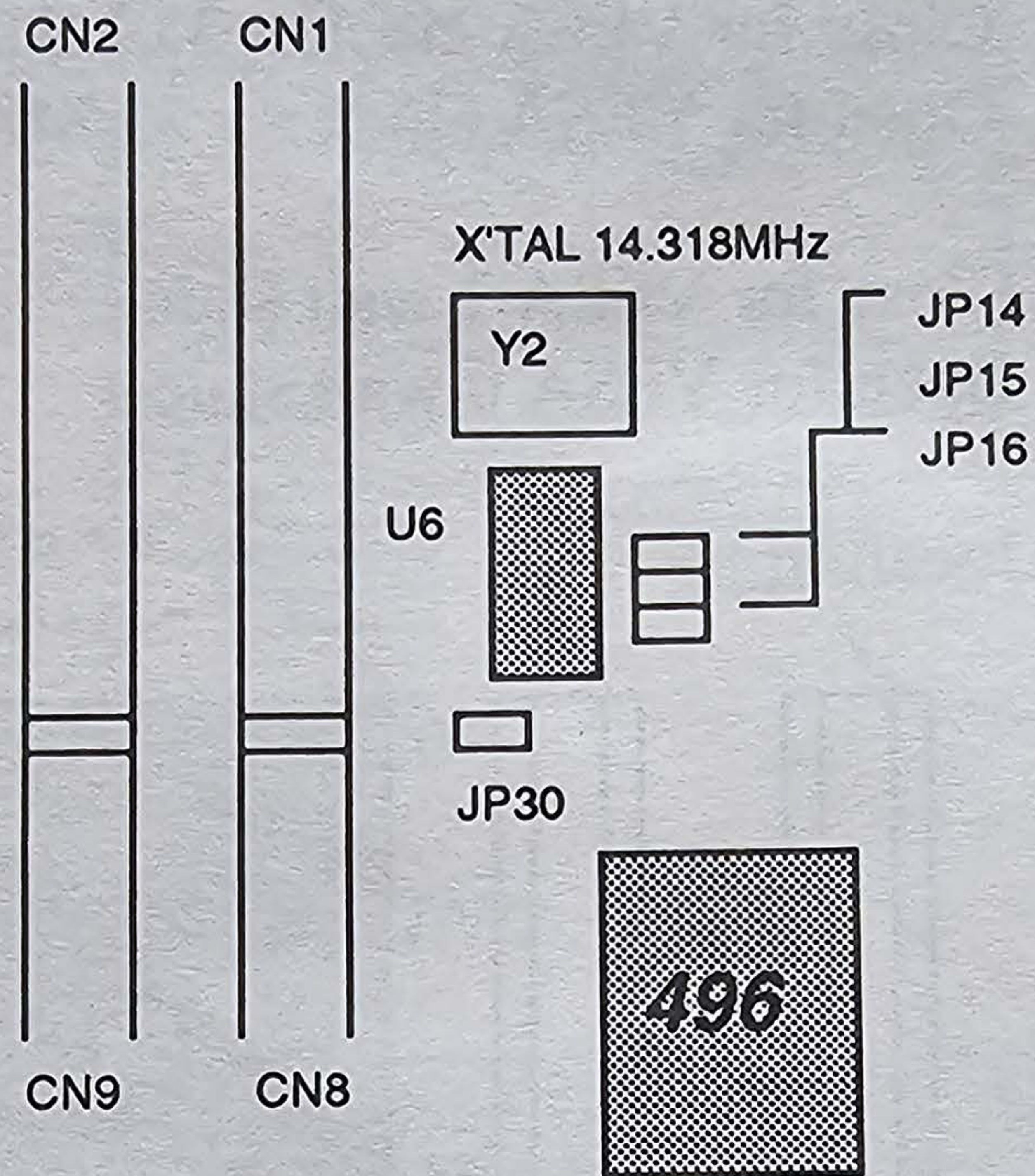


2 - 4 CPU CLOCK SETTING :

	JP6	JP5	JP4
25MHz	CLOSE	OPEN	OPEN
33MHz	CLOSE	CLOSE	CLOSE
40MHz	CLOSE	CLOSE	OPEN
50MHz	OPEN	OPEN	CLOSE

JP30 : Normal close for output clock speed select

Jumper Location :

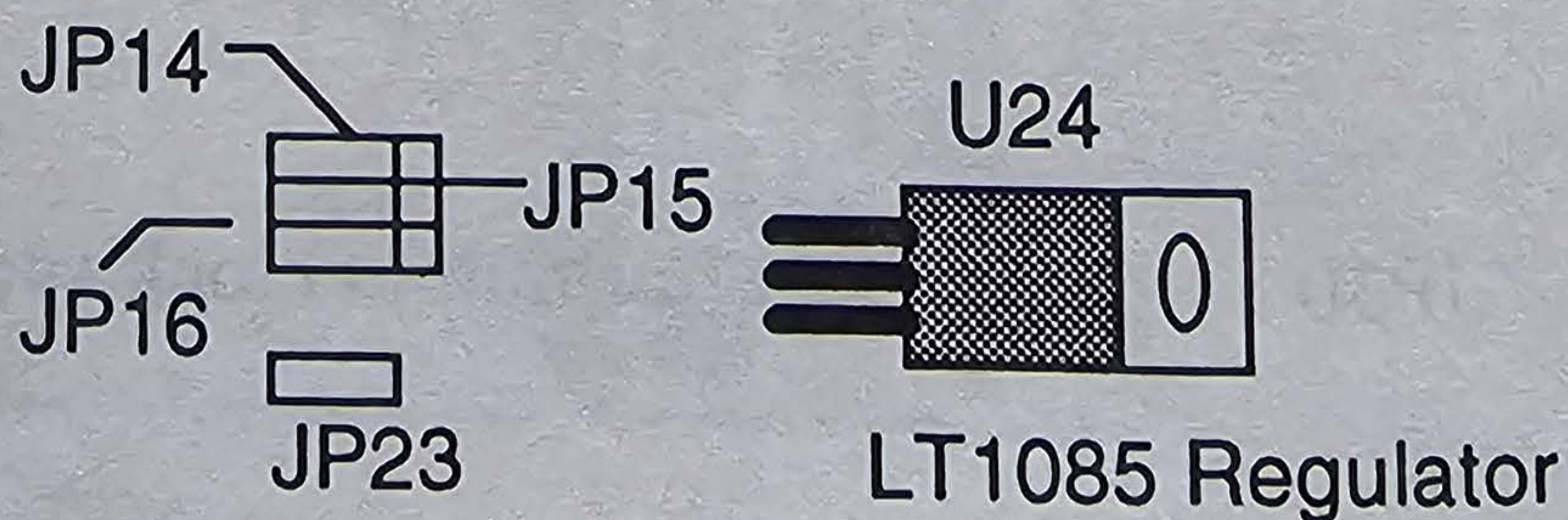


2 - 5 CPU POWER SETTING

U24 for 5V --> 3.3V, 3.45V regulator, LT 1085 must be installed (for Model : MB456 only)

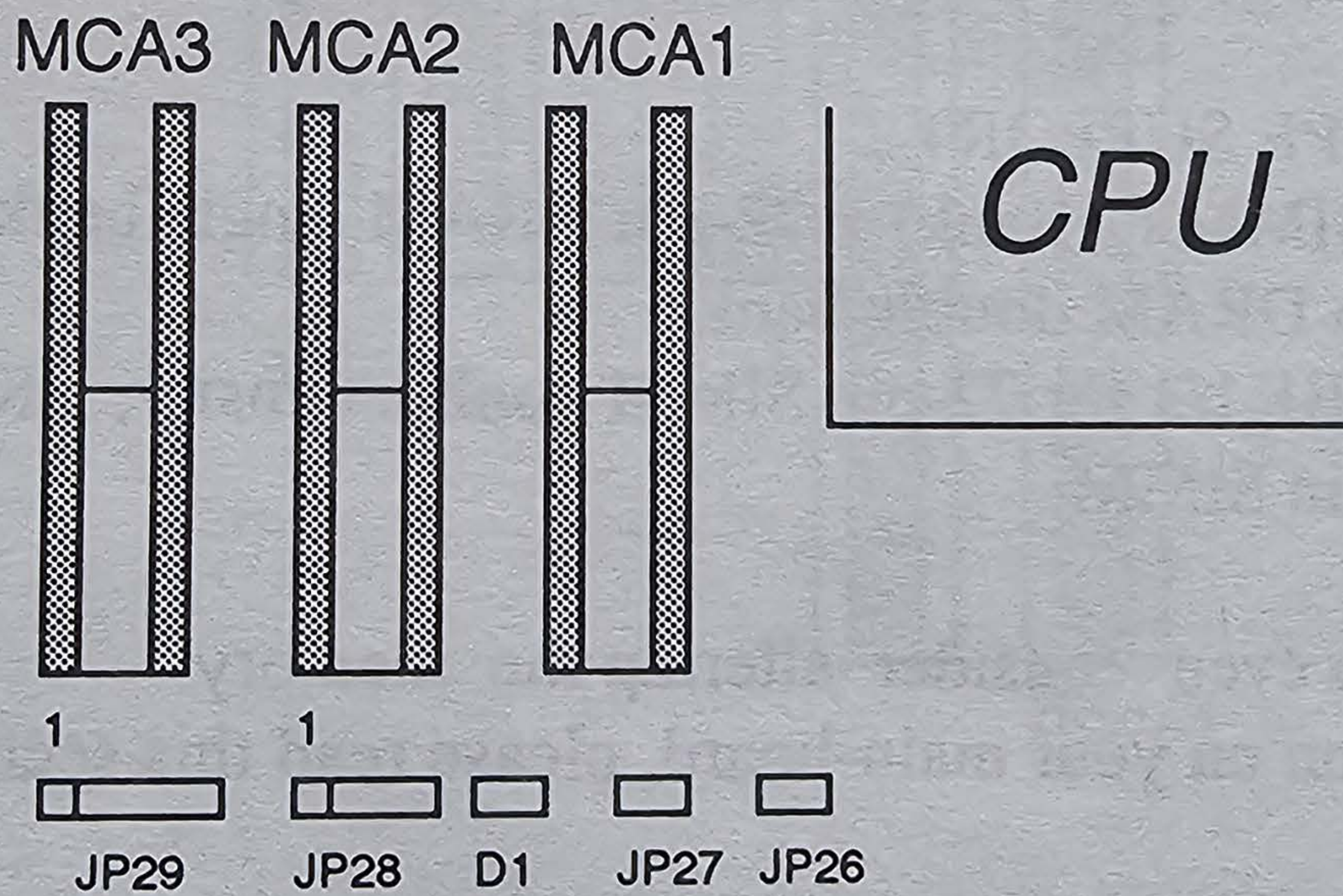
	JP14	JP15	JP16	JP23
3.3V	1 - 2	1 - 2	1 - 2	CLOSE
3.45V	1 - 2	1 - 2	1 - 2	OPEN
5 V	2 - 3	2 - 3	2 - 3	OPEN

Jumper Location :



2 - 6 OTHER ON BOARD JUMPER SETTING

- P1 : Power Connector
- KB1 : Keyboard Connector
- JP26 : Hardware Reset
- D1 : Turbo LED
- JP27 : Turbo Switch
- JP29 : Power LED and Key Lock
- JP28 : Speaker
- JP17 : Normal close for internal KBC. keylock
- JP1 : For on board battery --> Normal 2 - 3
For extend battery --> Pin 1 "+", Pin 4 "-"



2 - 7 DRAM INSTALLATION

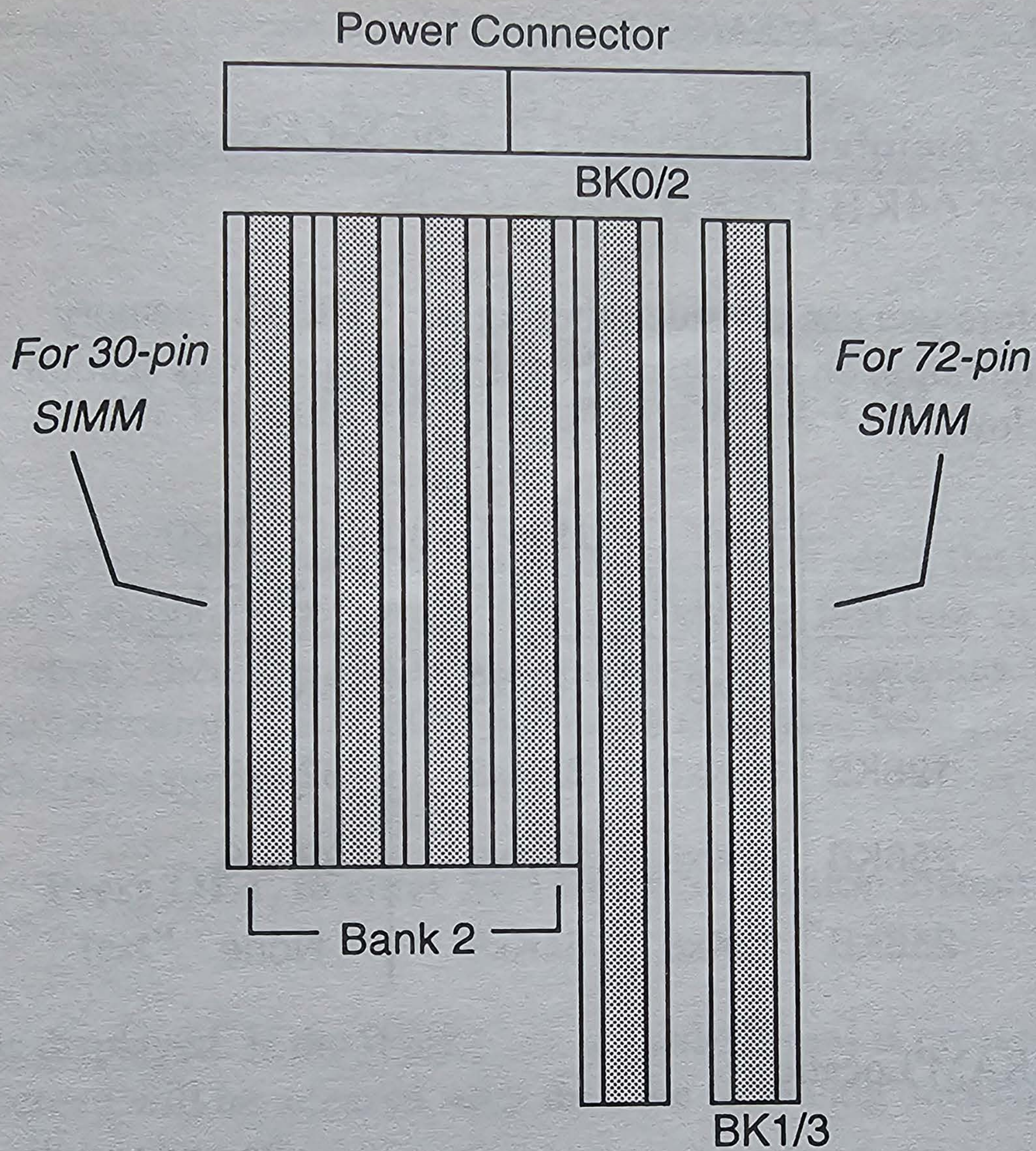
The memory is capable of supporting a minimum 1 Megabyte of memory up to total 64 megabytes memory. The 256KB /1MB / 4MB/16MB SIMM memory are available.

The mainboard allows you to install and expand the system memory via on board four 30-pin SIMM and two 72-pin SIMM sockets. It supports fast-page mode DRAM SIMM memory, with a minimum 70ns RAS (Row Address Strobe) access time. There are four banks of memory (Bank0/1/2/3), you don't care which one is Bank0 because the BIOS will automatically test which one is Bank0.

DRAM TYPE SUPPORT :

30-pin SIMM (1 Bank) + 72-pin DRAM single bank
+ 72-pin DRAM double bank
BK0/2, BK1/3 for 72-pin SIMM double density, BK2
for 30-pin SIMM.

Before you even consider altering the memory configuration on your main-board, please read this section as below:



Note : If Bank2 has been installed , the bank 'BK0/2' cann't be used double density SIMM. you just use single side 72-pin SIMM. Because the BK2 was being used for 30-pin SIMM. So if you want to use BK2(30-pin) and BK0/2(72-pin) at the sametime then the BK0/2(72-pin) SIMM must be used as single side SIMM.

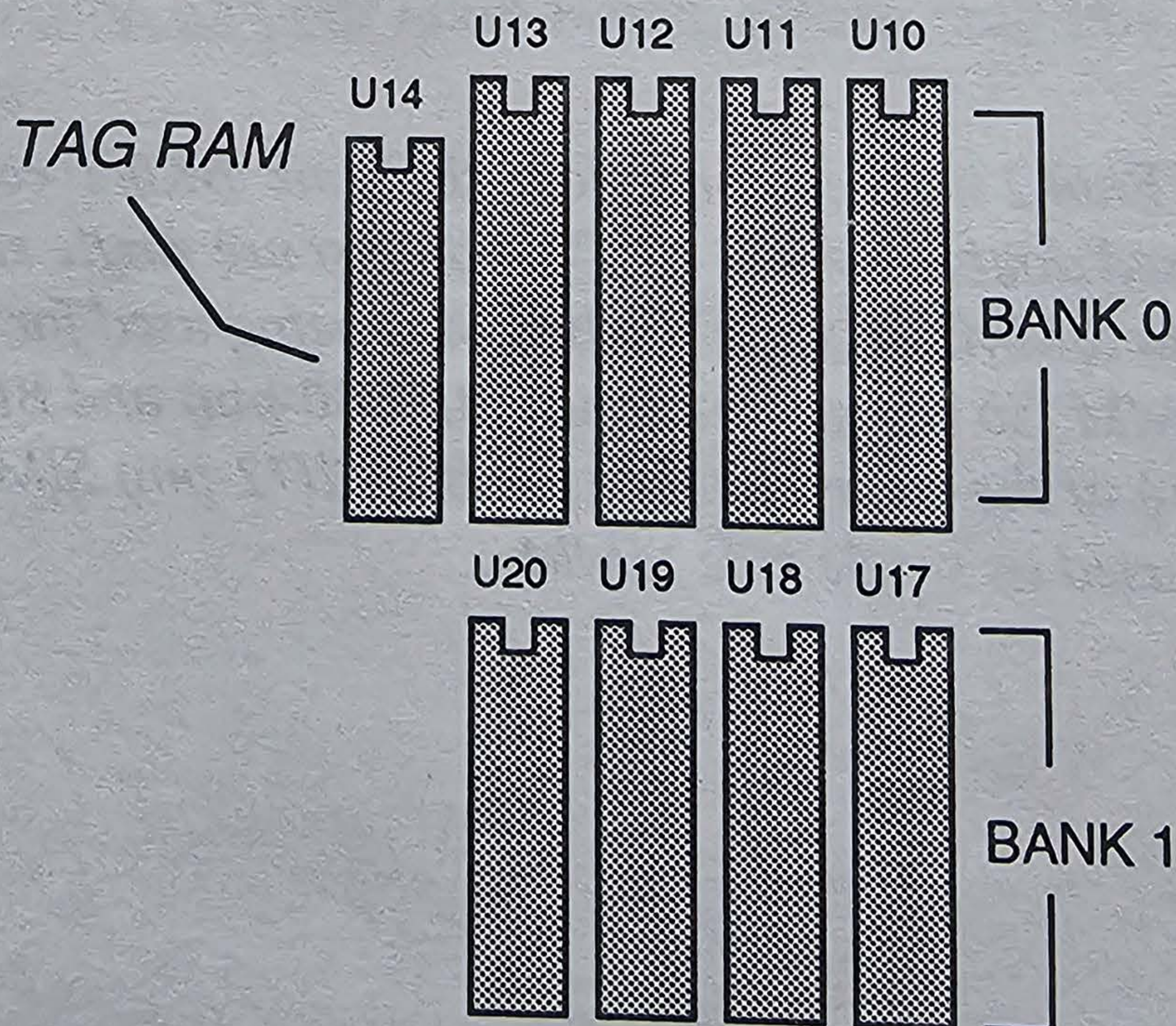
2 - 8 CACHE MEMORY INSTALL

This mainboard supports Cache SRAM configurations: 64KB, 128KB and 256KB.

Before you can consider altering the CACHE memory configuration on your main-board, please read this section as below:

	U14 TAG.R	U10 - U13 BANK 0	U17 - U20 BANK 1
64KB	8Kx8	8Kx8	8Kx8
128KB	32Kx8	32Kx8	32Kx8
256KB	32Kx8	32Kx8	32Kx8
256KB	32Kx8	64Kx8	None

SRAM Location :



Chapter 3

AWARD BIOS SETUP

When the system is being powered on or reset, the BIOS will display a copyright message on the first line of the screen, then the BIOS will perform the diagnostics and initialization. After all of the above tests have been passed, the message

"Press DEL to enter SETUP, ESC to skip memory test"

is displayed. If the [DEL] key or [ctrl-alt-esc] is pressed, the screen will be cleared and then the following message will be showed:

ROM ISA BIOS (XXXXXXXX)
CMOS SETUP UTILITY
AWARD SOFTWARE. INC.

STANDARD CMOS SETUP	PASSWORD SETTING
BIOS FEATURES SETUP	IDE HDD AUTO DETECTION
CHIPSET FEATURES SETUP	SAVE & EXIT SETUP
POWER MANAGEMENT SETUP	EXIT WITHOUT SAVING
LOAD BIOS DEFAULTS	
LOAD SETUP DEFAULTS	

3 - 1 Standard CMOS Setup

Date (mn/date/year) : Sat, Jan 1 1994						
Time (hh/min/sec) : 16 : 45 : 44						
	CYLS	HEADS	PRECOMP	LANDZONE	SECTORS	
Drive C: None (0Mb)	0	0	0	0	0	0
Drive D: None (0Mb)	0	0	0	0	0	0
Drive A: : 1.2M , 5.25 in.						
Drive B: : None						
Video : EGA/VGA						
Halt On : All Errors						
				Base Memory:	640K	
				Extended Memory:	3328K	
				Expended Memory:	0K	
				Other Memory:	128K	
				<hr/>		
				Total Memory:	4096K	

The setup program is completely menu-driven:

1. Use arrow keys to select entry : Data, Time, Hard Disk(C/D), Floppy, and Display.
2. Use PgUp/PgDn key to modify the option of each entry.
3. Use Esc to exit this screen.

3 - 2 BIOS Feature Setup

If you don't really understand the meanings of each item, please don't change the default values. The default setting maybe different from those shown below:

ROM ISA BIOS (XXXXXXXX)
BIOS FEATURES SETUP
AWARD SOFTWARE, INC.

Virus Warning	: Disabled	System BIOS Shadow	: Enabled
CPU Internal Cache	: Enabled	Video BIOS Shadow	: Enabled
External Cache	: Enabled	C8000-CBFFF Shadow	: Disabled
Quick Power on Seft Test	: Enabled	CC000-CFFFF Shadow	: Disabled
Boot Sequence	: A, C	D0000-D3FFF Shadow	: Disabled
Swap Floppy Driver	: Disabled	D4000-D7FFF Shadow	: Disabled
Boot Up Floppy Seek	: Enabled	D8000-DBFFF Shadow	: Disabled
Boot Up NumLock Status	: On	DC000-DFFFF Shadow	: Disabled
Boot Up System Speed	: High	E0000-E3FFF Shadow	: Disabled
HDD IDE Block Mode	: Disabled	E4000-E7FFF Shadow	: Disabled
Gate A20 Option.	: Fast	E8000-EBFFF Shadow	: Disabled
Memory Parity Check	: Enabled	EC000-EFFFF Shadow	: Disabled
Typematic Reat Setting	: Disabled		
Typematic Reat (Chars/Sec)	: 6		
Typematic Reat (Msec)	: 250		
Security Option	: Setup		

3 - 3 Chipset Features Setup

The Chipset Features Setup is entirely chipset specific portion and requires full knowledge about the detail definition of UMC chipset . Each option is tightly corresponding with the hardware structure. Without our engineering change notice, we strongly recommend "don't change any contents in advanced chipset setup menu".

ROM ISA BIOS (XXXXXXXX)
 CHIPSET FEATURES SETUP
 AWARD SOFTWARE, INC.

Auto Configuration	: Enabled	Alt Bit in Tag SRAM	: 7 + 1 Bit
DRAM Wait State select	: 2 WS	ISA Bus Refresh Mode	: Fast
DRAM Type	: Normal Page	DRAM Hiddern Refresh	
L2 Cache Read Wait State	: 3-2-2-2	LOWA20# Emulation	: Disabled
L2 Cache Write Wait State	: 2WS	RC Reset Emulation	: Disabled
Keyboard Controller Clock	: 9.5 MHz	Weitek type coprocessor	: Absent
ISA Bus Clock Option	: CLKI/4	Non-Cacheable Block 0	: Disabled
System BIOS Cacheable	: Disabled	Non-Cacheable Block 0 Size	: 1MB
Video BIOS Cacheable	: Disabled	Non-Cacheable Block 0 Base	: 1000000H
IO Recovery (Bus/Onboard)	: 5/ 3	Non-Cacheable Block 1	: Disabled
Weitek Ready Out Delay	: 2WS	Non-Cacheable Block 1 Size	: 1MB
Local Ready Delay Setting	: Delay 1T	Non-Cacheable Block 1 Base	: 1000000H
Signal LDEV# Sample Time	: In T2		
CPU ADS# Delay 1T or Not	: Delay 1T		
Flush Cache when Dethrbo	: Disabled		
Force Miss when Deturbo	: Disabled		
Hold CPU Percentage	: 4/16		

3 - 4 Power Management Setup

Supporting the EPA Energy Star PC specification with Deep

Green system Design. It supports the advanced SMM CPU. Accommodated with Intel S series CPU or AMD DXL, DXL2 CPU, system performs stop clock mode. The function for power savings options are:

. HDD Standby Timer :

The Hard disk entering power down mode.

. Display Power Down :

The display screen will be closed.

. System power down mode :

Full-on : System runs in full speed CPU clock

Doze : Sytem runs in lower CPU clock

Standby : System scales-down the CPU clock

Suspend : With SMM CPU, performs stop clock in suspend mode

ROM ISA BIOS (X X X X X X X X)
 POWER MANAGEMENT SETUP
 AWARD SOFTWARE, INC.

Power Management : Disabled	* Monitor Even In Full On Mode
Video Off Method : Blank Screen	VESA Slave Activity : Disabled
HDD Standby Timer : Disabled	LPT Port Activity : Enabled
Doze Timer Select : 512 Min	COM Port Activity : Enabled
Standby Timer Select : 512 Min	ISA Master Activity : Enabled
Inactive Timer Select : 512 Min	IDE Activity : Enabled
Control Item : CPU CLK VGA	Floppy Activity : Enabled
Doze mode Control : 1/4 CLKI On	VGA Activity : Disabled
Standby Mode Control : 1/8 CLKI Off	Keyboard Active : Enabled
Inactive Mode Control : STOP CLK Off	
Suspend Switch Select : Disabled	

POWER MANAGEMENT Timer Selection :

Disabled : HDD Standby Timer : Disabled
 Doze Timer Select : 512 Min
 Standby Timer Select : 512 Min
 Inactive Timer Select : 512 Min

Min Saving : HDD Standby Timer : 15 Min
 Doze Timer Select : 512 Min
 Standby Timer Select : 512 Min
 Inactive Timer Select : 512 Min

Max Saving : HDD Standby Timer : 1 Min
 Doze Timer Select : 0.5 Min
 Standby Timer Select : 2 Min
 Inactive Timer Select : 2 Min

Optimize : HDD Standby Timer : 3 Min
Doze Timer Select : 8 Min
Standby Timer Select : 8 Min
Inactive Timer Select : 8 Min

User Define : HDD Standby Timer : Disabled
Doze Timer Select : 512 Min
Standby Timer Select : 512 Min
Inactive Timer Select : 512 Min

Control Item Select :

CPU CLK : For CPU input Clock Control
1/4 CLKI --> Slow Down CPU to Clock/4
1/8 CLKI --> Slow Down CPU to Clock/8
STOP CLK --> CPU Clock Stop
VGA : On --> Display screen open
Off--> The display screen will be closed.

Wake up the system:

Pressing any Key or moving Mouse to Wake up the system.

3-5 Standard type of hard disk

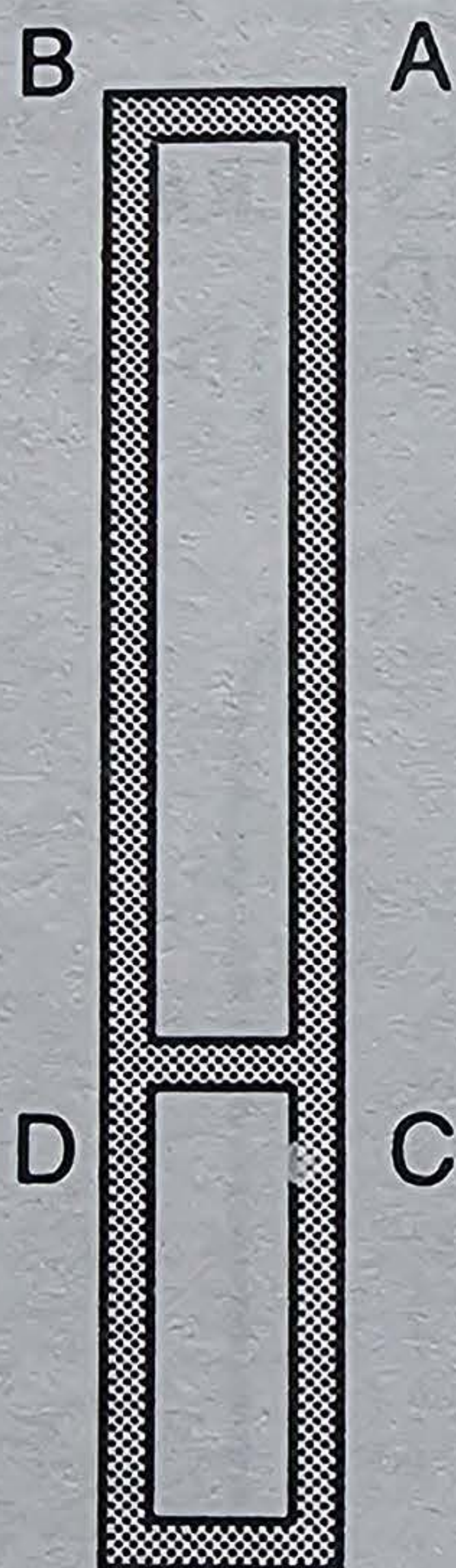
Type	Size	Cylinders	Heads	Sec	W-Pcomp	L-Zone
1	10MB	306	4	17	128	305
2	20MB	615	4	17	300	615
3	30MB	615	6	17	300	615
4	62MB	940	8	17	512	940
5	46MB	940	6	17	512	940
6	20MB	615	4	17	None	615
7	30MB	462	8	17	256	511
8	30MB	733	5	17	None	733
9	112MB	900	15	17	None	901
10	20MB	820	3	17	None	820
11	35MB	855	5	17	None	855
12	49MB	855	7	17	None	855
13	20MB	306	8	17	128	319
14	42MB	733	7	17	None	733
15	Reserved					
16	20MB	612	4	17	0	663
17	40MB	977	5	17	300	977
18	56MB	977	7	17	None	977
19	59MB	1024	7	17	512	1023
20	30MB	733	5	17	300	732
21	42MB	733	7	17	300	732
22	30MB	306	5	17	300	733
23	10MB	977	4	17	0	336
24	40MB	1024	5	17	None	976
25	76MB	1224	9	17	None	1023
26	71MB	1224	7	17	None	1223
27	111MB	1224	11	17	None	1223
28	152MB	1024	15	17	None	1223
29	68MB	1024	8	17	None	1023
30	93MB	918	11	17	None	1023
31	83MB	925	11	17	None	1023
32	69MB	1024	9	17	None	926
33	85MB	1024	10	17	None	1023
34	102MB	1024	12	17	None	1023
35	110MB	1024	13	17	None	1023
36	119MB	1024	14	17	None	1023
37	17MB	1024	2	17	None	1023
38	136MB	1024	16	17	None	1023
39	114MB	918	15	17	None	1023
40	40MB	820	6	17	None	1023
41	42MB	1024	5	17	None	1023
42	65MB	1024	5	26	None	1023
43	40MB	809	6	17	None	852
44	61MB	809	6	26	None	852
45	100MB	776	8	33	None	775
46	203MB	684	16	38	None	685
USER						

Chapter 4

APPENDIX

APPENDIX A :

ISA SLOT PIN OUT SPECIFICATIONS :



A1 : IOCHCK#	A17: SA14
A2 : SD7	A18: SA13
A3 : SD6	A19: SA12
A4 : SD5	A20: SA11
A5 : SD4	A21: SA10
A6 : SD3	A22: SA9
A7 : SD2	A23: SA8
A8 : SD1	A24: SA7
A9 : SD0	A25: SA6
A10: IOCHRDY	A26: SA5
A11: BAEN	A27: SA4
A12: SA19	A28: SA3
A13: SA18	A29: SA2
A14: SA17	A30: SA1
A15: SA16	A31: SA0
A16: SA15	

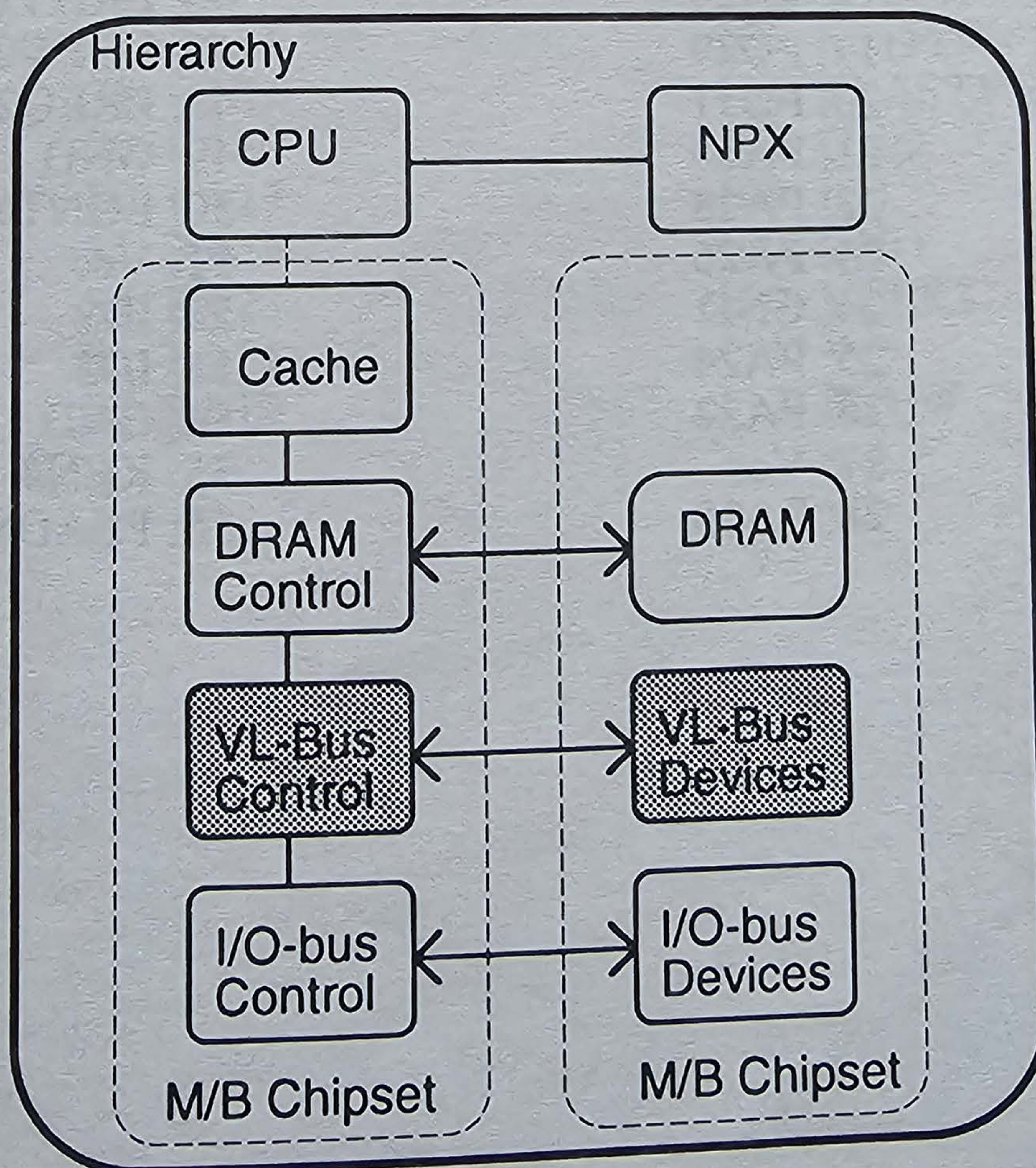
B1 : GND	C1 : SBHE#	D1 : MEMCS16#
B2 : SYSRST	C2 : SA23	D2 : IOCS16#
B3 : Vcc	C3 : SA22	D3 : IRQ10
B4 : IRQ9	C4 : SA21	D4 : IRQ11
B5 : - 5v	C5 : SA20	D5 : IRQ12
B6 : DRQ2	C6 : SA19	D6 : IRQ15
B7 : - 12v	C7 : SA18	D7 : IRQ14
B8 : WS0#	C8 : SA17	D8 : DACK0#
B9 : + 12v	C9 : MEMR#	D9 : DRQ0
B10: GND	C10: MEMW#	D10: DACK5#
B11: SMEMW#	C11: SD8	D11: DRQ5
B12: SMEMR#	C12: SD9	D12: DACK6#
B13: IOW#	C13: SD10	D13: DRQ6
B14: IOR#	C14: SD11	D14: DACK7#
B15: DACK3#	C15: SD12	D15: DRQ7
B16: DRQ3	C16: SD13	D16: Vcc
B17: DACK1#	C17: SD14	D17: MASTER#
B18: DRQ1	C18: SD15	D18: GND
B19: RFSH#		
B20: SYSCLK		
B21: IRQ7		
B22: IRQ6		
B23: IRQ5		
B24: IRQ4		
B25: IRQ3		
B26: DACK2#		
B27: TC		
B28: BALE		
B29: Vcc		
B30: OSC		
B31: GND		

APPENDIX B :

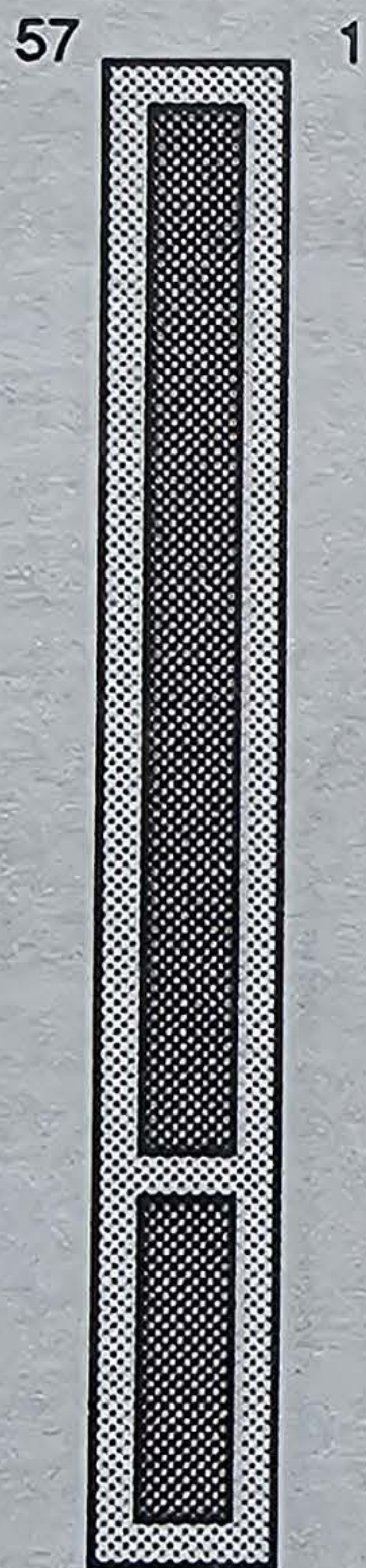
SUMMARY OF VL-BUS FEATURES :

The VL - Bus design is capable of operating zero to three VL-Bus slots. A slotless VL - Bus device would physically reside directly on the mainboard. Regardless of the number of slots, the maximum number of devices supported is three. Loading requirements allow some VL-Bus implementations to connect directly to the CPU bus without buffering address, data, and control signals. Optionally, the VL-Bus may buffer address, data, and control signals. Optionally, the VL -Bus may buffer address, data, and control signals to meet the loading requirements of full three-slot implementations.

VL-BUS INTERFACE BLOCK DIAGRAM :



VL-BUS PIN OUT SPECIFICATIONS

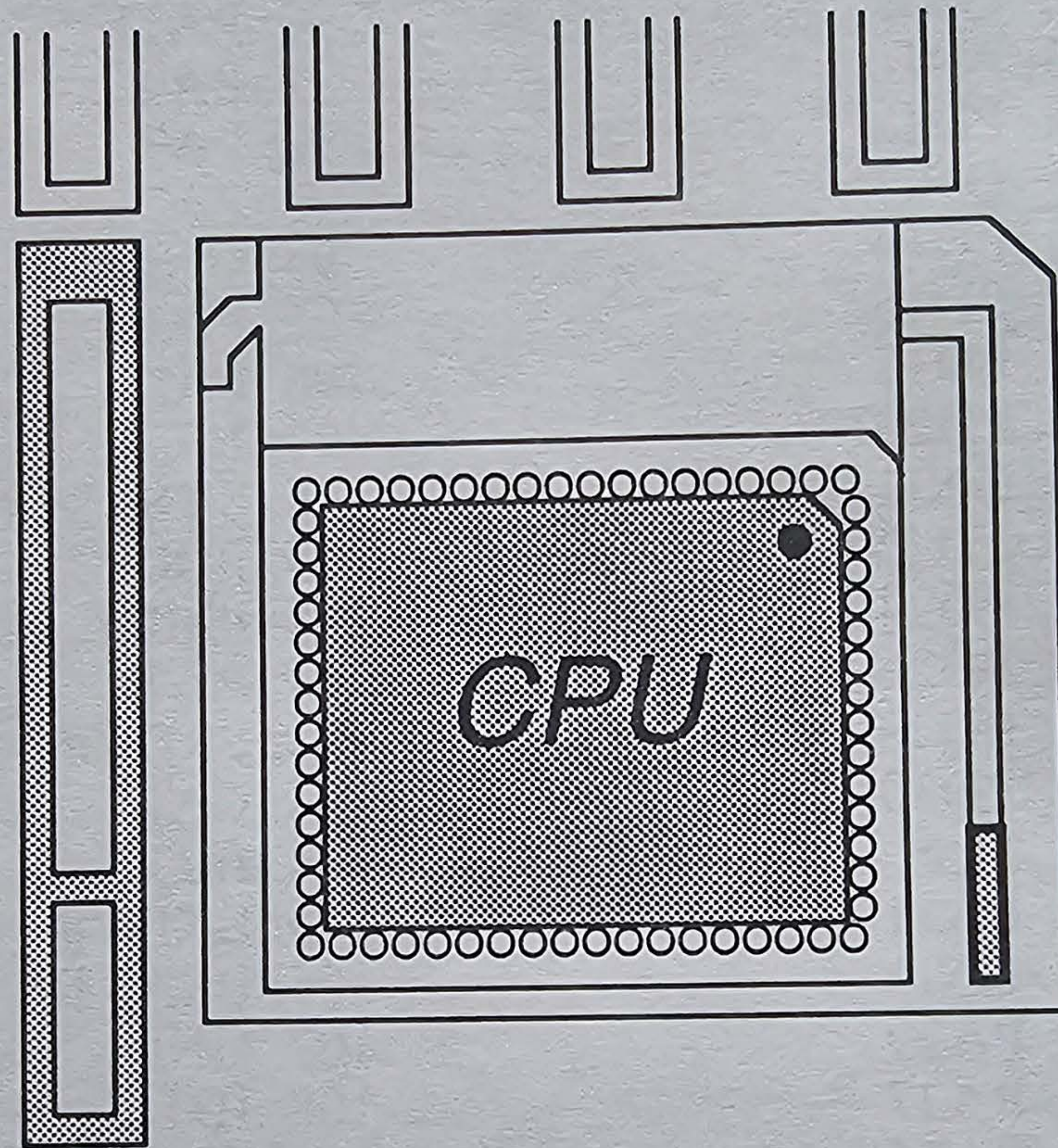


- | | |
|----------|------------|
| 1 : PD1 | 29: PA18 |
| 2 : PD3 | 30: PA16 |
| 3 : GND | 31: PA14 |
| 4 : PD5 | 32: PA12 |
| 5 : PD7 | 33: PA10 |
| 6 : PD9 | 34: PA8 |
| 7 : PD11 | 35: GND |
| 8 : PD13 | 36: PA6 |
| 9 : PD15 | 37: PA4 |
| 10: GND | 38: HITM# |
| 11: PD17 | 39: BE0# |
| 12: Vcc | 40: Vcc |
| 13: PD19 | 41: BE1# |
| 14: PD21 | 42: BE2# |
| 15: PD23 | 43: GND |
| 16: PD25 | 44: BE3# |
| 17: GND | 45: PADS# |
| 18: PD27 | 46: LRDY# |
| 19: PD29 | 47: LDEV2# |
| 20: PD31 | 48: LREQ2# |
| 21: PA30 | 49: GND |
| 22: PA28 | 50: LGNT# |
| 23: PA26 | 51: Vcc |
| 24: GND | 52: ID2 |
| 25: PA24 | 53: ID3 |
| 26: PA22 | 54: GND |
| 27: Vcc | 55: KEN# |
| 28: PA20 | 56: PEADS# |

57: PD0	85: GND
58: PD2	86: PA17
59: PD4	87: PA15
60: PD6	88: Vcc
61: PD8	89: PA13
62: GND	90: PA11
63: PD10	91: PA9
64: PD12	92: PA7
65: GND	93: PA5
66: PD14	94: GND
67: PD16	95: PA3
68: PD18	96: PA2
69: PD20	97: N/C
70: GND	98: SYSRST#
71: PD22	99: PDC
72: PD24	100: PMIO
73: PD26	101: PWR
74: PD28	102: PRDY#
75: PD30	103: GND
76: Vcc	104: IRQ9
77: PA31	105: BRDY#
78: GND	106: BLAST#
79: PA29	107: GND
80: PA27	108: ID1
81: PA25	109: GND
82: PA23	110: VCLKI
83: PA21	111: Vcc
84: PA19	112: BS16#

APPENDIX C:

INSTALLING CPU :



The system board is specifically designed to support Intel, AMD, Cyrix and UMC CPU as below :

Intel 486SX,486DX,486DX2,486DX4,
Overdrive P24T,P24D,P24C
and S-series SMM CPU
AMD 486DX,DX2,DXL,DXL2/66
Cyrix M6, M7
UMC 486 CPU

Note : Place the CPU into the socket. Make sure pin 1 on the CPU lines up with pin 1 on the socket.

APPENDIX D : AT TECHNICAL INFORMATION

D-1 : I/O & MEMORY MAP

MEMORY MAP :

[0000000-009FFFF]	System memory used by DOS and application program.
[00A0000-00BFFFF]	Display buffer memory for VGA/EGA/CGA/Monochrome adapter.
[00C0000-00DFFFF]	Reserved for I/O device BIOS ROM or RAM buffer.
[00E0000-00EFFFF]	Reserved for BASIC ROM.
[00F0000-00FFFFFF]	System BIOS ROM.
[0100000-1FFFFFF]	System extension memory.

I/O MAP :

From	To	Description
001	01F	DMA controller.(MASTER)
020	021	INTERRUPT controller.(MASTER)
022	023	CHIPSET control registers I/O ports.
040	05F	TIMER control registers.
060	06F	KEYBOARD interface controller.(8042)
070	07F	RTC ports & CMOS I/O ports.
080	09F	DMA register.
0A0	0BF	INTERRUPT controller.(SLAVE)
0C0	0DF	DMA controller.(SLAVE)
0F0	0FF	MATH COPROCESSOR
1F0	1F8	HARD DISK controller
278	27F	PARALLEL port-2
2B0	2DF	GRAPHICS adapter controller.
2F8	2FF	SERIAL port-2

From	To	Description
360	36F	NETWORK ports.
378	37F	PARALLEL ports-1.
3B0	3BF	MONOCHROME & PRINTER adapter.
3C0	3CF	EGA adapter.
3D0	3DF	CGA adapter
3F0	3F7	FLOPPY DISK controller.
3F8	3FF	SERIAL port-1.

D-2 : TIMER & DMA CHANNELS MAP

TIMER MAP:

TIMER Channel-0 system timer interrupt
 TIMER Channel-1 DRAM REFRESH request
 TIMER Channel-2 speaker tone generator

DMA CHANNELS:

DMA Channel-0 Available
 DMA Channel-1 IBM SDLC
 DMA Channel-2 FLOPPY DISK adapter
 DMA Channel-3 Available
 DMA Channel-4 Cascade for DMA controller 1
 DMA Channel-5 Available
 DMA Channel-6 Available
 DMA Channel-7 Available

D-3 : INTERRUPT MAP

NMI: Parity check error

IRQ(H/W): 0 System TIMER interrupt from TIMER-0
1 KEYBOARD output buffer full
2 Cascade for IRQ 8-15
3 SERIAL port 2
4 SERIAL port 1
5 PARALLEL port 2
6 FLOPPY DISK adapter
7 PARALLEL port 1
8 RTC clock
9 Available
10 Available
11 Available
12 Available
13 MATH coprocessor
14 HARD DISK adapter
15 Available

D-4 RTC & CMOS RAM MAP

RTC & CMOS:

00	Seconds
01	Second alarm
02	Minutes
03	Minutes alarm
04	Hours
05	Hours alarm
06	Day of week
07	Day of month
08	Month
09	Year
0A	Status register A
0B	Status register B
0C	Status register C
0D	Status register D
0E	Diagnostic status byte
0F	Shutdown byte
10	FLOPPY DISK drive type byte
11	Reserve
12	HARD DISK type byte
13	Reserve
14	Equipment type
15	Base memory low byte
16	Base memory high byte
17	Extension memory low byte
18	Extension memory high byte
19-2D	Reserve
2E-2F	2-byte, COMS RAM chechsum
30	Reserve for extension memory low byte
31	Reserve for extension memory high byte
32	DATE CENTURY byte
33	INFORMATION FLAG
34-3F	Reserve
40-7F	Reserve for CHIPSET SETTING DATA

