RADIO FREQUENCY INTERFERENCE STATEMENT

This equipment generates and uses radio frequency energy and if not installed and used properly, that is, in strict accordance with the manufacturer's instructions, may cause interference with radio and television reception.

If this equipment does cause interference to radio or TV reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

* *Reorient the receiving antenna.*
* *Relocate the computer away from the receiver.*
* *Move the computer away from the receiver.*
* *Plug the computer into a different outlet so that computer and receiver are on different branch circuits.*
* *Ensure that card slot covers are in place when no card is installed.*
* *Ensure that card mounting screws, attachment connector screws, and ground wires are tightly secured.*
* *If peripherals are used with this system, it is suggested to use shielded, grounded cables, with in-line filters if necessary.*

If necessary, the user should consult the dealer service representative for additional suggestions.

The manufacturer is not responsible for any radio or TV interference caused by unauthorized modifications to this equipment. It is the responsibility of the user to correct such interference.

NOTE

1. When you see an error message appear on the screen after turning the power on, leave the system switched on for one or two hours to recharge the battery. You can then enter the system configuration.

2. Leave your system switched on for 10 to 15 hours to completely recharge the battery.

3. If you had left the system switched off for more than one month, follow step 2, above.

VERSION: 1.0

CONTENT

Chapter 1 INTRODUCTION

OCTEK Pointer-386 consists of 32-bit 80386 microprocessor, a large cache memory and highly integrated chipsets to provide high performance, reliability and compatibility. OCTEK Pointer-386 is a perfect choice for CAD/CAM workstation and file server and can support sophisticated 32-bit applications and multi-user operating systems.

To speed up the performance of the system, a cache memory with maximum size of up to 64KB is incorporated. Frequently used program codes can be fetched by CPU from the high speed cache memory without wait state. Furthermore, access to main memory is accelerated because the cache controller and memory controller are integrated together and operate concurrently to minimize the overhead of accessing main memory.

Aimed at supporting advanced CAD/CAM applications, OCTEK Pointer-386 supports 80387 or WEITEK 3167. 8MB memory can be installed on board and additional 8MB is on memory expansion board which is installed on a fast speed 32-bits memory expansion slot.

Fast A20 gate and fast reset generation are incorporated to improve the performance of advanced operation system and expanded memory managers.

Compatibility and reliability are important issues. I/O channel is compatible to standard AT bus. Therefore any peripherals may be used on OCTEK Pointer-386. On board POWERGOOD generator is essential to ensure the reliability of the system and is well-designed to work with all power supplies.

Chapter 2 GENERAL FEATURES

Specification

Processor: *Intel 80386DX CPU*
with optional 80387DX Math Coprocessor
or WEITEK 3167 Coprocessor

Speed: *Turbo/normal speed*
Software/hardware selectable

I/O Slot: *Compatible to standard AT bus*
Two 8-bit and six 16-bit slots

Cache Memory:
32KB or 64KB cache memory
Direct mapped/Write through

Memory: *Shadow RAM and Page/Interleaved mode*
SIMM sockets for 256K or 1M modules
8MB on board
Up to 16MB with option memory
Expansion board

System support functions:
- 8-Channel DMA (Direct Memory Access)
- 16-level interrupt
- 3 programmable timers
- CMOS RAM for system configuration
- Real time clock with battery back-up
- Fast A20 gate and fast reset

Other Features:
- Support EMS 4.0 with driver
- On board POWERGOOD generation
- External battery connector
- Hardware turbo switch

PROCESSOR

80386DX is a 32-bit microprocessor with 32-bit external data bus and 32-bit external address bus. Therefore it processes more data at the same time than 80286 and can access a large memory size which is necessary for 32-bit applications.

80386DX operates at real mode and protected mode. At real mode, all existing software for XT/AT can be used without problem. Furthermore, new mechanism allows switching between real mode and protected mode at fast speed. Hence multi-user operation systems and applications using EMS memory can run more efficiently.

Virtual 8086 mode is a special feature of 80386DX. It allows several programs designed for XT/AT to be executed concurrently. Programs are protected from each other by 80386DX and each can consider that it is running at a XT/AT.

Internal memory management unit is much more complicated than 80286, but provide a more flexible addressing scheme for next generation operation system. Multitasking, concurrent operation and manipulating huge data base can be accomplished with excellent performance. Paging mechanism is employed by 80386DX to allow powerful operating system to implement virtual memory.

MATH COPROCESSOR

Math coprocessor is optional and both Intel 80387 and WEITEK 3167 are supported. 80387 is upward object-code compatible from 80287 and 8087 and runs 6 to 11 times faster than 80287 used in AT. WEITEK 3167 can deliver more power than 80387 and is supported by various operation systems and compilers.

CACHE MEMORY

The cache controller is integrated into the chipset and works jointly with the memory controller. This arrangement can speed up memory access when a cache read miss occurs and hence the overall performance is improved. For a cache read hit, the CPU operation is completed with zero wait state

The cache memory size is 32KB or 64KB and the line size is 4, 8 or 16 bytes. The design of the cache controller is intended to provide optimum performance with simple construction. With 64KB cache memory, hit rate exceeds 95% and the wait state is almost eliminated.

By using cache memory, low speed DRAMs can be used for main memory because the memory need not run as fast as the CPU.

MEMORY SYSTEM

Four banks of DRAMs can be installed. Two banks are available on motherboard and others are on optional memory expansion board. The maximum memory size is 16MB when using 1MB DRAM for all banks.

The memory system provides a flexible memory configuration. 256KB and 1MB DRAM can be used together. Several combinations of DRAM types are allowed. So, a basic system is equipped with 1MB using 256KB DRAM and then memory size is increased to 5MB by putting another bank of 1MB DRAM.

The memory system supports page-interleaved mode. The memory is divided into pages. Successive memory accesses within the same page need not require wait state and thus CPU can run at full speed. When more than one bank of memory are installed, the page size is effectively increased because several banks of memory can be kept active. If four banks are filled, the page size is increased by a factor of four.

To enhance the system performance, shadow RAM mode is supported. In shadow RAM mode, system BIOS and video BIOS contained in low speed memory such as EPROM and ROM are copied into DRAM. Improvement is significant because access to DRAM is mush faster than ROM.

Another useful feature is memory remapping. 640KB is allocated as base memory. On the other hand, system BIOS and video BIOS occupy some locations between 640K and 1M. When 1M bytes or more are installed, there are some parts of DRAM overlapping with the BIOS and cannot be accessed. Memory remapping allows these parts of memory to be accessed at other locations and thus can be utilized by the software. Memory remapping is supported by hardware and can be enabled in system setup.

SYSTEM FUNCTIONS

System functions include:

- Interrupt
- DMA
- Timer
- Real time clock
- Clock and ready generation
- I/O channel control

All system functions are 100% compatible to AT standard. I/O channel of OCTEK Pointer-386 is designed to be compatible with standard AT bus. All the expansion cards conformed to the standard AT bus can be used in OCTEK Pointer-386 without problem.

Chapter 3 INSTALLING COMPONENTS

Important Note : Turn off the power before installing or replacing any component.

Installing Math Coprocessor

Math coprocessor 80387 and WEITEK 3167 are PGA devices. Beside the CPU, there is a 121-pin PGA socket. To install Math coprocessor, be sure to line up pin 1 of the Math coprocessor with pin 1 of the socket as shown below.

Installing RAM Modules

OCTEK Pointer-386 has eight sockets for SIMM modules. Whenever you add memory to the motherboard, install four modules at the same time. Also make sure that the chips on the modules face toward the memory expansion slot as shown below. The modules should be locked by the sockets. Please check carefully before turning on the power. Otherwise, the system will not work properly.

Configuration of Memory

The configuration of the memory is very flexible. Either 256KB or 1MB SIMM modules are acceptable. There are several combinations of DRAM types you may consider. So, a basic system can be equipped with fewer memory and later more memory can be installed when upgrading the system. The configuration of memory is illustrated on next page.

Page mode is always active. Interleaved mode is only enabled for the those banks with similar pairs or quartet of DRAMs. The performance is automatically better whenever the interleaved mode is active. The memory size is detected by BIOS and indicated during memory test after reset. No jumper is needed to be set for the memory size and DRAM type.

The speed of DRAM depends on the speed of the system and wait state. The highest performance is accomplished by using zero wait state, but high speed DRAM has to be used. If zero wait state is selected, fast page mode DRAM is needed. Consult your dealer for details. The number of wait state is assigned in the BIOS setup.

DRAM Configuration

	Bank	*Bank*	*Bank*	*Bank*	*Total*	*Inter-*
	0	*1*	*2*	*3*	*Memory*	*leaved*
1	*0*	*0*	*0*	*0*	*0*	
2	*256K*	*0*	*0*	*0*	*1M*	*2W*
3	*256K*	*256K*	*0*	*0*	*2M*	*2W*
4	*256K*	*256K*	*256K*	*0*	*3M*	*4W*
5	*256K*	*256K*	*256K*	*256K*	*4M*	
6	*1M*	*0*	*0*	*0*	*4M*	
7	*256K*	*1M*	*0*	*0*	*5M*	
8	*1M*	*256K*	*0*	*0*	*5M*	
9	*256K*	*256K*	*1M*	*0*	*6M*	*2W*
10	*256K*	*1M*	*256K*	*0*	*6M*	
11	*1M*	*256K*	*256K*	*0*	*6M*	
12	*256K*	*256K*	*1M*	*256K*	*7M*	*2W*
13	*256K*	*1M*	*256K*	*256K*	*7M*	*2W*
14	*1M*	*256K*	*256K*	*256K*	*7M*	*2W*
15	*1M*	*1M*	*0*	*0*	*8M*	*2W*
16	*256K*	*1M*	*1M*	*0*	*9M*	
17	*1M*	*1M*	*256K*	*0*	*9M*	*2W*
18	*1M*	*256K*	*1M*	*0*	*9M*	
19	*256K*	*256K*	*1M*	*1M*	*10M*	*2W*
20	*256K*	*1M*	*1M*	*256K*	*10M*	
21	*1M*	*1M*	*256K*	*256K*	*10M*	*2W*
22	*1M*	*256K*	*1M*	*256K*	*10M*	
23	*1M*	*1M*	*1M*	*0*	*12M*	*2W*
24	*256K*	*1M*	*1M*	*1M*	*13M*	*2W*
25	*1M*	*1M*	*1M*	*256K*	*13M*	*2W*
26	*1M*	*256K*	*1M*	*1M*	*13M*	*2W*

27	*1M*	*1M*	*1M*	*1M*	*16M*	*4W*

Configuration of Cache Memory

Consult your local dealer for configuring the cache memory. Improper configuration will make the system malfunction.

The cache memory is either 32KB or 64KB. 32KB is sufficient for general applications and the performance is improved when the size is increased to 64KB. 32KB cache memory requires four SRAMs and 64KB cache memory requires eight SRAMs. Make sure that the number of SRAMs is correct. Otherwise the system will not work. JP1, 2 and 3 are used to define the cache memory size. There is no mini-Jumper on JP3. JP3 is only used when the cacheable memory size is 16MB.

Line size is the number of bytes which will be fetched from main memory to cache memory at one time when a cache read miss occurs. A burst mode read mechanism is implemented in the memory controller so as to minimize the overhead of reading multiple bytes. So it is recommended to select line size to be 16 bytes.

The cacheable memory size is set to 8MB. To increase the size to 16MB, an additional SRAM (U16) is required and JP3 has to be set.

There are several jumpers to configure the cache memory.

Cache Memory Size

	32KB	*64KB*
JP1	*1-2*	*2-3*
JP2	*2-3*	*1-2*
JP3	*1-2*	*2-3*

Line Size

	4	*8*	*16*
JP4	*1-2*	*1-2*	*2-3*
JP5	*1-2*	*2-3*	*2-3*

Control of System Speed

System Speed can be controlled by hardware switch and keyboard. Connector P3 is connected to the turbo switch of the case. When the system speed is fast, the turbo LED of the case should be turned on.

To change the speed by keyboard, use '-' and '+' of the numeric keypad. Press 'Ctrl', 'Alt' and '-' for slow speed and Press 'Ctrl', 'Alt' and '+' for fast speed.

Whenever the system speed is set to slow by turbo switch, it cannot be changed by keyboard, and vice versa.

Reset CMOS Setup Information

Sometimes, the improper setting of system setup may make the system malfunction. In this case, turn off the power and place a jumper on JP11 for a while. The internal CMOS status register is reset. Then remove the jumper and turn on the power. The BIOS finds the CMOS status register is reset and regards the setup information is invalid. So it will prompt you to correct the information.

System Board Jumper Setting

There are several options which allows user to select by hardware switches.

JP8	
1-2	*Non-pipelined **
2-3	*Pipelined*

ROM Size

JP6	
1-2	*27512*
2-3	*27256 **

Display Selection

JP10	
ON	*CGA, EGA, VGA*
OFF	*Monochrome display **

*Note : * factory setting*

System Board Connectors

Under typical conditions, these connectors should be connected to the indicators and switches of the system unit.

Connector	*Function*
P1	*Hardware reset connector*
P2	*Speaker connector*
P3	*Turbo switch connector*
P4	*Turbo LED connector*
P5	*Power LED & Ext-Lock connector*
P6, P7	*Power supply connector*
P8	*External battery connector*
KB1	*Keyboard connector*

Pin assignment of the connector are illustrated as follows:

P 1 - Hardware Reset Connector

Pin	*Assignment*
1	*Selection Pin*
2	*Ground*

P 2 - Speaker Connector

Pin	*Assignment*
1	*Data out*
2	*+5 Vdc*
3	*Ground*
4	*+5 Vdc*

P 3 - Turbo Switch Connector

Pin	*Assignment*
1	*Selection Pin*
2	*Ground*

P 4 - Turbo LED Connector

Pin	*Assignment*
1	*+5 Vdc*
2	*LED signal*

P 5 - Power LED & Ext-Lock Connector

Pin	*Assignment*
1	*+5 Vdc*
2	*Key*
3	*Ground*
4	*Keyboard inhibit*
5	*Ground*

P6,P7 - Power Supply Connector

Pin	*Assignment*
1	*POWERGOOD*
2	*+5 Vdc*
3	*+12 Vdc*
4	*-12 Vdc*
5	*Ground*
6	*Ground*

Pin	*Assignment*
1	*Ground*
2	*Ground*
3	*-5 Vdc*
4	*+5 Vdc*
5	*+5 Vdc*
6	*+5 Vdc*

P 8 - External Battery Connector

Pin	*Assignment*
1	*+6 Vdc*
2	*not used*
3	*Ground*
4	*Ground*

KB 1 - Keyboard Connector

Pin	*Assignment*
1	*Keyboard clock*
2	*Keyboard data*
3	*Spare*
4	*Ground*
5	*+5 Vdc*

Chapter 4 TECHNICAL INFORMATION

This section provides technical information about OCTEK Pointer-386 and is intended for advanced users interested in the basic design and operation of OCTEK Pointer-386.

Memory Mapping

Address	*Range*	*Function*
000000-7FFFFF	*000K-512K*	*System Board Memory (512K)*
080000-09FFFF	*512K-640K*	*System Board Memory (128K)*
0A0000-0BFFFF	*640K-768K*	*Display Buffer (128K)*
0C0000-0DFFFF	*768K-896K*	*Adaptor ROM / Shadow RAM (128K)*
0E0000-0EFFFF	*896K-960K*	*System ROM / Shadow RAM (64K)*
0F0000-0FFFFF	*960K-1024K*	*System BIOS ROM / Shadow RAM (64K)*
100000-7FFFFF	*1024K-8192K*	*System Memory*
800000-FFFFFF	*8192K-16318K*	*System Memory*

I/O Address Map

I/O Address Map on System Board

I/O address hex 000 to 0FF are reserved for the system board I/O.

ADDRESS (HEX)	*DEVICE*
000-01F	*DMA Controller 1, 8237*
020-03F	*Interrupt Controller 1, 8259, Master*
040-05F	*Timer, 8254*
060-06F	*Keyboard Controller*
070-07F	*Real Time Clock, NMI (non-maskable interrupt) mask*
080-09F	*DMA Page Register, 74LS612*
0A0-0BF	*Interrupt Controller 2, 8259*
0C0-0DF	*DMA Controller 2, 8237*
0F0	*Clear Math Coprocessor Busy*
0F1	*Reset Math Coprocessor*
0F8-0FF	*Math Coprocessor Port*

I/O address hex 100 to 3FF are available on the I/O channel.

ADDRESS (HEX)	*DEVICE*
1F0-1F8	*Fixed Disk*
200-207	*Game I/O*
278-27F	*Parallel Printer Port 2*
2F8-2FF	*Serial Port 2*
300-31F	*Prototype Card*
360-36F	*Reserved*
378-37F	*Parallel Printer Port 1*
380-38F	*SDLC, bisynchronous 2*
3A0-3AF	*Bisynchronous 1*
3B0-3BF	*Monochrome Display and Printer Adapter*
3C0-3CF	*Reserved*
3D0-3DF	*Color Graphics Monitor Adapter*
3F0-3F7	*Diskette Controller*
3F8-3FF	*Serial Port 1*

System Timers

OCTEK Pointer-386 has three programmable timer/counters controlled by 82C206 and they are defined as channels 0 through 2:

Channel 0	*System Timer*
Gate 0	*Tied on*
Clk in 0	*1.190 MHz OSC*
Clk out 0	*8259 IRQ 0*

Channel 1	*Refresh Request Generator*
Gate 1	*Tied on*
Clk in 1	*1.190 MHz OSC*
Clk out 1	*Request Refresh Cycle*

Channel 2	*Tone Generation of Speaker*
Gate 2	*Controlled by bit 0 of port hex 61 PPI bit*
Clk in 2	*1.190 MHz OSC*
Clk out 2	*Used to drive the speaker*

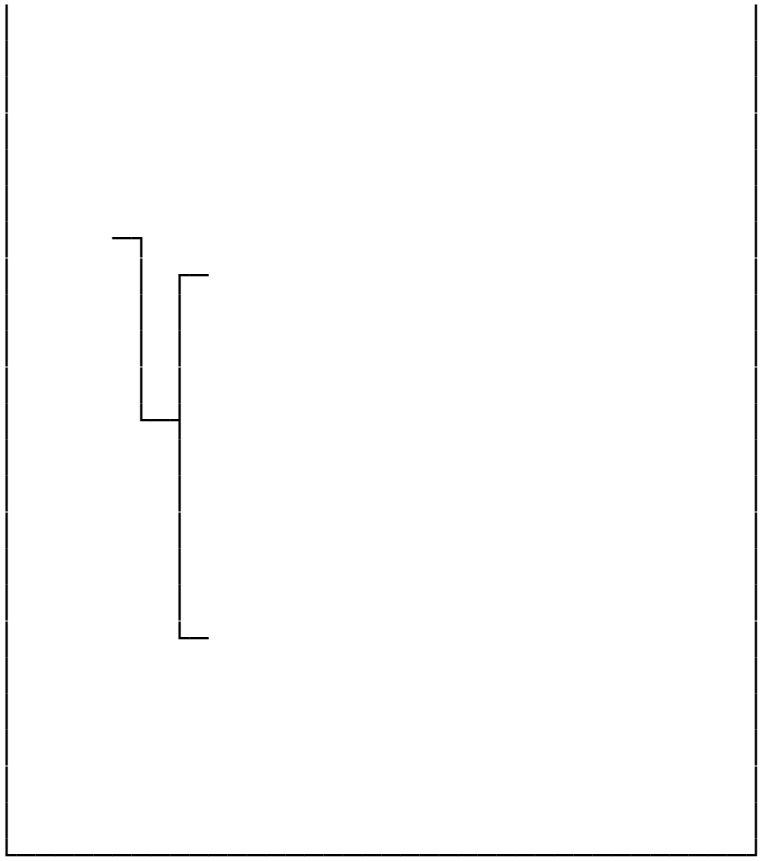
Note : Channel 1 is programmed to generate a 15-micro-second period signal.

The 8254 Timer/Counters are treated by system programs as an arrangement of four programmable external I/O ports. Three are treated as counters and the fourth is a control register for mode programming.

System Interrupts

Sixteen levels of system interrupts are provided on OCTEK Pointer-386. The following shows the interrupt-level assignments in decreasing priority.

Level		Function
Microprocessor NMI		*Parity or I/O Channel Check*
Interrupt Controllers		
CTLR 1	*CTLR 2*	
IRQ0		*Timer Output 0*
IRQ1		*Keyboard (Output Buffer Full)*
IRQ2		*Interrupt from CTLR 2*
	IRQ8	*Realtime Clock Interrupt*
	IRQ9	*Software Redirected to INT 0AH (IRQ2)*
	IRQ10	*Reserved*
	IRQ11	*Reserved*
	IRQ12	*Reserved*
	IRQ13	*Coprocessor*
	IRQ14	*Fixed Disk Controller*
	IRQ15	*Reserved*
IRQ3		*Serial Port 2*
IRQ4		*Serial Port 1*
IRQ5		*Parallel Port 2*
IRQ6		*Diskette Controller*
IRQ7		*Parallel Port 1*



Direct Memory Access (DMA)

OCTEK Pointer-386 supports seven DMA channels.

Channel	*Function*
0	*Spare (8 bit transfer)*
1	*SDLC (8 bit transfer)*
2	*Floppy Disk (8 bit transfer)*
3	*Spare (8 bit transfer)*
4	*Cascade for DMA Controller 1*
5	*Spare (16 bit transfer)*
6	*Spare (16 bit transfer)*
7	*Spare (16 bit transfer)*

The following shows the addresses for the page register

Page Register	*I/O Address (HEX)*
DMA Channel 0	*0087*
DMA Channel 1	*0083*
DMA Channel 2	*0081*
DMA Channel 3	*0082*
DMA Channel 5	*008B*
DMA Channel 6	*0089*
DMA Channel 7	*008A*
Refresh	*008F*

Real Time Clock and CMOS RAM

Real time clock and CMOS RAM are contained on board. Real time clock provides the system date and time. CMOS RAM stores system information. Both are backed up by battery and will not lose information after power off. The following page shows the CMOS RAM Address Map.

CMOS RAM Address Map

Addresses	*Description*
00-0D	** Real-time clock information*
0E	** Diagnostic status byte*
0F	** Shutdown status byte*
10	*Diskette drive type byte - drives A and B*
11	*Reserved*
12	*Fixed disk type byte - drives C and D*
13	*Reserved*
14	*Equipment byte*
15	*Low base memory byte*
16	*High base memory byte*
17	*Low expansion meory byte*
18	*High expansion memory byte*
19-2D	*Reserved*
2E-2F	*2-byte CMOS checksum*
30	** Low expansion memory byte*
31	** High expansion memory byte*
32	** Date century byte*
33	** Information flags (set during power on)*
34-3F	*Reserved*

Real Time Clock Information

The following table describes real-time clock bytes and specifies their addresses.

Byte	*Function*	*Address*
0	*Seconds*	*00*
1	*Second alarm*	*01*
2	*Minutes*	*02*
3	*Minute alarm*	*03*
4	*Hours*	*04*
5	*Hour alarm*	*05*
6	*Day of week*	*06*
7	*Date of month*	*07*
8	*Month*	*08*
9	*Year*	*09*
10	*Status Register A*	*0A*
11	*Status Register B*	*0B*
12	*Status Register C*	*0C*
13	*Status Register D*	*0D*

System Expansion Bus

OCTEK Pointer-386 provides eight 16-bit slots.

The I/O channel supports:

* *I/O address space from hex 100 to hex 3FF*
* *Selection of data access (either 8 or 16 bit)*
* *24 bit memory addresses (16MB)*
* *Interrupts*
* *DMA channels*
* *Memory refresh signal*

The following figure shows the pin numbering for I/O channel connectors J3 to J10.

The following figure shows the pin numbering for I/O channel connectors J13-J20.

The following tables summarize pin assignments for the I/O channel connectors.

I/O Channel (A-Side)

I/O Pin	Signal Name	I/O
A1	-I/O CH CK	I
A2	SD7	I/O
A3	SD6	I/O
A4	SD5	I/O
A5	SD4	I/O
A6	SD3	I/O
A7	SD2	I/O
A8	SD1	I/O
A9	SD0	I/O
A10	-I/O CH RDY	I
A11	AEN	O
A12	SA19	I/O
A13	SA18	I/O
A14	SA17	I/O
A15	SA16	I/O
A16	SA15	I/O
A17	SA14	I/O
A18	SA13	I/O
A19	SA12	I/O
A20	SA11	I/O
A21	SA10	I/O
A22	SA9	I/O
A23	SA8	I/O
A24	SA7	I/O

A25	*SA6*	*I/O*
A26	*SA5*	*I/O*
A27	*SA4*	*I/O*
A28	*SA3*	*I/O*
A29	*SA2*	*I/O*
A30	*SA1*	*I/O*
A31	*SA0*	*I/O*

I/O Channel (B-Side)

I/O Pin	*Signal Name*	*I/O*
B1	*GND*	*Ground*
B2	*RESET DRV*	*I*
B3	*+5 Vdc*	*Power*
B4	*IRQ9*	*I*
B5	*-5 Vdc*	*Power*
B6	*DRQ2*	*I*
B7	*-12 Vdc*	*Power*
B8	*0WS*	*I*
B9	*+12 Vdc*	*Power*
B10	*GND*	*Ground*
B11	*-SMEMW*	*O*
B12	*-SMEMR*	*O*
B13	*-IOW*	*I/O*
B14	*-IOR*	*I/O*
B15	*-DACK3*	*I*
B16	*DRQ3*	*O*
B17	*-DACK1*	*I*
B18	*DRQ1*	*O*
B19	*-Refresh*	*I/O*
B20	*CLK*	*O*
B21	*IRQ7*	*I*
B22	*IRQ6*	*I*
B23	*IRQ5*	*I*
B24	*IRQ4*	*I*
B25	*IRQ3*	*I*
B26	*-DACK2*	*O*
B27	*T/C*	*O*

B28	*BALE*	*O*
B29	*+5 Vdc*	*Power*
B30	*OSC*	*O*
B31	*GND*	*GROUND*

I/O Channel (C-Side)

I/O Pin	*Signal Name*	*I/O*
C1	*SBHE*	*I/O*
C2	*LA23*	*I/O*
C3	*LA22*	*I/O*
C4	*LA21*	*I/O*
C5	*LA20*	*I/O*
C6	*LA19*	*I/O*
C7	*LA18*	*I/O*
C8	*LA17*	*I/O*
C9	*-MEMR*	*I/O*
C10	*-MEMW*	*I/O*
C11	*SD8*	*I/O*
C12	*SD9*	*I/O*
C13	*SD10*	*I/O*
C14	*SD11*	*I/O*
C15	*SD12*	*I/O*
C16	*SD13*	*I/O*
C17	*SD14*	*I/O*
C18	*SD15*	*I/O*

I/O Channel (D-Side)

I/O Pin	*Signal Name*	*I/O*
D1	*-MEM CS16*	*I*
D2	*-I/O CS16*	*I*
D3	*IRQ10*	*I*
D4	*IRQ11*	*I*
D5	*IRQ12*	*I*
D6	*IRQ15*	*I*
D7	*IRQ14*	*I*
D8	*-DACK0*	*O*
D9	*DRQ0*	*I*
D10	*-DACK5*	*O*
D11	*DRQ5*	*I*
D12	*-DACK6*	*O*
D13	*DRQ6*	*I*
D14	*-DACK7*	*O*
D15	*DRQ7*	*I*
D16	*+5 Vdc*	*Power*
D17	*-MASTER*	*I*
D18	*GND*	*Ground*

APPENDIX A SYSTEM BIOS

The system BIOS provides an interface for operating systems and applications to access hardware. It also performs self-test after reset and includes a setup program to configure the system.

Self-test

To ensure the computer hardware is functional, the system BIOS will carry out a self-test upon reset. The test is very intensive and covers all parts of hardware. It takes a while before some messages are shown on the screen. It does not mean that the system is not working when the screen is blank. After completing the self-test, the BIOS will display some messages on the screen.

Unlike most of the tests which take a short time, the memory test may be very slow, especially when the memory size is large. Therefore the system BIOS allows you to bypass the memory test by pressing 'ESC'. The following message will be shown during memory test:

Press <ESC> Key to bypass MEMORY test

The total memory size is displayed after the test.

In case of serious errors, the BIOS will suspend the test. If the display is not initialized, the BIOS will report the error through a sequence of beeps. Otherwise, error message will be shown on the screen.

System Setup

The BIOS incorporates two setup sections:

(1) CMOS SETUP
(2) EXTENDED SETUP PROGRAM

It is important that all setup procedures should be completed before operating the system. Otherwise, the system will not run properly with the incorrect setup information. Run the setup again if the configuration is changed.

To enter the setup section, press 'Del' when the following message is shown:

Press <Del> if you want to run SETUP/EXTD-SET

Whenever the system BIOS find that the configuration of the system is altered, error message will be shown and you may press 'F1' to run setup.

In CMOS SETUP section, you can enter system configuration information which will be stored in CMOS RAM on the motherboard. The information include the devices of the system as well as memory size.

EXTENDED SETUP PROGRAM allows you to configure the registers of the chipsets. These registers are programmed with default settings by the BIOS. You may change the setting to improve performance or to suit the system configuration. Improper setting the registers may make the system malfunction. Consult your dealer if you have any doubt.

SECTION 1 CMOS SETUP

The memory size and the numeric processor are detected by the BIOS. So you are only required to set those options on the left side of the screen. The system configuration information are shown as follows:

OPTION 1 TIME AND DATE

Use PgUp and PgDn keys to change the value. The date and time cannot be entered directly.

OPTION 2 FLOPPY DISK DRIVE

Four types of floppy disk drives are supported:

1. *5-1/4 inch standard drive (360K)*
2. *5-1/4 inch high-density drive (1.2M)*
3. *3-1/2 inch standard drive (720K)*
4. *3-1/2 inch high-density drive (1.44M)*

Select the correct types. Otherwise the drives cannot work properly. The system BIOS supports two floppy disk drives and they are recognized as drive A and B. If one of them is not installed, select 'Not Installed' for that drive. The BIOS is able to detect the type of the drives. But remember to check the settings before exit.

There are 47 types of fixed disks supported by the BIOS. Consult your fixed disk manual to determine its correct type. The parameters such as cylinder number, head number, sector number and pre-compensation must be matched with your fixed disk.

Use PgUp and PgDn keys to change the fixed disk type. If the type of your fixed disk is not listed, define a new type as type 47. Use left and right arrow keys to move between the parameter fields and enter the parameters. The parameters will be stored in the CMOS RAM and your fixed disk can be used afterwards.

If the type of fixed disk is wrong, it takes a while before the BIOS can identify the error. After setting the fixed disk type, if the system halts after reboot, please wait for a while. It is most likely that the setting of fixed disk type is incorrect.

Some fixed disks are specially handled and must be set to 'Not Installed'. Consult the fixed disk manual for details.

OPTION 4 DISPLAY

Four types of display are supported:

1. *CGA 80 column mode*
2. *CGA 40 column mode*
3. *EGA and VGA*
4. *Monochrome*

If the type of display is incorrect, the BIOS will prompt you and ask you to set up again. But the BIOS is still able to display messages on the display attached to the system. Thus you can enter the setup program.

OPTION 5 KEYBOARD

If a keyboard is attached to the system, select 'Installed'. The BIOS will test the keyboard during self-test.

OPTION 6 Scratch RAM

The BIOS may require some storages for certain functions and this storage can be allocated in two ways. One way is to use the BIOS stack and another is to allocate a 1K bytes memory in the base memory. Generally, the former option is appropriate. If the hard disk type 47 is defined or if you run program like OS/2 which will use 80386 instruction, select the option 2.

SECTION 2 EXTENDED SETUP PROGRAM

All the registers of the chipset are set to default values. Usually, you need not modify these registers unless the configuration is changed. Since improper settings of these registers may make the system malfunction, check your settings before exit.

Select 'Write CMOS register and exit' to save the new settings in the CMOS RAM. The BIOS will then reboot the system and the new settings are in effect afterwards.

There are two ways to program the registers: advanced setup and easy setup. Advanced setup is more complicated and you have to program the registers bit by bit. In advanced setup, use arrow keys to move the cursor between each field. The corresponding explanation is displayed for your reference.

In most cases, the easy setup is adequate and simple to use. There are four groups of selections:

(1) Clock
(2) Wait state
(3) Shadow RAM and remap
(4) Cache controller

In this section, you simply use the up and down arrow keys to move between selections and press 'Enter' to select. The BIOS will set the registers accordingly.

(1) Clock

CPU clock

When set to CLKIN, the CPU will run at 33MHz for 66MHz oscillator or 25MHz for 50MHz oscillator. If ICLK is selected, the CPU will run at low speed.

ICLK clock

ICLK is used by peripherals on the motherboard and slots, such as display and DMA. If normal speed mode is enabled, the CPU will use ICLK clock.

	CPU Speed	
ICLK	*33 MHz*	*25 MHz*
CLKIN/4	*8.25*	*6.25*
CLKIN/3	*11.00*	*8.33*
CLKIN/2	*16.50*	*12.50*

To be compatible with add-on cards, the ICLK must be 8.33 MHz or less.

ATCLK stretch

When enabled, the performance is further improved. Nevertheless, compatibility problem may arise. Check with your configuration before permanently enabling this feature.

(2) Wait state

The number of wait state for memory read and write operations depends on the speed of CPU and DRAM.

	Number of	wait state
CPU speed	1	0
25 MHz	100ns	70ns
33 MHz	80ns	60ns

(3) Shadow RAM and remap

640K bytes is allocated for base memory. There are 384K bytes left below 1M. This part of memory is divided into three partitions: allocated for system BIOS shadow RAM, allocated for video BIOS shadow RAM and 256K bytes unused. The unused partition can be remapped to other address. Usually enable the remapping function.

(4) Cache Controller

There are four selections:

Cache enable/disable
Cache controller
256KB remapped area cached enabled/disabled
Cacheable address range

The cache controller is incorporated in the chipset and can be disabled.

256KB remapped area is located at a new address. Select 'enable' to inform the cache controller to include this area in the cacheable area.

Cacheable address range should be equal to the memory size on board.

APPENDIX B SYSTEM LAYOUT DIAGRAM