User's Manual

Model P5000HX Series CPU

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This equipment has been tested and found to comply with the limits for a Class A digital device pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference, in which case the user will be required to correct the interference at the user's own expense.

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Changes or modifications not expressly approved by Texas Microsystems could void the product warranty and the user's authority to operate the equipment.

This product also meets requirements for compliance with EN55022, Class B ITE.

Table of Contents

1 Introduction to the P5000HX Series CPU

Thank you for purchasing Texas Micro's P5000HX Series CPU. This chapter:

- introduces the primary features of the P5000HX, and
- discusses the PCI backplane and PICMG.

If you wish to configure and install your P5000HX quickly and you are familiar with P5000HX features and PCI concepts, go directly to Chapter 2, then read this chapter at your convenience.

1.1 P5000HX Features

The P5000HX

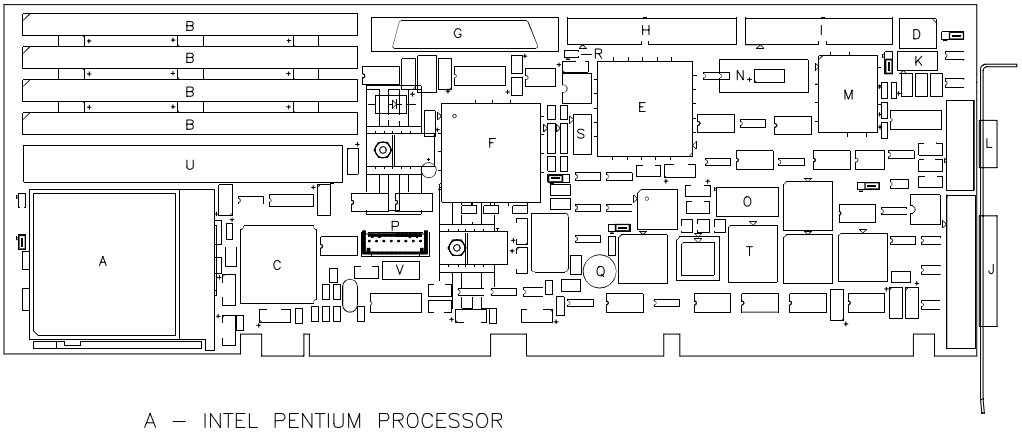
The Texas Micro P5000HX:

- provides a 100/133/166/200 MHz, 64-bit Pentium P54C processor,
- contains on-board PCI peripheral devices such as SCSI and EIDE, and
- features 512 KByte flash memory and a CELP socket for optional high-speed pipelined burst SRAM modules (up to 512 KBytes).

Additional features include...

- Support for up to 256 MByte scaleable FPM DRAM (chip set allows ECC using standard SIMMs),
- One RS-232 serial port, one programmable RS-232/422/485 serial port,
- a multi-function enhanced IEEE 1284 parallel port,
- a floppy disk controller,
- an EIDE hard disk controller , and
- a PCI Bus-to-Fast and Wide SCSI Controller.

FIGURE 1 P5000HX components



A – INTEL PENTIUM PROCESSOR
B – SIMM SOCKETS
C – PCI/CACHE/MEMORY CONTROLLER
D – DIP SWITCH BLOCK
E – PCI/ISA/EIDE CONTROLLER
F – ADAPTEC AIC–7870 PCI BUS MASTER WIDE SCSI CONTROLLER
G – SCSI DEVICE CONTROLLER CABLE HEADER
H – EIDE DRIVE CONTROLLER CABLE HEADER
I – FLOPPY DRIVE CONTROLLER CABLE CONNECTOR
J – PARALLEL PORT CONNECTOR
K – SERIAL PORT 2 CONNECTOR
L – SERIAL PORT 1 CONNECTOR
M – INTEL 82091 ADVANCED INTEGRATED PERIPHERAL (AIP)
N – DS 12887 REAL–TIME CLOCK
O – FLASH DEVICE
P – AT KEYBOARD, RESET, KEYBOARD LOCK
Q – SPEAKER
R – EIDE/SCSI CONNECTOR
S – PS/2 MOUSE CONNECTOR
T – AUX BIOS
U – CELP FOR COAST L2 CACHE
V – KEYBOARD POLYFUSE

1.2 A PCI Discussion

Overview

The P5000HX is designed to be used with either an ISA or a PCI backplane. This section discusses the PCI Local Bus.

The PCI Local Bus

The PCI Local Bus is a high-performance, 133 MB/sec, 32-bit bus with multiplexed address and data lines. It is intended for use as an interconnect mechanism between highly-integrated peripheral controller components, add-in boards, and processor/memory systems.

Why the PCI Local Bus?

Graphics-oriented operating systems such as Windows and OS/2 have created a data bottleneck between the processor and its display peripherals in standard PC I/O architectures. Moving peripheral functions with high-bandwidth requirements closer to the system's processor bus can eliminate this bottleneck.

Substantial performance gains are seen with graphical user interfaces (GUI's) and other high-bandwidth functions (i.e., full-motion video, SCSI, LANs, etc.) when a "local bus" design is used.

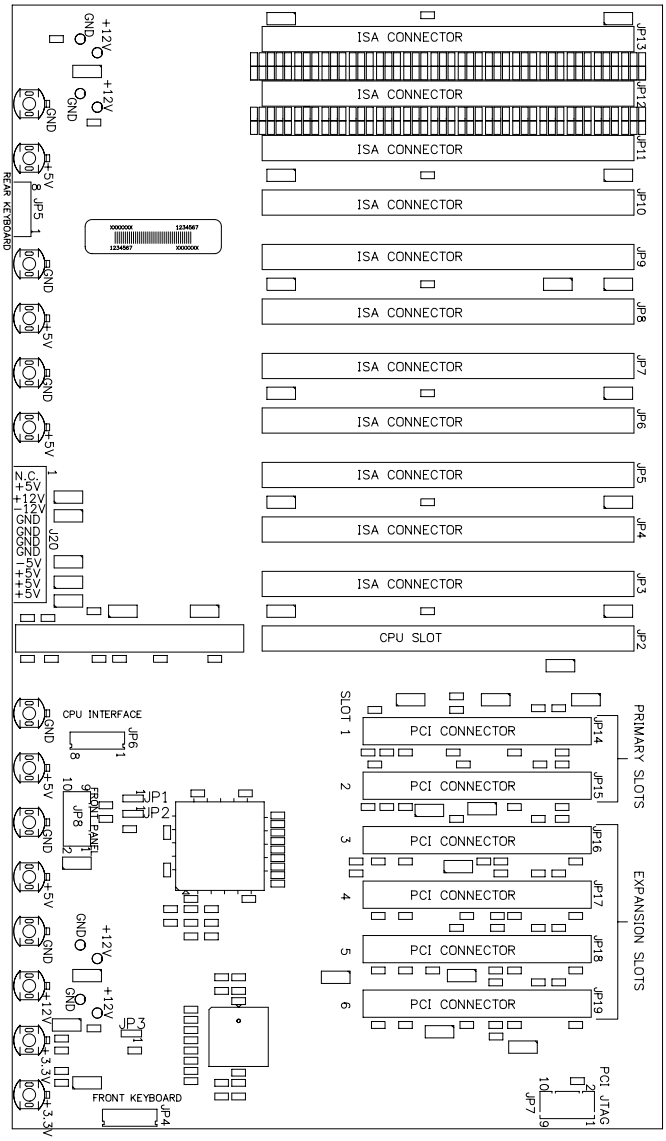
The PCI Bridge

The processor/cache/memory subsystem in a PCI system is connected to PCI through a "PCI Bridge." This bridge provides a low-latency path through which the processor may directly access PCI devices mapped anywhere in the memory or I/O address spaces. It also provides a high-bandwidth path, allowing PCI masters direct access to main memory.

PICMG

Texas Microsystems is a founding member of the PICMG (PCI Industrial Computer Manufacturers Group), founded to develop standards for PCI-based passive backplane systems. The P5000HX is fully PICMG-compliant.

FIGURE 2 A sample PCI backplane (Texas Micro's 18-slot version)



This chapter covered...

- P5000HX features
- basic P5000HX components
- the PCI Local Bus and Bridge
- PICMG

Next...

The next chapter outlines the seven basic steps for P5000HX configuration and installation.

2

7 Steps to P5000HX Operation

This chapter provides some basic precautions for handling the P5000HX, then outlines the seven basic steps for configuring and installing the P5000HX Series CPU:

1. Check jumper settings,
2. Check switch settings,
3. Connect peripherals to headers,
4. Install the board,
5. Attach peripherals to connectors,
6. Power-up the system, and
7. Run the Setup Utility.

2.1 Handling the P5000HX

Overview

This section provides basic precautions for handling the P5000HX CPU.

Static electricity

The P5000HX features ESD (electro-static discharge) and over-voltage protection circuitry built into the board's design to protect the I/O ports. However, excessive static electricity can damage P5000HX components.

Use the provided grounding wrist strap to discharge static electricity before you handle the board. Instructions for using the wrist strap are printed on the strap envelope. Always handle the board by the edges to help eliminate accidental static damage.

Safety considerations

It is important to protect yourself and your equipment before you perform any of the following procedures. **Never touch the P5000HX while it is installed in the chassis and power is ON.**

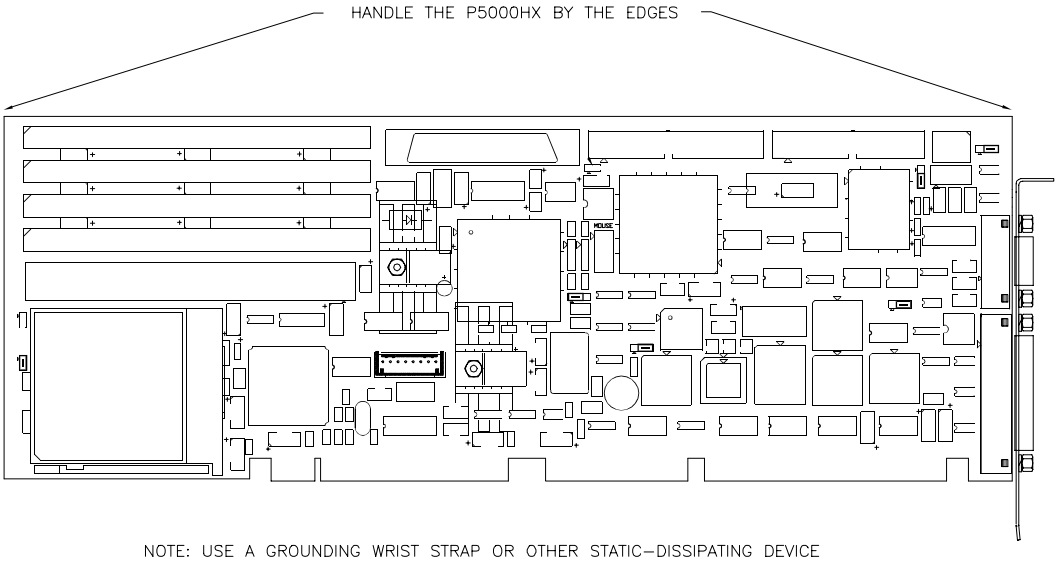
You should check the P5000HX configuration before you install the board. However, if the P5000HX is already installed in your system, remove power by turning all power switches OFF and disconnecting all power cords from their power sources. Follow all safety precautions outlined by the chassis manufacturer.

Only qualified, experienced electronics personnel should access the unit's interior.

Next...

Before you install the P5000HX, check the jumper and DIP switch settings outlined in Section 2.2 and Section 2.3, respectively. Pay particular attention to the switch settings; the jumpers are preconfigured at the factory and are appropriate for most applications.

FIGURE 3 Handling the P5000HX



2.2 Step 1 - Check Jumper Block Settings

Overview

The first step in configuring the P5000HX is checking the jumper settings on the board.

What are jumpers?

Jumpers are small metal "bridges" that connect pins in a **jumper block** on a CPU board. The position of a jumper affects the board's operational parameters.

Jumper blocks

The P5000HX contains:

- five (5) three-pin jumper blocks (JP2, JP3, JP4, JP5 and JP7), and
- two 2) two-pin jumper blocks (JP6 and JP8).

Settings

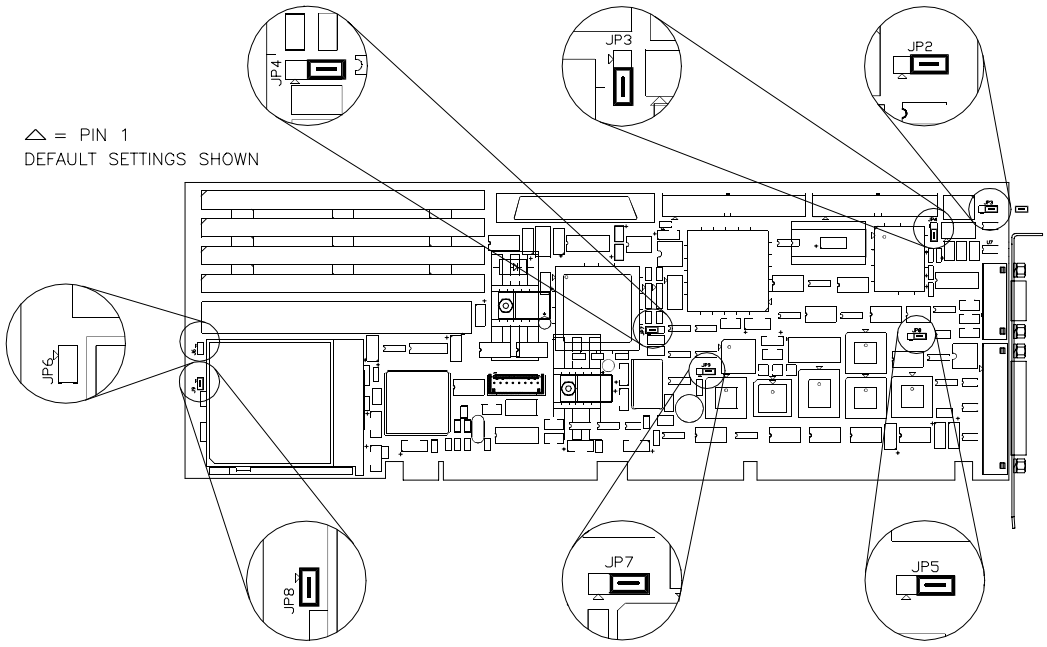
Settings for these jumper block are provided in the following tables.

3-pin Jumper Block Configuration		
JP2, JP3, JP5	**UART 2 Configuration**	
	Pin 2 jumpered to Pin 3	**RS232 configuration (default)**
	Pin 1 jumpered to Pin 2	RS422/485 configuration
JP4	**Watchdog Timer**	
	Pin 1 jumpered to Pin 2	Watchdog timer reset active enabled
	Pin 2 jumpered to Pin 3	**Watchdog timer reset inactive (default)**
JP7	**Next Step OS Configuration**	
	Pin 1 jumpered to Pin 2	When running Next Step OS and experiencing operational problems with the PS/2 mouse, use this setting.
	Pin 2 jumpered to Pin 3	**Normal operation (default).**

Bus/Processor Speed Table

JP6 jumper installed?	JP8 jumper installed?	Bus Core Frequency Ratio	Bus/Processor Speed
Yes	Yes	2/5	66/166
Yes	No	1/3	66/200
No	Yes	1/2	66/133 (default)
No	No	2/3	66/100

FIGURE 4 Jumper Block locations



Note: Only experienced personnel should change these jumper settings. The P5000HX is very sensitive to static discharge and can be damaged if precautions are not taken. See Section 2.1 on page 12 for more information.

2.3 Step 2 - Check Switch Settings

Overview

After you check the jumper settings, check the switch block for proper configuration.

Switch block

The switch block (see Figure 5) contains four (4) DIP switches that can be configured to affect the following:

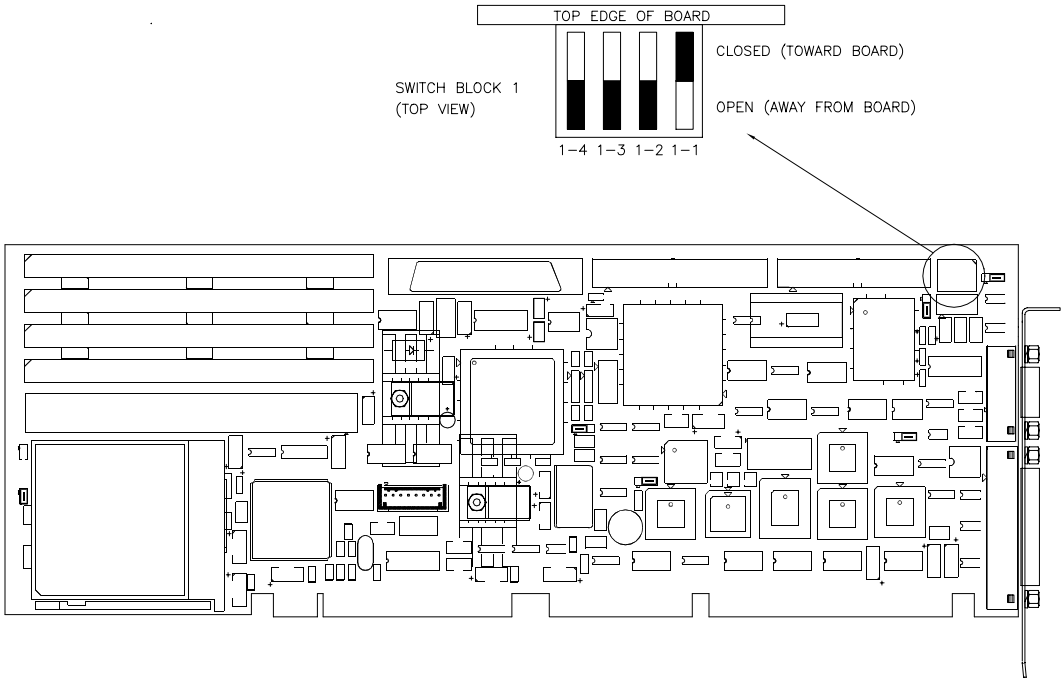
- default monitor type (SW1-1),
- on-board ROM access (SW1-2),
- CMOS RAM (SW1-3), and
- configuration ports (SW1-4).

Settings

Settings for the switches are provided below.

Switch	Setting	Result
SW1-1	Open	Monochrome monitor position
	Closed (default)	**Color monitor position**
SW1-2	**Open (default)**	**Flash memory is enabled; auxiliary ROM is disabled**
	Closed	Auxiliary ROM is enabled; Flash memory is disabled.
SW1-3	**Open (default)**	**Normal operation of the CMOS RAM**
	Closed	Used is special cases when the CMOS RAM becomes corrupted. When this switch is CLOSED, the factory default values for the Setup Utility are reloaded into CMOS RAM.
SW1-4	**Open (default)**	**Configuration ports are mapped to I/O addresses 270/271. Under normal conditions, this switch should remain open.**
	Closed	Configuration ports are mapped to I/O addresses 370/371.

FIGURE 5 Switch block location



Note: The P5000HX is very sensitive to static discharge and can be damaged if precautions are not taken. See Section 2.1 on page 12 for more information.

2.4 Step 3 - Connect Peripherals to Headers

Overview

The next step in installing your P5000HX is connecting peripherals to the on-board headers.

Headers

Headers are peripheral connectors located on the board's surface (as opposed to **connectors**, which are located on the I/O bracket, and are discussed in Section 2.6 on page 28).

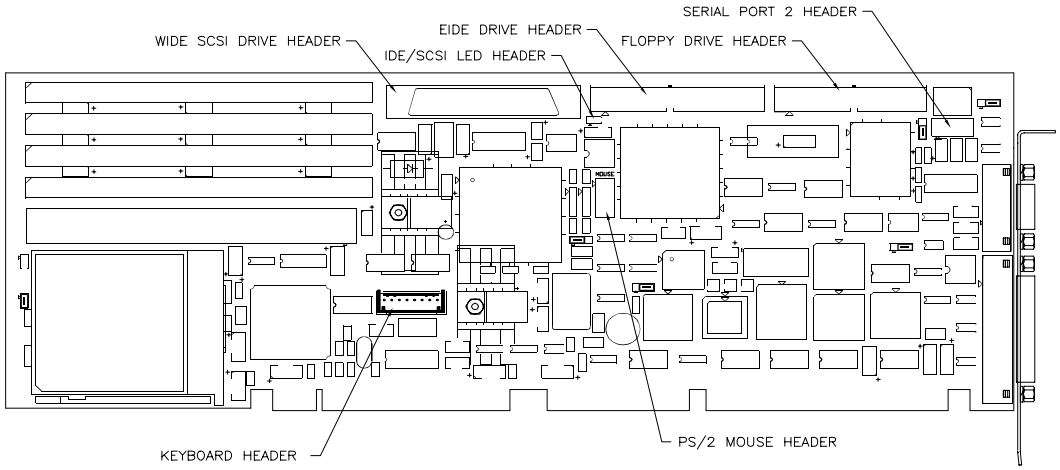
The P5000HX features the following headers for peripheral connection:

- a PCI-Bus-to-Fast and Wide SCSI controller,
- an EIDE drive header,
- an IDE/SCSI drive LED header,
- a floppy drive header,
- a serial port header (Serial Port 2),
- an AT-style keyboard header, and
- a PS/2 mouse header.

Descriptions

Descriptions of each of these headers are provided on page 20 through page 24.

FIGURE 6 P5000HX header locations



Note: The P5000HX is very sensitive to static discharge and can be damaged if precautions are not taken. See Section 2.1 on page 12 for more information.

Step 3 (cont.) - Connect Peripherals to Headers

Wide SCSI Drive Header

Up to seven (7) Small Computer System Interface (SCSI) hard disk drives can be attached to the P5000HX via this header and a 68-conductor cable. SCSI devices are daisy-chained via this cable, and both ends of the cable are terminated. Terminators can be connected to either SCSI devices or SCSI cables.

Devices connected to these chains must contain the correct number of terminators for proper operation. No more than two (2) terminators can exist in a chain of SCSI devices - one at each end of the physical chain.

If more than two SCSI devices are connected in a SCSI daisy-chain, the termination must be removed from the middle device(s) in the control cable.

EIDE Drive Header

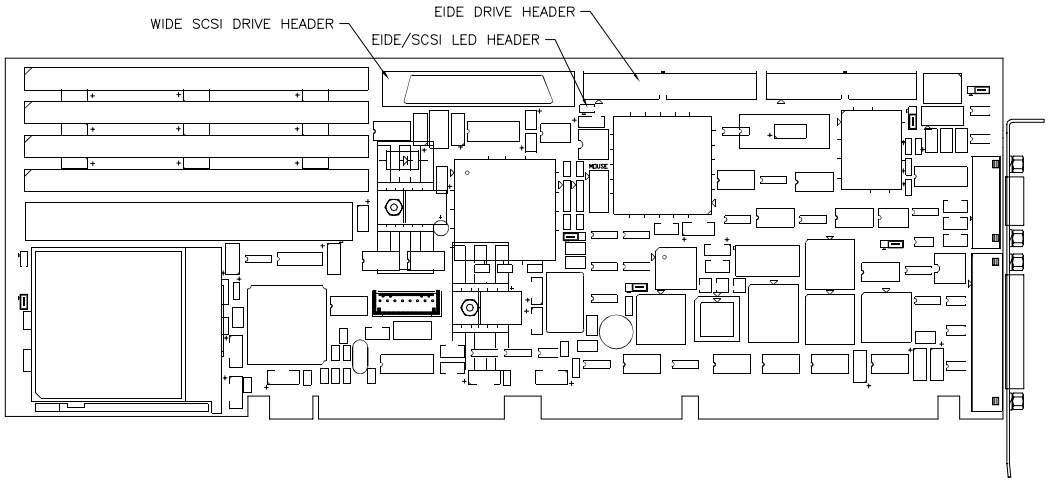
Two (2) Integrated Device Electronics (EIDE - backwards-compatible with IDE) hard disk drives can be attached to the P5000HX board via this header and a 40-conductor cable.

Note: The "red stripe" on the 40-pin cable should be near Pins 1 and 2 on the 40-pin connector. The IDE hard drive(s) will not work correctly if the cable is plugged in backwards.

IDE/SCSI Drive LED Header

This header provides an interface for the IDE/SCSI drive's activity LED cable. Pin 1 is the anode; Pin 2 is the cathode.

FIGURE 7 SCSI, EIDE, and LED headers



Step 3 (cont.) - Connect Peripherals to Headers

Floppy Drive Header

Two (2) floppy drives can be attached to the P5000HX via this header and a 34-conductor flat cable no more than three (3) feet in length.

Note: The "red stripe" on the 34-pin cable should be near Pins 1 and 2 on the 34-pin header. The floppy drive(s) will not work correctly if the cable is plugged in backwards.

The two installed drives may be any combination of:

- 360 KB and 1.2 MB 5.25" drives, or
- 720 KB, 1.44 MB, and 2.88 MB 3.5" drives.

Serial Port 2

Serial ports allow you to connect serial devices (a serial mouse, serial printers, etc.) to the P5000HX via appropriate serial cables. Serial ports are also known as UART (Universal Asynchronous Receiver/Transmitter) ports.

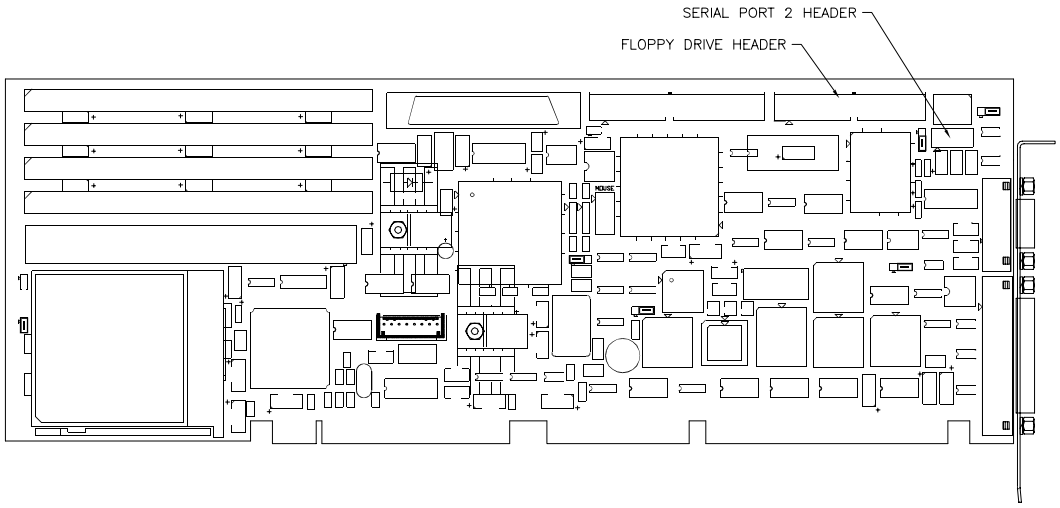
Note: The P5000HX uses 16550 UART's.

UART 2, the "second serial port," is a 10-pin header located on the card's front surface. **Be sure to use the proper cable when connecting a serial device to the P5000HX. If connecting a serial mouse to this port, use a shielded cable.**

Note that the other serial port (UART 1) is located on the edge of the card (on the I/O bracket). More information about this port can be found in Section 2.6 on page 28.

Note: The "red stripe" on the 10-pin cable should be near Pins 1 and 2 on the 10-pin header. Damage to the CPU/cable/external device can occur if the cable is plugged in backwards..

FIGURE 8 Floppy drive and Serial Port 2 headers



Step 3 (cont.) - Connect Peripherals to Headers

Keyboard Cable Header

The P5000HX provides an AT-style 8-pin keyboard cable header. See Figure 9 for location.

The sockets on the Texas Micro keyboard connector cable are numbered in reverse order when compared to the pinout of the P5000HX keyboard cable header. For example, Position 8 of the connector cable corresponds with Pin 1 of the header, Position 7 of the cable corresponds with Pin 2 of the header, etc.

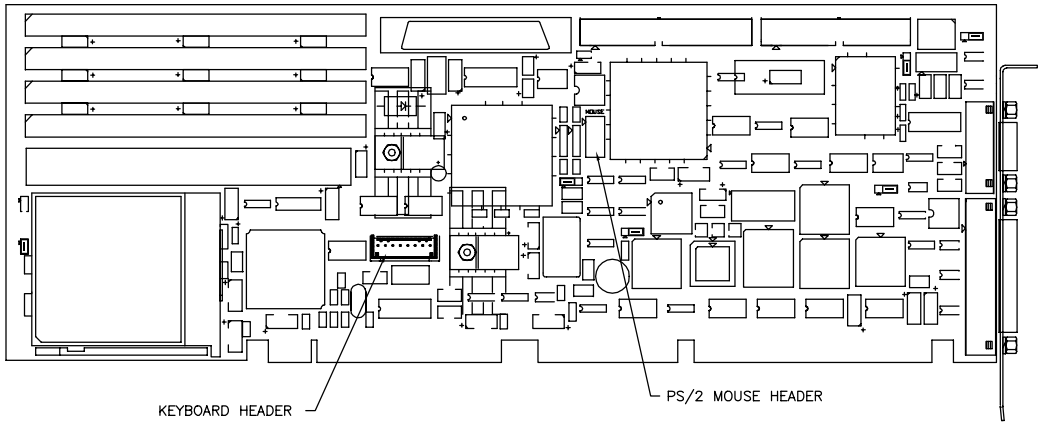
PS/2 Mouse Header

A 10-pin (2x5) header allows connection with a cable adapter to a PS/2 mouse connector.

Next...

After you've connected all desired peripherals to on-board headers, install the board as described on page 26.

FIGURE 9 Keyboard and PS/2 Mouse headers



2.5 Step 4 - Install the Board

Installation Procedure

The procedure for installing the P5000HX into a typical Texas Micro chassis is described below.

Step #	Action
1	Remove power from the chassis and disconnect all power cords. Use the provided grounding wrist strap to discharge static electricity, which can damage components. Follow all power-down procedures outlined in your chassis' user's guide.
2	Remove the chassis cover, then detach the circuit card hold-down bracket (if required). This bracket stretches across the tops of the circuit cards and holds them in place.
3	(For PCI operation; otherwise skip to step 4) Locate the "platform" or "CPU" slot. If the CPU is installed in another slot, it will be unable to communicate with any third-party PCI adapter cards.
4	Remove the I/O bracket spacer from the rear of the chassis (if required). This spacer occupies the area where the card's I/O bracket is accessed through the back of the chassis.
5	Ensure that you've connected all desired peripherals to the P5000HX on-board headers as outlined in Section 2.4.
6	Place the board ends into the appropriate card guide and card-end slot in the chassis. Lower the board into position and carefully push the card-edge connector into the slot. Ensure that the I/O bracket is accessible through the back of the chassis.
7	Secure the card-edge I/O bracket to the hold-down lip and attach any other cables to the P5000HX.

Next...

Attach desired peripherals to P5000HX connectors as outlined on page 28.

Note: To install the P5000HX into a passive backplane not manufactured by Texas Micro, follow the instructions provided by the backplane manufacturer. *If the P5000HX is installed in a non-Texas Micro chassis, a custom cable might be needed to adapt the keyboard connector to the wiring in the non-Texas Micro chassis. Texas Micro is unable to create such a cable.*

2.6 Step 5 - Attach Peripherals to Connectors

Overview

Connectors are also used to connect external components to the P5000HX, but, unlike headers, connectors are located on the I/O bracket at the end of the P5000HX board (which will make them accessible after you install the board). These include:

- a serial port connector ("SERIAL PORT 1") and
- a parallel port connector.

Serial Port 1

As mentioned earlier, serial ports allow you to connect serial devices (a serial mouse, serial printers, etc.) to the P5000HX via appropriate serial cables. Serial ports are also known as UART (Universal Asynchronous Receiver/Transmitter) ports.

Note: The P5000HX uses 16550 UART's.

SERIAL 1 is a 9-pin connector located on the edge of the card (on the I/O bracket). This means that you can access SERIAL 1 through the back of the chassis after the P5000HX is installed.

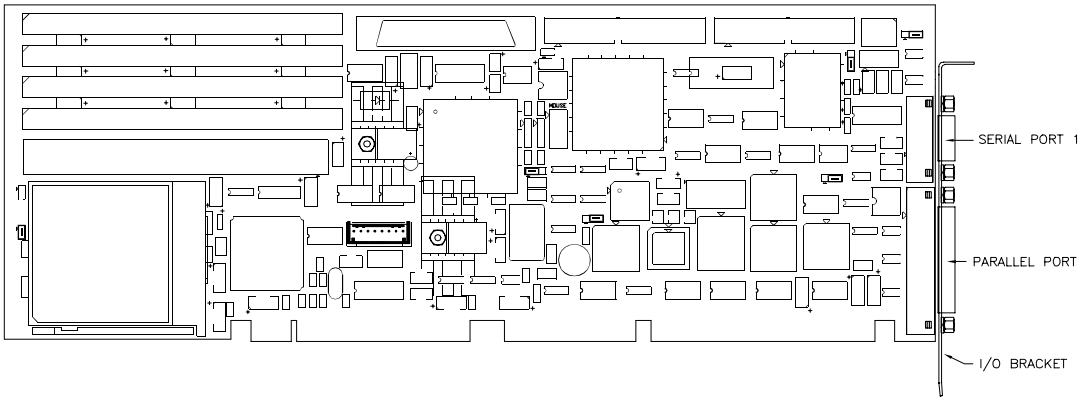
Parallel Port

The parallel port (IEEE1284, ECP/EPP/bidirectional) is normally used for connecting a printer to the P5000HX. This port is a 25-pin connector located on the I/O bracket. Connect the printer cable to this port for printer operation.

Next...

Power up the system as outlined on page 30.

FIGURE 10 Serial Port 1 and Parallel Port



2.7 Step 6 - Power-up the System

Overview

After all switches and jumpers have been checked and peripherals have been connected, turn on the power to your system. If the P5000HX has been properly installed, a power-up banner will be displayed and a power-up memory test will run.

Accessing the Setup Utility

If desired, you can now access the P5000HX Setup Utility. The Setup Utility can be accessed by pressing F2 when prompted by the BIOS during the power-up operation.

Next...

Turn to Section 2.8 on page 32 for instructions on using the P5000HX Setup Utility.

FIGURE 11 Setup Utility access

To access Setup, press...	When?
the “F2” key	When prompted by the BIOS

This screen will be displayed (sample configuration)...

Texas Microsystems, Inc. Setup Utility Copyright (c) 1988-1996
Model P5000HX BIOS Version x.x.x

Basic Options

Time and Date
Floppy Disks
Fixed Disks
Keyboard
Shadow RAM
Boot Options
Password Edit

Advanced Options
PCI Options

Time 10:18:28
Date..... July 1, 1996
Weekday..... Monday

Drive A:..... 3 1/2 Inch, 2.88 MB
Drive B:..... Not Installed
Hard Disk 1..... Type 40 is 514 MB
Hard Disk 2..... Not Installed

Keyboard Typematic Delay..... 250 msec
Keyboard Typematic Rate ..... 30 char/sec
Base Memory 640K
Extended Memory 007168K
Floating Point Unit ..... Operational
Boot Drive Sequence ..... Drive A:, then C:
101-Keyboard NumLock..... Disabled
Boot Option ..... Diagnostic Boot

↑ (prev) ↓ (next) F5 (color) Esc (reboot) Enter (execute)

2.8 Step 7 - Run the Setup Utility

Overview

The P5000HX Computer BIOS (**B**asic **I**nput/**O**utput **S**ystem) Setup Utility is a special set of functions used to set the computer time, date and configuration data.

Access

As described on page 30, the Setup Utility can be accessed by pressing F2 when prompted by the BIOS during the power-up operation.

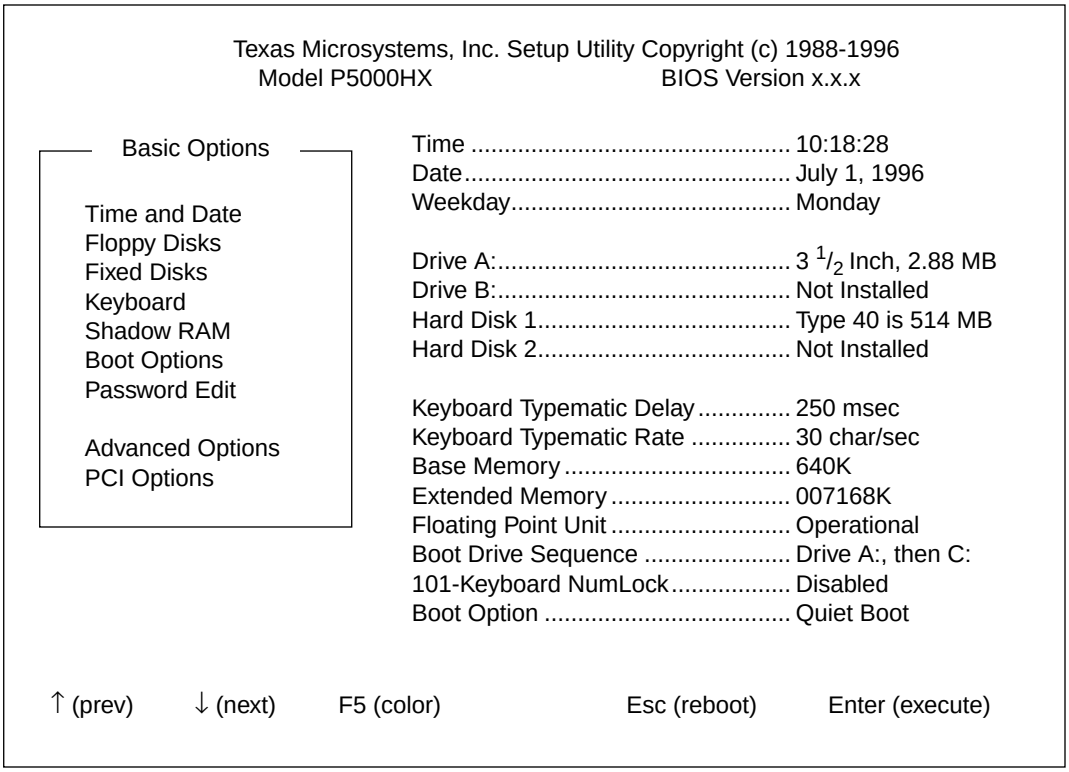
Main Menu

The Setup Utility begins by displaying the Main Menu screen pictured in Figure 12.

Next...

Turn to page 34 for information on the Main Menu.

FIGURE 12 The P5000HX Setup Utility (sample configuration)



Step 7 (cont.) - Run the Setup Utility (The Main Menu)

Overview

The Main Menu, the first screen displayed by the Setup Utility, is comprised of two basic components:

- the Basic Options Menu and
- the summary information area.

Basic Options

The Basic Options Menu is located on the left side of the screen. It contains a list of system parameters you can modify to meet your system requirements. Use these keys:

To...	Press...
move the cursor up	UP ARROW
move the cursor down	DOWN ARROW
select an item for modification	ENTER
save settings and reboot	ESC

Summary

The “summary information” area displays current system settings information and is located to the right of the Options Menu.

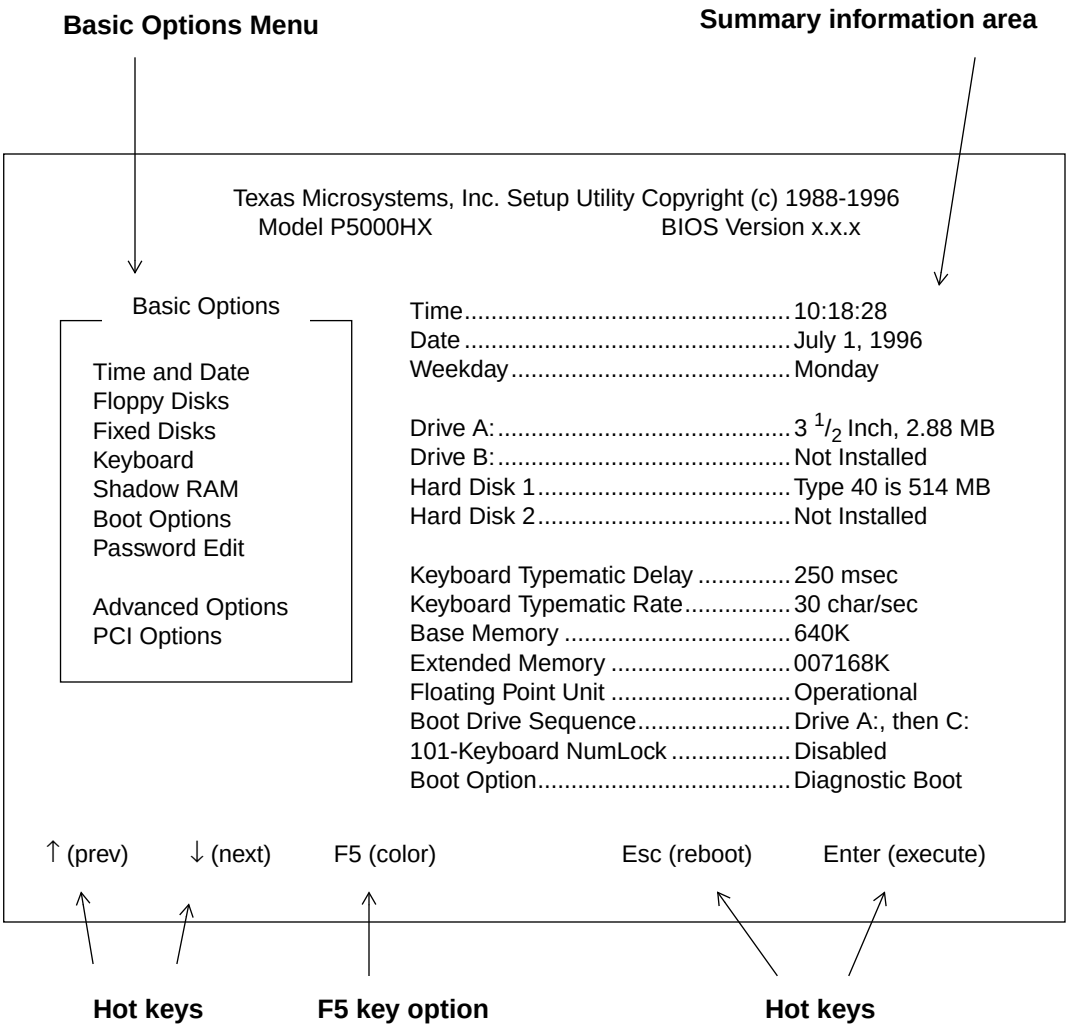
F5 key

If you are using an external monochrome VGA monitor and are experiencing trouble seeing the cursor when the Main Menu is displayed, press the F5 key. The Main Menu attributes will be switched from color to black and white, making the menu easier to read.

Next...

Turn to page 36 for information on the Basic Options Menu.

FIGURE 13 The Main Menu (sample configuration)



Step 7 (cont.) - Run the Setup Utility (Basic Options)

Overview

The Basic Options Menu provides the following options.

Time and Date

This option allows you to set the time and date in the battery-backed clock/calendar.

Floppy Disks

This option allows you to configure the P5000HX to operate the floppy drive subsystem.

Fixed Disks

This option provides menus that allow configuration of the P5000HX fixed disk subsystem.

Note: The "Large Disk DOS Compatible" option should be enabled when you are running DOS-based operating systems. This option enables BIOS translation for drives greater than 528 MB.

Keyboard

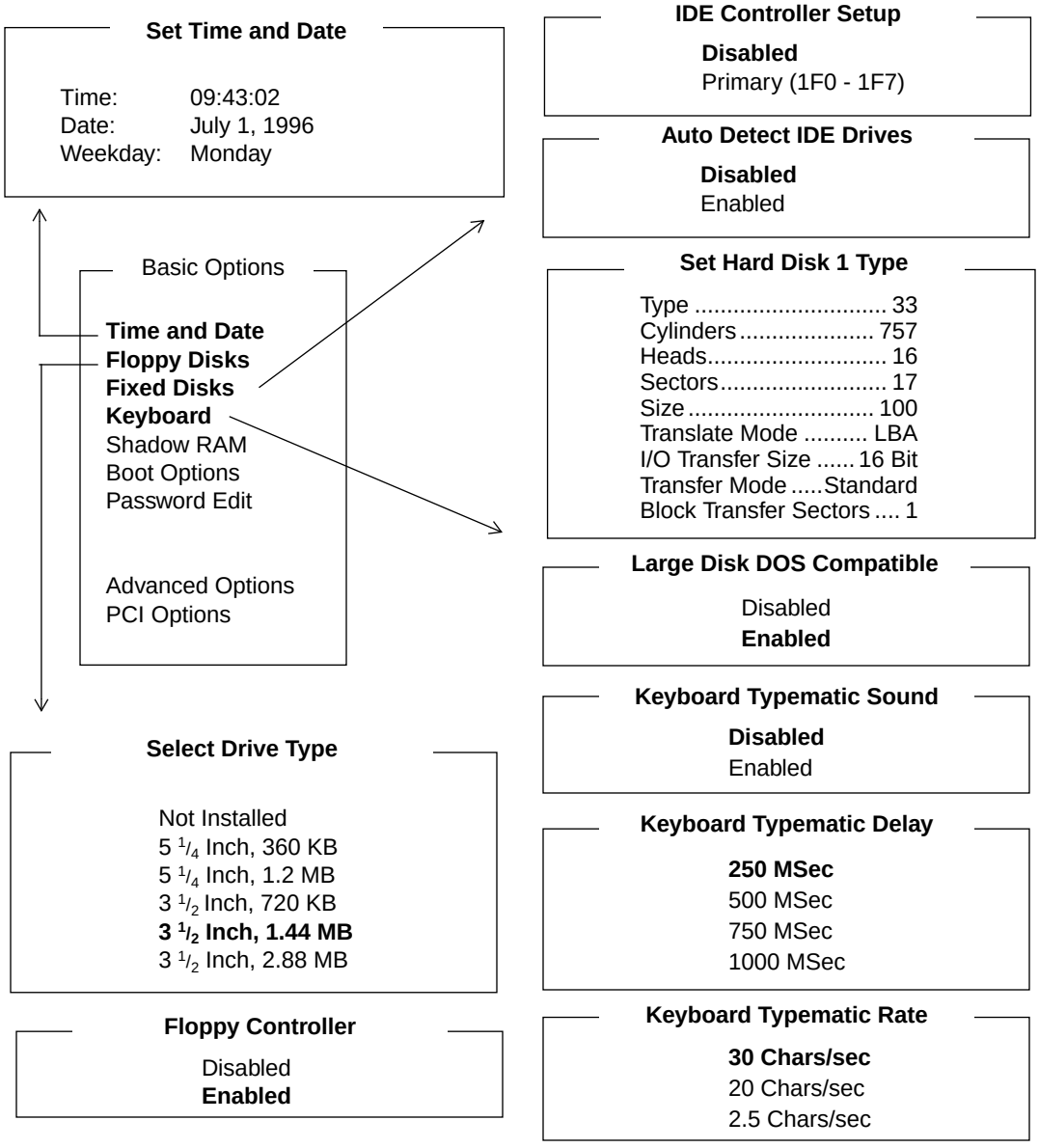
These three menus allow you to set these external keyboard "Typematic" options:

- **sound** (if enabled, the system speaker will "click" as you press keys on the external keyboard),
- **delay** (the period that elapses between the time a key is held down until it begins to repeat), and
- **rate** (the rate at which a character will repeat). *Note: The "Keyboard Typematic Rate" menu will display only three optional settings simultaneously. Continue to scroll through the settings to view all available options.*

Next...

Turn to page 38 for the remaining Basic Options Menu settings.

FIGURE 14 Basic Options (with their associated menus)



Step 7 (cont.) - Run the Setup Utility (Basic Options - cont.)

Overview

The remainder of the Basic Options Menu is described below.

Shadow RAM

When you select this option, a memory map that displays memory in 16 KByte blocks is displayed. If a ROM is found within that 16 KByte location, the Setup Utility will display:

- **ROM** - the system will execute code directly from the ROM device,
- **SHADOW** - the system will copy the code from the ROM device into DRAM at the same address, allowing code to run from the DRAM (dramatically improving system performance), or

A window displays the starting address, length, and status for each option ROM.

Boot Options

The first menu allows you to set the NumLock key status at boot. If a 101-key keyboard is attached, this option directs the BIOS to enable/disable the NumLock key before booting. The second menu allows you to set the boot drive sequence. The third allows for a "quiet boot" (a banner will be displayed, rather than power-up diagnostics).

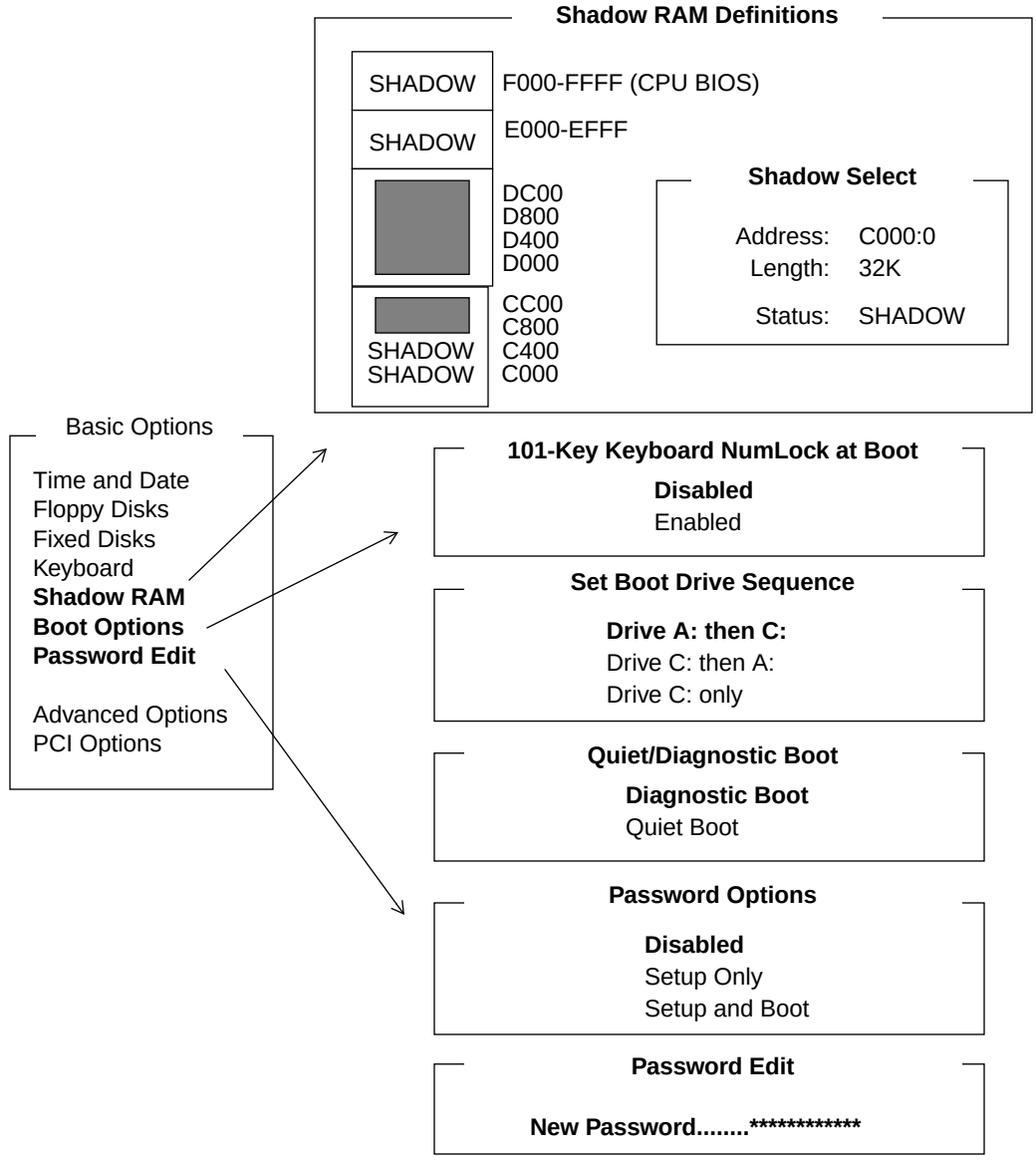
Password Options

This feature allows you to enable and enter a password for Setup Utility access or for Setup and boot access. The password may consist of from one to 12 characters. Letters A to Z (case-sensitive) and numbers 0 to 9 are accepted.

Advanced Options and PCI Options

Note the "Advanced Options" and "PCI Options" items. Choosing these items will cause new menus of options to be displayed. We'll discuss these menus beginning on page 40.

FIGURE 15 More Basic Options



Step 7 (cont.) - Run the Setup Utility (Advanced Options)

Overview

This section introduces the "Advanced Options" menus.

Serial Ports

Use this option to select the port addresses for 16550-compatible Serial Port 1 (UART1) and Serial Port 2 (UART2). *Note: If Serial Ports 1 and 2 are given the same base port address, you will be prompted to make a choice that will resolve the conflict.*

Parallel Ports

Use this feature to select an address for the on-board parallel port (IEEE 1284). This port can also be configured as AT-compatible or PS/2 compatible.

Memory Cache

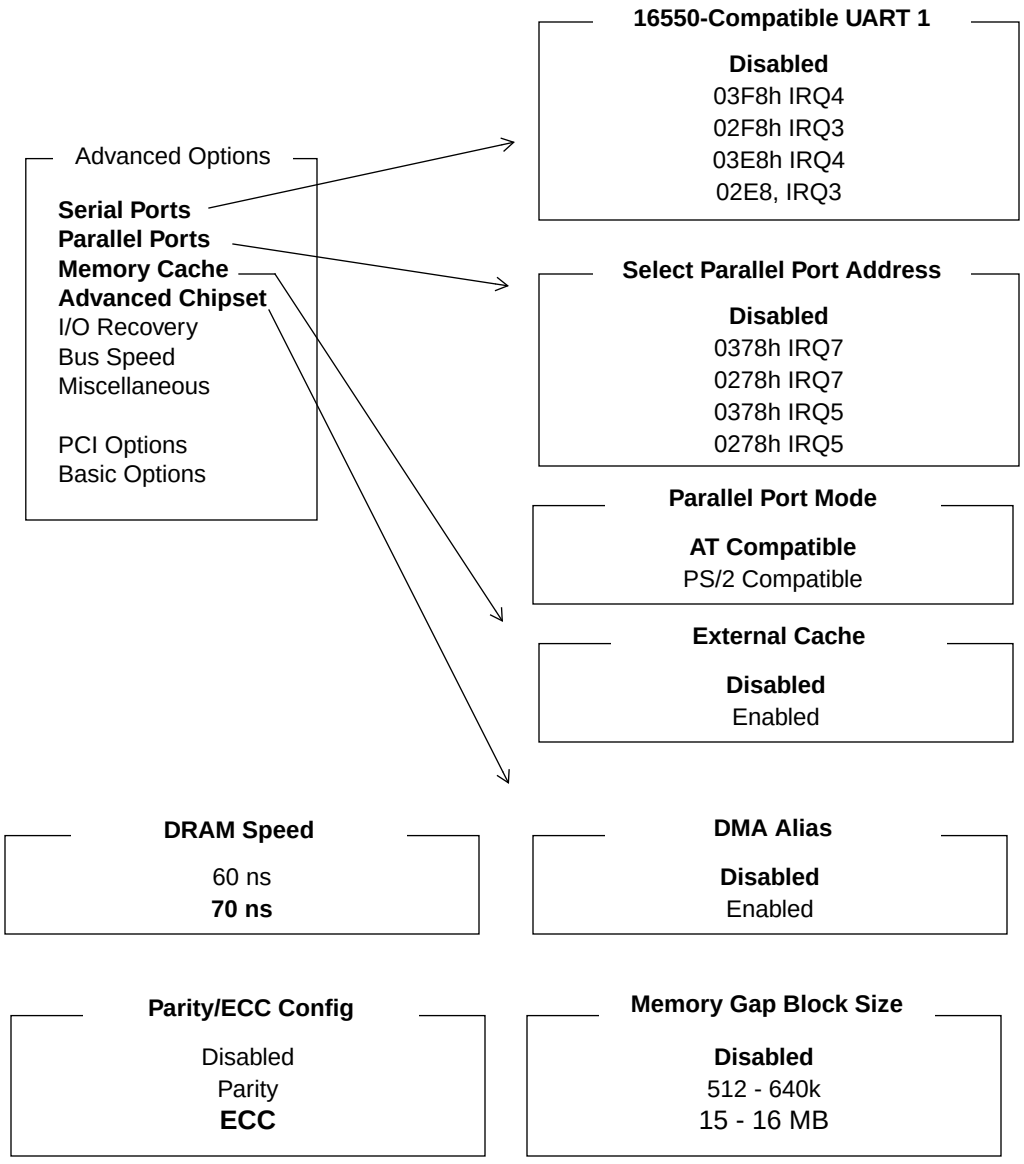
This option allows you to enable or disable the external (L2) write-back cache.

Advanced Chipset

This menu allows you to configure four options:

- **DRAM Speed** - set this option to match the speed of installed SIMMs. *Caution should be used when changing defaults; incorrect settings can damage the system.*
- **DMA Alias** - the DMA Alias feature is an I/O range switch for the chip that is responsible for bridging the PCI to ISA bus. Enable this feature only when experiencing I/O address-mapping compatibility problems.
- **Parity/ECC** - For DRAM with a parity bit, ECC (Error Correction Code) enables the chipset to detect and correct single-bit errors from data reads prior to CPU processing (doesn't apply to multi-bit errors). With the Parity setting, single bit errors are not corrected.
- **Memory Gap Block Size** - this option allows use of the selected memory block for other purposes.

FIGURE 16 Advanced Options menus



Step 7 (cont.) - Run the Setup Utility (Advanced Options - cont.)

Overview

This section describes the remainder of the “Advanced Options” menus pictured on the facing page.

I/O Recovery

These menus provide options to set 8-bit and 16-bit I/O recovery time (in essence, providing additional wait states).

ISA Bus Speed

This menu allows you to configure the P5000HX to match your system’s ISA Bus Speed.

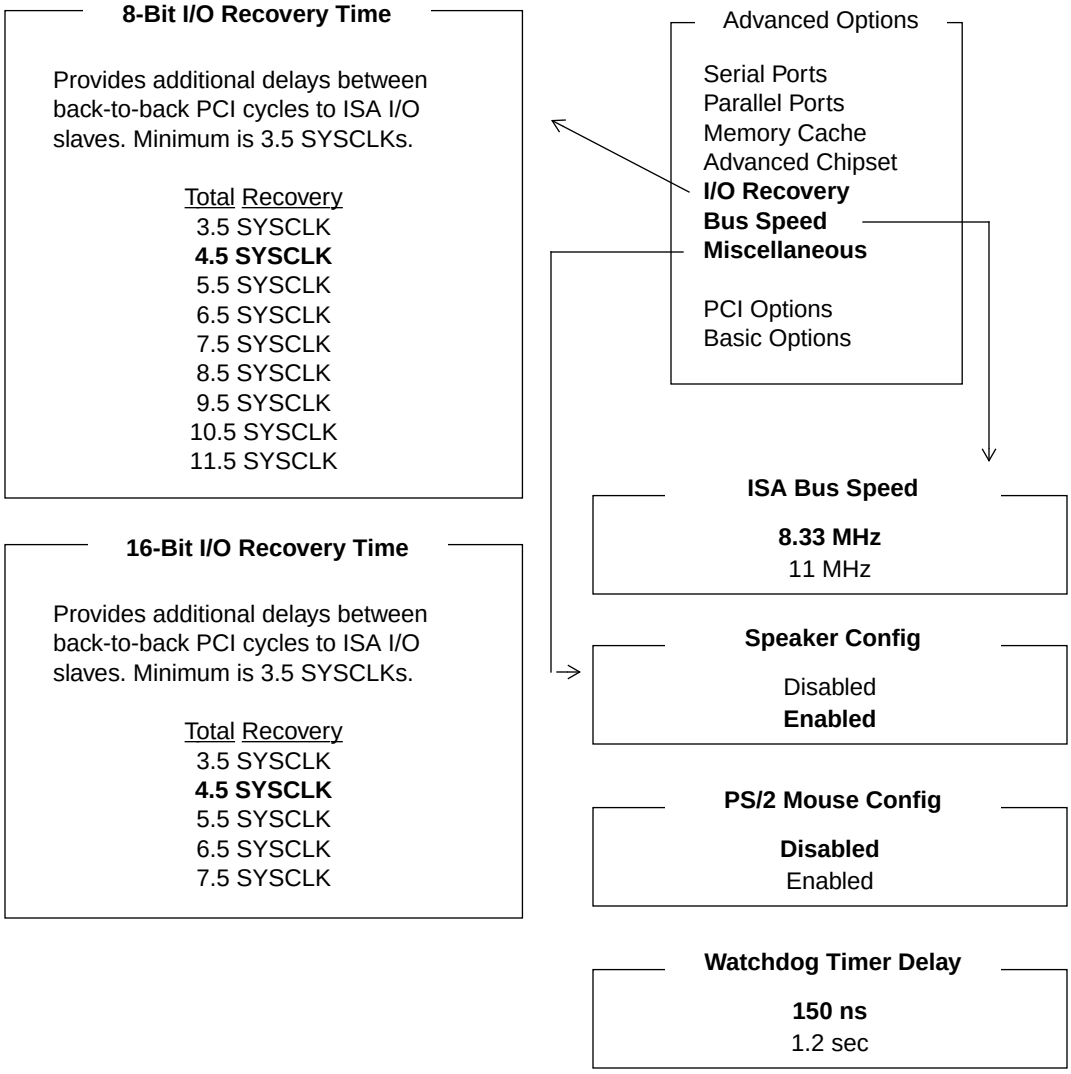
Miscellaneous

This menu allows you to configure three options:

- You can enable/disable the on-board speaker,
- You can enable/disable the on-board PS/2 mouse, and
- You can set the watchdog timer delay (which will be in effect if jumper JP4 is configured for an active watchdog timer - see Section 2.2 on page 14).

Next... Turn to page 44 for information on PCI Options.

FIGURE 17 Advanced Options menus (cont.)



Step 7 (cont.) - Run the Setup Utility (PCI Options)

Overview

This section provides information on the PCI Options menus.

PCI IRQs Setup

The PCI bus features four (4) interrupts: INTA, INTB, INTC and INTD. These interrupts are level-sensitive and can be shared. If a PCI device uses one of these interrupts, the device must be routed to a standard AT interrupt to function. If a PCI device needs an interrupt, you must route the PCI interrupt (INTA, INTB, INTC, or INTD) to an ISA interrupt (IRQ5, IRQ9, IRQ10, IRQ11, IRQ12, IRQ14, or IRQ15).

Using this option, specify which IRQ's are available in the system so the BIOS can allocate any or all the listed IRQ's to PCI devices found in the system. **Do not route the PCI interrupt to an ISA interrupt that is already being used by an ISA device.**

INTA, INTB, INTC or INTD (the PCI bus interrupts) may share a common ISA interrupt. If a PCI interrupt is not used, it will not be routed to the ISA bus, nor will you have the option of routing the interrupt. You can use the "Auto" option to automatically route the PCI devices, but only if no ISA cards are installed.

Note: A number of third-party PCI devices do not share interrupts and will not function properly if assigned the same interrupt as another PCI device in the system. If you are using a PCI card of this type, you must assign additional ISA IRQ resources to the PCI controller.

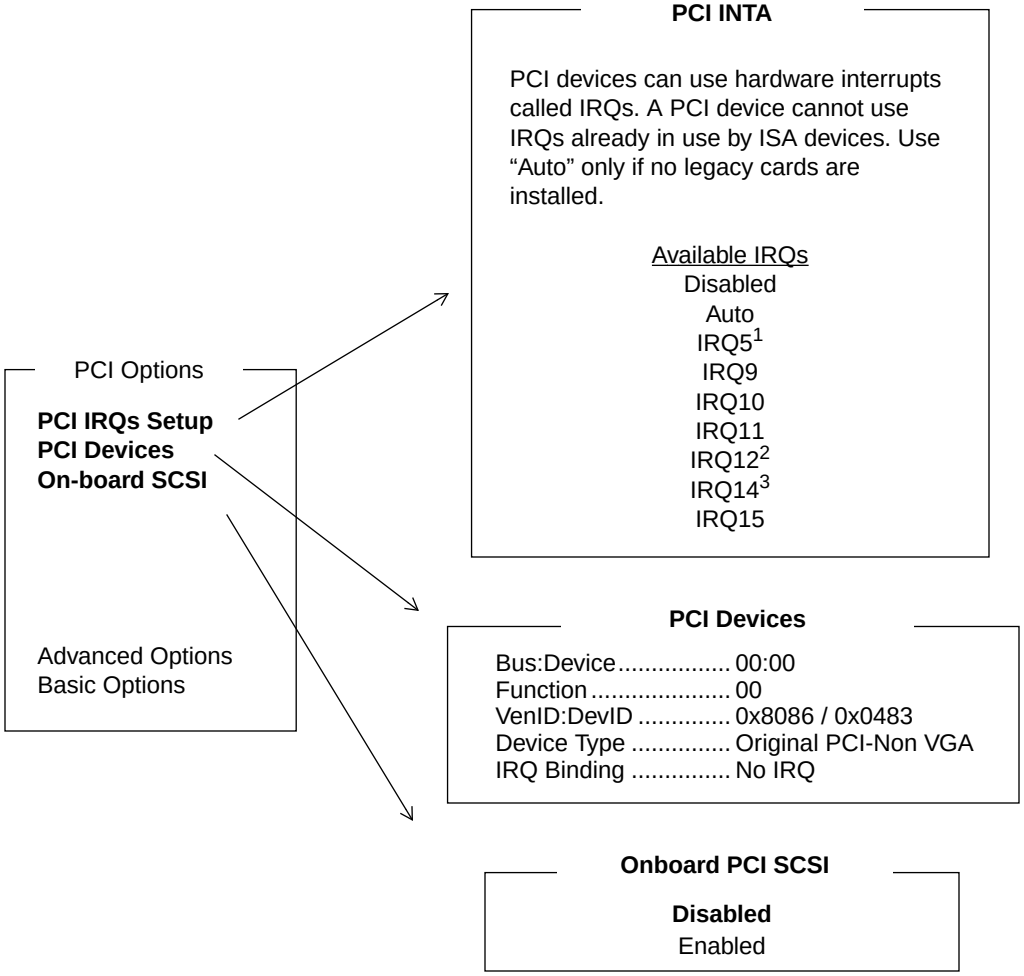
PCI Devices

Each device found on the PCI bus will generate a PCI device window. The window contains information on that PCI device.

On-board SCSI

This menu gives you the option of enabling/disabling the on-board PCI SCSI controller.

FIGURE 18 The PCI Options menu



[1] Only if IRQ 5 is not enabled in the Parallel Port Menu
[2] Only if the PS/2 mouse is not enabled
[3] Only if no other device is using on-board PCI/IDE

This chapter covered...

- P5000HX handling
- jumper configuration
- switch setting
- peripheral connection
- power-up
- the Setup Utility

Next...

The next chapter provides procedures for upgrading and maintaining the P5000HX.

3

P5000HX Service and Support

This chapter provides information on:

- Installing extra memory,
- Maintaining the P5000HX,
- Calling the Texas Microsystems Technical Support line,
- Returning products for service,
- Accessing the Texas Microsystems Bulletin Board System (BBS) and InfoLine fax service, and
- Accessing the Texas Micro Home Page on the Internet.

3.1 Installing Memory

Overview

The P5000HX supports up to 256 MBytes of on-board memory. Memory can be added through the installation of SIMM's (Single Inline Memory Modules).

Memory Banks

The P5000HX provides four 72-pin SIMM sites for memory expansion equivalent to two (2) memory banks, with each bank consisting of two sockets and providing a 64-bit wide data path and 8 parity bits. Memory size is detected by the system BIOS. Memory timing requires 70 ns fast page devices. Parity generation/checking is provided for each byte.

SIMM Types

Five SIMM types (1, 2, 4, 8, and 16MByte) are supported. These x36 SIMM's can be installed in SIMM sockets 1, 2, 3, or 4 as shown in Figure 19:

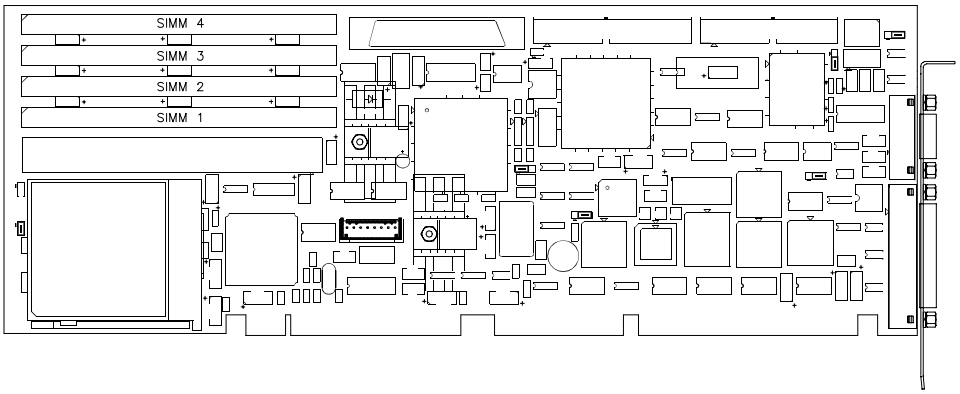
- Sockets 1 and 2 comprise Bank 0.
- Sockets 3 and 4 comprise Bank 1.

Banks must be completely filled to be operable (i.e. if a 1 MByte SIMM is installed in Socket 1, another 1 MByte SIMM must be installed in Socket 2, etc.). The table on the following page summarizes the supported configurations.

Note: The P5000HX board's gold sockets require gold SIMM's. The warranty may be voided if tin/lead SIMM's are used.

CAUTION: Before installing SIMM's, remove power from the system and disconnect all power cords. After power has been removed, remove the P5000HX from the chassis. Only qualified, experienced electronics personnel should access the interior of a chassis. Wear the grounding wrist strap provided with your P5000HX to help remove static electricity. While out of the unit, P5000HX components should be placed on a static-dissipative surface.

FIGURE 19 SIMM sockets



SIMM 1, 2	SIMM 3, 4	Total Memory
1M x 36 (4 MB)	Empty	8 MB
1M x 36 (4 MB)	1M x 36 (4 MB)	16 MB
2M x 36 (8MB)	Empty	16 MB
2M x 36 (8 MB)	1M x 36 (4 MB)	24 MB
2M x 36 (8 MB)	2M x 36 (8 MB)	32 MB
4M x 36 (16 MB)	Empty	32 MB
4M x 36 (16 MB)	1M x 36 (8 MB)	40 MB
4M x 36 (16 MB)	2M x 36 (8 MB)	48 MB
4M x 36 (16 MB)	4M x 36 (16 MB)	64 MB
8M x 36 (32 MB)	Empty	64 MB
8M x 36 (32 MB)	1M x 36 (4 MB)	72 MB
8M x 36 (32 MB)	2M x 36 (8 MB)	80 MB
8M x 36 (32 MB)	4M x 36 (16 MB)	96 MB
8M x 36 (32 MB)	8M x 36 (32 MB)	128 MB
16M x 36 (64 MB)	Empty	128 MB
16M x 36 (64 MB)	1M x 36 (4 MB)	136 MB
16M x 36 (64 MB)	2M x 36 (8 MB)	144 MB
16M x 36 (64 MB)	4M x 36 (16 MB)	160 MB
16M x 36 (64 MB)	8M x 36 (32 MB)	192 MB
16M x 36 (64 MB)	16M x 36 (64 MB)	256 MB

3.2 General Maintenance

Overview

As with any electronic hardware, an adequate maintenance program will enhance the P5000HX's ability to provide dependable performance.

Inspecting the P5000HX

In general terms, maintenance includes periodic inspection of the P5000HX to ensure that it is clean and free from signs of dirt, dust, wear and stress. Cleaning should be performed by a Texas Micro Service Representative.

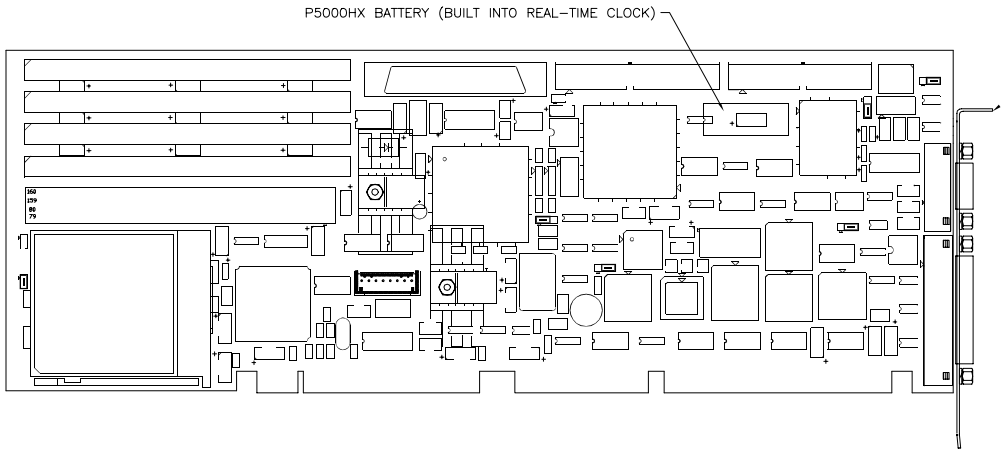
Caution: Always remove power from the system before inspecting the P5000HX Card. Disconnect the power cord from the power source. Only experienced electronics personnel should access the interior of a computer chassis. Do not allow moisture or condensation to contact P5000HX components; damage to sensitive components may occur.

Inspect all cables and connectors to verify that they are securely fastened to their connecting components. Replace worn or stressed cables and connectors. All peripheral equipment used with the P5000HX should be properly maintained. Malfunctioning equipment should be immediately replaced to prevent damage to the P5000HX CPU.

Lithium battery

The P5000HX CPU Card contains a built-in, high-capacity lithium battery that retains the correct time, date and computer parameters in CMOS memory when the system is powered OFF. This retained information assists BIOS in performing initialization and configuration during power-up or reset operations. The battery is designed to provide years of service without replacement. However, if configuration or clock-related inconsistencies occur, the battery may require replacement. **Please return the P5000HX to the factory for battery replacement.**

FIGURE 20 Lithium battery location



WARNING: *Due to risk of fire or explosion, do not recharge, force open or heat the P5000HX battery or dispose of the battery in fire.*

WARNING: *Improper replacement of the battery may cause damage to the P5000HX and void the warranty acquired with the purchase of the P5000HX Card.*

3.3 Customer Support

Overview

Texas Microsystems supports the P5000HX through its Technical Support line, Bulletin Board System (BBS), InfoLine fax service, and Internet home page.

Technical Support

Texas Microsystems provides on-line technical support weekdays from 7:00 a.m. to 6:00 p.m. (Central Time) for your convenience. Our staff of trained professionals welcomes the opportunity to answer questions and assist with technical requirements.

Returning Products for Service

Whenever Texas Microsystems products require service, the factory must be contacted and a Return Goods Authorization (RGA) number must be obtained from a Technical Support Representative.

BBS

Texas Microsystems provides a BBS service that enables customers with modem/communications packages to download several types of software (new BIOS versions, software drivers, etc.) for their Texas Microsystems products. The BBS is in operation 24 hours a day, 7 days a week. The BBS can support modems capable of:

- 300,
- 1200,
- 2400, and
- 9600 (V.32 modulation only) baud.

InfoLine

InfoLine is a “demand publishing” delivery tool that allows customers to use a touch-tone phone to send product description documents to any fax machine, 24 hours a day, 7 days a week.

Internet Home Page

Our home page can be found on the World Wide Web at **http://www.texmicro.com**

Calling Technical Support (7 a.m. - 6 p.m. Central Time)

Step	Action
1	Dial 1-800-627-8700 inside the U.S. Outside the U.S., dial 713-541-8200 (add any appropriate long distance/international access dialing codes).
2	Have the Texas Microsystems product model and serial numbers available.
3	Upon answer by the automated system, press “3” for Technical Support.

Returning Products for Service

Step	Action
1	Call Technical Support (see the table above), ensuring that you have the product model and serial numbers available.
2	When a Returned Goods Authorization (RGA) number is assigned, place it, along with the product serial number, on any packing materials and correspondence. The factory will be unable to accept delivery without these numbers.

Accessing the BBS (available anytime)

Step	Action
1	Dial 713-541-8250 (add any appropriate long distance/international access dialing codes).
2	Set your communication program to use “ANSI” (sometimes called “ANSI-BBS”) as the terminal emulation setting.
3	Follow the directions on the screen as the BBS menu system guides you through the program.

Using the InfoLine Service (available anytime)

Step	Action
1	Dial 1-800-627-8700 (add any appropriate long distance/international access dialing codes).
2	Upon answer by the automated system, press “190” (the InfoLine extension).
3	Enter information as prompted to order documents.

This chapter covered...

- DRAM installation,
- P5000HX maintenance, and
- Customer support.

Next...

Specifications and technical information are provided for your reference.

4

Technical Data

This chapter provides:

- specifications,
- connector pinouts,and
- component-level data

for the P5000HX Series CPU Board.

4.1 Specifications

Overview

Specifications for the P5000HX board are provided in the table on the facing page.

Note...

Specifications are subject to change without notice.

FIGURE 21 P5000HX Specifications

Parameter	Condition	Specification
Temperature	Operating Non-Operating	0°C to 60°C -40°C to +70°C
Humidity	Operating Non-Operating	5% to 95% @40°C, non-condensing 0% to 95% @40°C, non-condensing
Shock	Operating Non-Operating	1.25G, 10ms (10.0G, 11 ms in appropriate chassis) 30.0G, 10ms (40.0G, 11 ms in appropriate chassis)
Vibration	Operating Non-Operation	.25G @ 5Hz to 100Hz (1.5G over 5Hz to 100Hz in appropriate chassis) 5G @ 5Hz to 100Hz
Altitude	Operating Non-Operating	15,000 feet (4572 meters) 50,000 feet (15,240 meters)

4.2 Connector Pinouts

Overview

This section provides pinouts for the P5000HX connectors

Serial Port 1

The Serial Port 1 pinout is as follows.

Pin	Signal Name
1	DCD (Data Carrier Detect)
2	RXD (Receive Data)
3	TXD (Transmit Data)
4	DTR (Data Terminal Ready)
5	GND (Signal Ground)
6	DSR (Data Set Ready)
7	RTS (Request to Send)
8	CTS (Clear to Send)
9	RI (Ring Indicator)

Serial Port 2

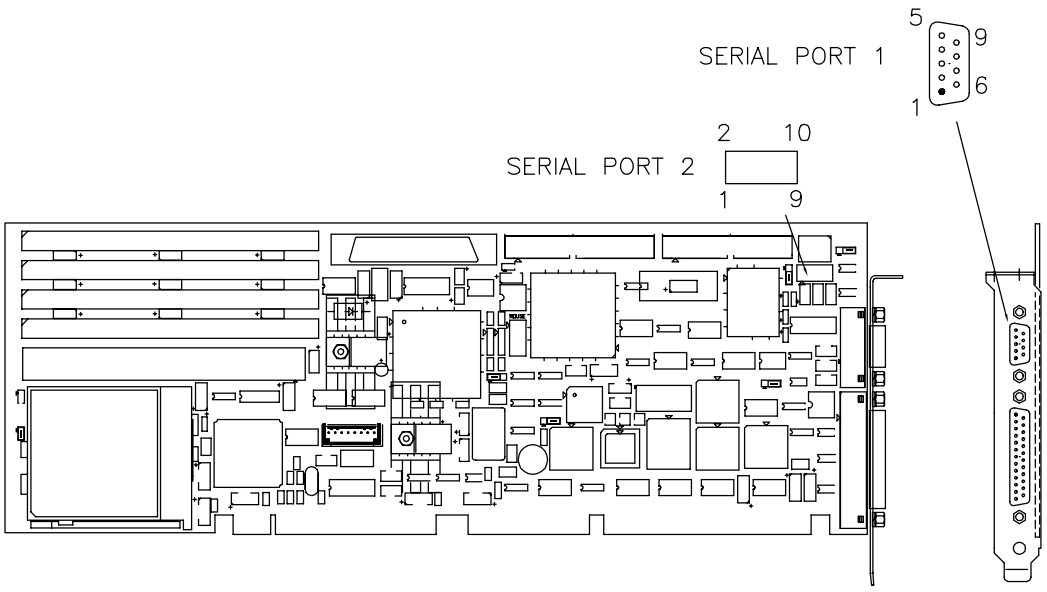
The Serial Port 2 RS-232 pinout is as follows (RS422/485 on facing page).

Pin	Signal Name	Pin	Signal Name
1	DCD -Data Carrier Detect	2	DSR - Data Set Ready
3	RX - Receive Data	4	RTS - Request to Send
5	TX - Transmit Data	6	CTS - Clear to Send
7	DTR - Data Terminal Ready	8	RI - Ring Indicator
9	GND - Signal Ground	10	VCC +5

Next...

Turn to page 60 for additional pinouts.

FIGURE 22 Pin orientation - Serial Ports 1 and 2



Serial Port 2 (UART 2) RS-422/485 Pinout

Pin No.	Description
1	/Z Output (TX-)
2	/B Receive (RX-)
3	Y Output (TX+)
4	Not Connected
5	Ground
6	A Receive (RX+)
7	Not Connected
8	Not Connected
9	Not Connected
10	+5V

To connect two RS-485 devices, use a shielded twisted-pair cable no longer than 4000 ft., configured as follows:

Machine A		Machine B	
Pin No.	**Description**	**Pin No.**	**Description**
1	/Z Output (TX-)	2	/B Receive (RX-)
3	Y Output (TX+)	6	A Receive (RX+)
2	/B Receive (RX-)	1	/Z Output (TX-)
6	A Receive(RX+)	3	Y Output (TX+)

Note: The Pin numbers above are appropriate for connecting two Texas Micro CPU cards through the 10-pin headers only.

Connector Pinouts (cont.)

Overview

Parallel port and hard drive connector pinouts are provided below.

Parallel Port

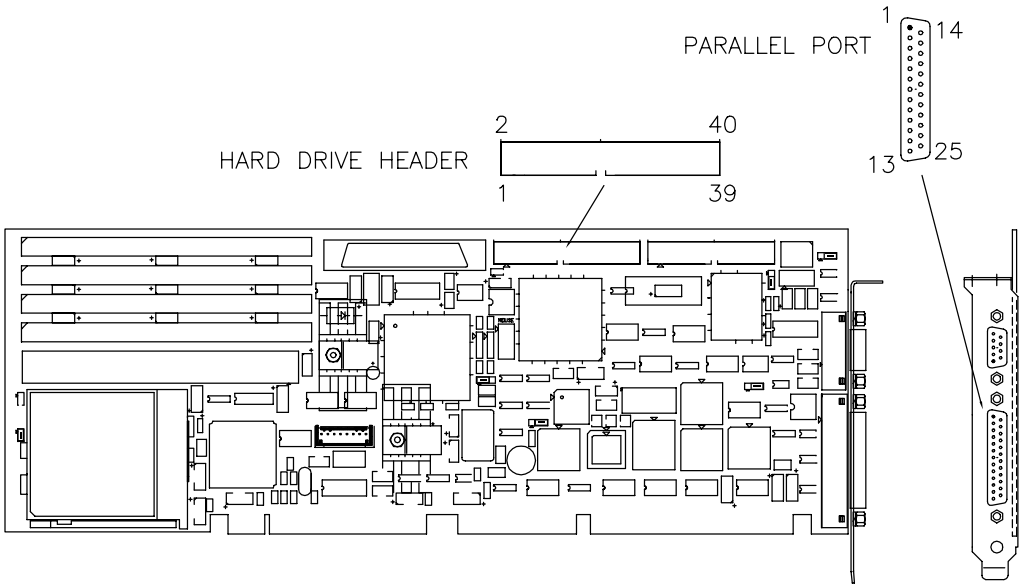
Pin	Signal Name	Pin	Signal Name
1	- Strobe	10	- Acknowledge
2	+ Data Bit 0	11	+ Busy
3	+ Data Bit 1	12	+ Paper End
4	+ Data Bit 2	13	+ Select
5	+ Data Bit 3	14	- Auto Feed
6	+ Data Bit 4	15	- Error
7	+ Data Bit 5	16	- Init. Printer
8	+ Data Bit 6	17	- Select Input
9	+ Data Bit 7	18-25	- Ground

Hard Drive Connector

Pin	Signal Name	Pin	Signal Name
1	Reset, output	2	Ground
3	+ Data 7, input/output	4	+ Data 8, input/output
5	+ Data 6, input/output	6	+ Data 9, input/output
7	+ Data 5, input/output	8	+ Data 10, input/output
9	+ Data 4, input/output	10	+ Data 11, input/output
11	+ Data 3, input/output	12	+ Data 12, input/output
13	+ Data 2, input/output	14	+ Data 13, input/output
15	+ Data 1, input/output	16	+ Data 14, input/output
17	+ Data 0, input/output	18	+ Data 15, input/output
19	Ground	20	No connection
21	No connection	22	Ground

Pin	Signal Name	Pin	Signal Name
23	-I/O Write, output	24	Ground
25	-I/O Read, output	26	Ground
27	No connection	28	+ALE, output
29	No connection	30	Ground
31	+IRQ 14, input	32	I/O CS16, output
33	+ADDR1, output	34	No connection
35	+ADDR0, output	36	+ADDR2, output
37	-CS0, output	38	CS1, output
39	Activity light, output	40	Ground

FIGURE 23 Pin Orientation - Parallel and Hard Drive connectors



Next... Turn to page 62 for more pinouts.

Connector Pinouts (cont.)

Overview

Additional pinouts are provided below.

Floppy Drive

Pin	Signal Name	Pin	Signal Name
1	Ground	2	Disk speed change, output
3	Ground	4	No connection
5	Ground	6	No connection
7	Ground	8	Index detect, input, active low
9	Ground	10	Motor enable Drive A, output, active low
11	Ground	12	Select Drive B, output, active low
13	Ground	14	Select Drive A, output, active low
15	Ground	16	Motor enable Drive B, output, active low
17	Ground	18	Head step direction, output, active low
19	Ground	20	Head step pulse, output, active low
21	Ground	22	Write data, output, active low
23	Ground	24	Write gate, output, active low
25	Ground	26	Track 0 detect, input, active low
27	Ground	28	Write protect sense, input, active low
29	Ground	30	Read data, input, active high
31	Ground	32	Head select, output
33	Ground	34	Diskette change detect, input, active low

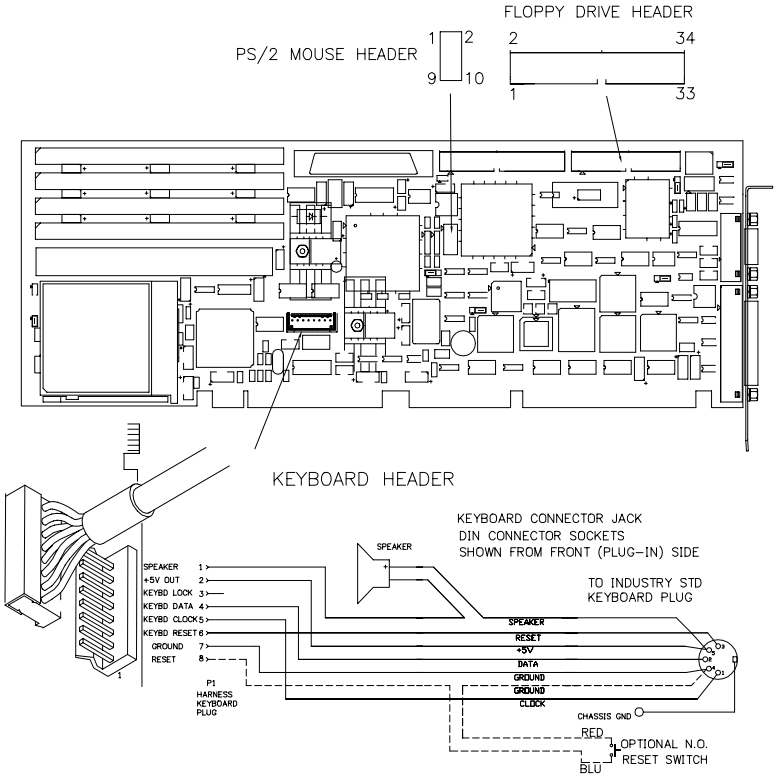
PS/2 Mouse Connector

Pin	Signal Name	Pin	Signal Name
1	Mouse data	6	No connection
2	Mouse Clock	7	No connection
3	No connection	8	No connection
4	No connection	9	Ground
5	No connection	10	+5V Out

AT-style Keyboard

Pin	Signal Name	Pin	Signal Name
1	Reset	5	Keyboard Data
2	Ground	6	Keyboard Lock
3	No connection	7	+5V Out
4	Keyboard Clock	8	Speaker

FIGURE 24 Pin orientation - Floppy, PS/2 Mouse, Keyboard



Next... Turn to page 64 for the SCSI connector pinout.

Connector Pinouts (cont.)

Overview

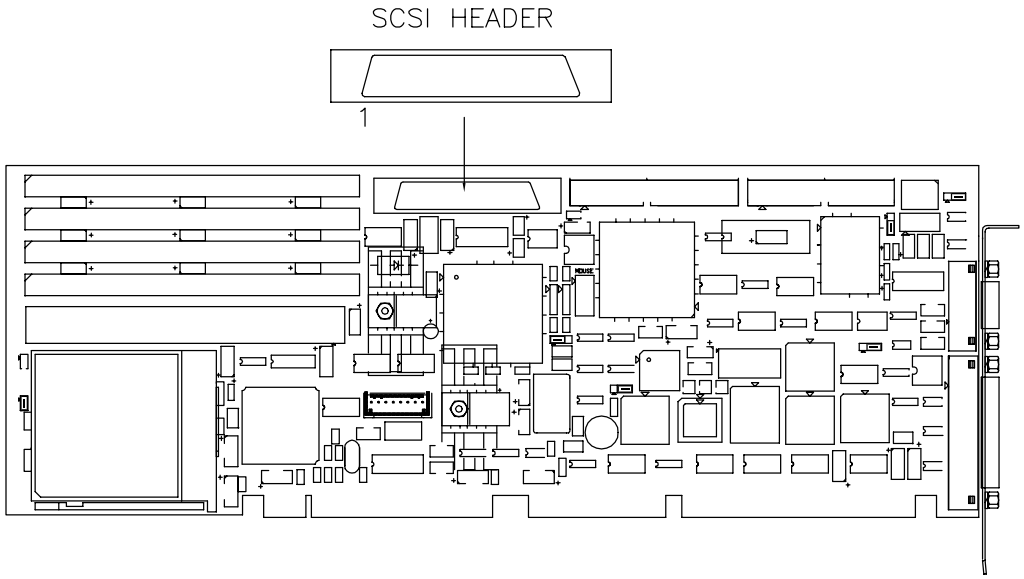
The pinout for the SCSI connector is provided below.

SCSI Connector

Pin	Signal Name	Pin	Signal Name
1	Ground	35	-DB12 (I/O)
2	Ground	36	-DB13 (I/O)
3	Ground	37	-DB14 (I/O)
4	Ground	38	-DB15 (I/O)
5	Ground	39	-DBPH(I/O)
6	Ground	40	-DB0 (I/O)
7	Ground	41	-DB1 (I/O)
8	Ground	42	-DB2 (I/O)
9	Ground	43	-DB3 (I/O)
10	Ground	44	-DB4 (I/O)
11	Ground	45	-DB5 (I/O)
12	Ground	46	-DB6 (I/O)
13	Ground	47	-DB7 (I/O)
14	Ground	48	-DBPL(I/O)
15	Ground	49	Ground
16	Ground	50	Ground
17	TRMPWR	51	TRMPWR
18	TRMPWR	52	TRMPWR
19	Reserved	53	Reserved
20	Ground	54	Ground
21	Ground	55	-ATN (Output)
22	Ground	56	Ground
23	Ground	57	-BSY (I/O)
24	Ground	58	-ACK (Output)

Pin	Signal Name	Pin	Signal Name
25	Ground	59	-RST (I/O)
26	Ground	60	-MSG (Input)
27	Ground	61	-SEL (I/O)
28	Ground	62	-CD (Input)
29	Ground	63	-REQ (Input)
30	Ground	64	-I/O (Input)
31	Ground	65	-DB8(I/O)
32	Ground	66	-DB9 (I/O)
33	Ground	67	-DB10 (I/O)
34	Ground	68	-DB11 (I/O)

FIGURE 25 Pin Orientation - SCSI Connector



4.3 Component Descriptions

Overview

This section provides information on P5000HX components.

CPU

The Enhanced P5000HX PCI/ISA is designed to operate with a 100/133/166/200 MHz Pentium microprocessor. It supports both read and write burst mode bus cycles and includes an on-chip 16 KB cache that is split into 8 KB code and data caches employing a write-back policy.

The Pentium processor also integrates an advanced numeric coprocessor that significantly increases the speed of floating point operations, while maintaining compatibility with i486DX math coprocessor and compliance with ANSI/IEEE standard 754-1985.

Second Level Cache

The Pentium processor's internal cache is complemented with a 256/512 KB write-back second-level cache implemented with optional pipelined burst SRAM modules. Tag and control logic is contained in the 82430HX TXC core chip. External tag 16k x 4 has been added for cacheability detection of up to 512KB cache.

Triton II Xcellerated Controller (TXC)

The Triton II Xcellerated Controller (TXC) is a single chip host-to -PCI bridge providing second level cache control and DRAM control functions. The second level cache (L2) supports a write-back cache policy for cache sizes of 256K and 512KB. The TXC provides a 64/72 bit data path to main memory, and memory sizes of 4M up to 512Mb are supported. The DRAM controller provides eight Rows and optional DRAM error detection/correction (EDC) or parity.

The TXC's optimized PCI interface allows the CPU to sustain the highest possible bandwidth to the graphics frame buffer at all supported frequencies.

The TXC interfaces with the Pentium processor host bus, a dedicated memory data bus, and the PCI bus. The TXC interfaces directly to the Pentium processor 3V host bus, directly to 5V or 3V DRAMs, and directly to the 5V PCI bus. The TXC works with the PCI IDE/ISA Xcellerator (PIIX3) component. PIIX3 provides the PCI to ISA bridge functions along with other features such as a Fast PCI IDE, Plug-n-play port, APIC interface and PCI 2.1 compliant operation.

PCI ISA IDE Xcellerator (PIIX3)

The PCI ISA IDE Xcellerator (82430HX- PIIX3) is a multi-function PCI device implementing a PCI-to-ISA bridge function and a PCI IDE function. In addition, the PIIX3 implements a .host/hub function. The PIIX3 integrates many common I/O functions found in ISA-based PC systems--- a seven Channel DMA controller, two 82C59 interrupt controllers, an 8254 timer/counter, and power management support. The DMA supports compatible and Type F transfers.

The chip select decode logic includes the BIOS, Real Time Clock (RTC) and keyboard controller. The PIIX3 provides support for up to four IDE devices providing an interface for hard disks and CD ROMs. The PIIX3 provides motherboard plug-n-Play compatibility.

Also, the PIIX3 provides an interface with host and hub control functions and two programmable ports. The PIIX3 provides support for an external I/O APIC.

Component Descriptions (cont.)

Overview

The following section describes each of the major functions on the 82430HX-PIIX3 including the memory and I/O address map, DMA controller, interrupt controller, timer/ counter, and power management:.

The PCI, ISA, X-bus and IDE interfaces

The PIIX3 interfaces to two system buses-- PCI and ISA buses. The PIIX3 provides some positive decode for certain I/O and memory space accesses on these buses as described in the next sections.

I/O Access

The PIIX3 positively decodes accesses to the PCI configuration registers, power management registers, APIC registers, and bus master IDE interface registers. Also, the PIIX3 positively decodes the ISA compatible registers, except for the DMA register I/O space, which is subtract decoded. The PIIX3 also provides positive decoding for BIOS and X-Bus and system event decoding for SMM support. The PIIX3 positively decodes PCI bus accesses to registers located on the IDE device when this is enabled.

DMA Controller

The DMA controller incorporates the functionality of two 82C37 DMA controllers with seven independently programmable channels. Each channel can be programmed for 8 or 16-bit DMA device size and ISA-compatible or fast DMA type “A,” type “B,” or type “F” timings. The PIIX3 provides 24 bit address in compliance with ISA specifications. Type F” DMA is selected via the MBDMA[1:0] registers and permits up to two channels to be programmed for type “F” transfers at the same time.

Type F cycles occur back to back at a minimum repetition rate of three SYSCLKs.

Verify transfers are not supported with type F DMA.

PCI local BUS IDE

The PIIX3 integrates a high performance interface from PCI to IDE. This interface is capable of accelerated PIO data transfers as well as acting as PCI bus master on behalf of an IDE DMA slave device. The IDE data transfers command strobes, DMA request and grant signals, and IORDY signal interface directly to the PIIX3. Also, the IDE data lines interface directly to the PIIX3 and are buffered to provide part of the ISA address bus as well as the X-Bus chip select signals. Only PCI masters have access to the IDE port. ISA bus masters cannot access the IDE I/O port addresses.

ISA Interface

The PIIX3 incorporates a fully ISA Bus compatible master and slave interface. The PIIX3 directly drives five ISA slots without external data buffers. The ISA interface also provides byte swap logic, I/O recovery support, wait state generation, and SYSCLK generation. ISA refresh cycles are generated by the refresh controller inside the PIIX3.

The ISA interface supports the following types of cycles:

- PCI master initiated I/O and memory cycles to the ISA bus
- DMA compatible cycles between main memory and ISA I/O, and ISA I/O and ISA memory.
- Enhanced DMA cycles between PCI memory and ISA I/O
- ISA refresh cycles initiated by the PIIX3 or an external ISA master
- ISA master-initiated memory cycles to PCI, and ISA master-initiated I/O cycles to the internal PIIX3 registers.

Component Descriptions (cont.)

Overview	Additional components are described below.
PCI Interface	The PIIX3 incorporates a fully PCI Bus compatible master and slave interface. As a PCI master, the PIIX3 runs cycles on behalf of DMA, ISA masters, or a bus master IDE. As a PCI slave, the PIIX3 accepts cycles initiated by PCI masters targeted for the PIIX3's internal register set of the ISA bus. The PIIX3 directly supports the PCI interface running at either 25 MHz, 30 MHZ, or 33 MHz. Also, the PIIX3 supports the standard PCI cycle terminations as described in the PCI local configuration.
Timer Block	The timer block contains three counters that are equivalent in function to those found in one 82C54 programmable interval timer. These three counters are combined to provide the System Timer function, Refresh Request, and speaker tone.
Utility Bus (X-Bus) Logic	Chip selects for Flash BIOS, real time clock, keyboard/mouse controller, floppy controller, two serial ports, one parallel port, and an IDE hard disk drive. The PIIX3 provides the control for the buffer that isolates the lower 8 bits of the ISA bus.
Interrupt Controller Block	The PIIX3 provides an ISA-compatible interrupt controller that incorporates the functionality of two 82C59 interrupt controllers.

Intel Advanced Integrated Peripheral (AIP) 82091AA.

Control for the integrated serial ports, parallel port, floppy drive and IDE hard drive interface is incorporated into a single component, the Intel 82091AA. This component provides:

- Two 16550-compatible UARTs with 16-byte FIFO and baud generation of up to 256K
- Multi-mode bi-directional parallel port
- Standard mode; IBM and Centronics compatible
- Enhanced Parallel Port (EPP)
- High Speed mode; Enhanced Capabilities Port (ECP) compatible with 16-byte FIFO
- Industry-standard floppy controller with 16-byte data FIFO (2.88 MB floppy support)
- IDE hard disk decode and chip select (NOT USED)
- Supports DMA with type F transfers
- Five programmable ISA interrupt lines
- Serial ports can be configured via setup program as either IRQ3 or IRQ4

Keyboard - PS/2 Mouse Interface

An Intel S82C42PC surface mount microcontroller contains the Phoenix Technologies-compatible keyboard/mouse controller code. An 8-pin header allows connection with a cable adapter to an AT-style keyboard connector. Also, a 10-pin (2x5) header allows connection with a cable adapter to a PS/2 mouse connector.

Dallas DS12887 Real Time Clock

The DS12887 is accurate to within 12 minutes/year at 25°C and requires no external support (the battery and oscillator are integrated into the device). The component is socketed and can be replaced if the internal battery loses its charge (the internal battery has an estimated life time of seven to ten years). The RTC can be set via the BIOS Setup Utility.

Component Descriptions (cont.)

Overview

The SCSI host adapter, system BIOS, and FLASH implementation are discussed below.

Adaptec AIC-7870 SCSI Host Adapter

The Enhanced P5000HX PCI/ISA uses the Adaptec AIC-7870 SCSI host adapter, which incorporates the PCI host interface, the SCSI protocol controller, a powerful 10 MIPS processor, and a large 256-byte FIFO in a 160-pin plastic quad flat pack (PQFP) package. The large FIFO maximizes DMA transfers and reduces system latencies. The 10 MIPS SCSI Phase-Engine functions as an I/O coprocessor to offload the host CPU. Active termination is provided through two monolithic ICs containing the voltage regulator, voltage reference, and resistors circuits.

The AIC-7870 features the following:

- True 32-bit PCI bus master DMA implementation.
- Maximizes data transfer on PCI local bus at 133 Mbytes/sec data bursts.
- Low SCSI command overhead of 50 ms greatly improves command executions.
- Only one interrupt per SCSI command.
- Up to 16 SCSI commands can be stored for auto execution by the.
- Phase-Engine, off-loading the CPU for other tasks.
- Scatter/Gather supported in hardware.
- Tagged Queuing supported.
- 256 bytes Data FIFO buffer reduces system latencies.
- 16-bit single-ended Fast SCSI port.
- Multithreading supports up to 8 simultaneous I/O tasks.

- Disconnect/Reconnect feature frees host for other processes when SCSI devices are busy
- One port with a single cable connects up to 7 SCSI peripherals.
- Up to 20 Mbytes/sec synchronous Fast SCSI data rate.

System BIOS

The Enhanced P5000HX PCI/ISA uses the Phoenix BIOS, which is stored in an auxiliary boot ROM and in a Flash EEPROM for upgradability using a floppy disk-based program. In addition to the BIOS, the Flash EEPROM also contains the Setup Utility, Power-On Self-Test (POST), update recovery code, and the PCI auto-configuration utility.

Flash Implementation

The FLASH component is organized as 512K x 8 (512 KB). The Flash device is divided into four areas, as described in the table below.

Address	Description
F000 - FFFF	BIOS
E000 - EFFF	ISA Devices
C800 - DFFF	Reserved for PCI/ISA devices
C000 - C7FF	Reserved for VGA BIOS

NOTES