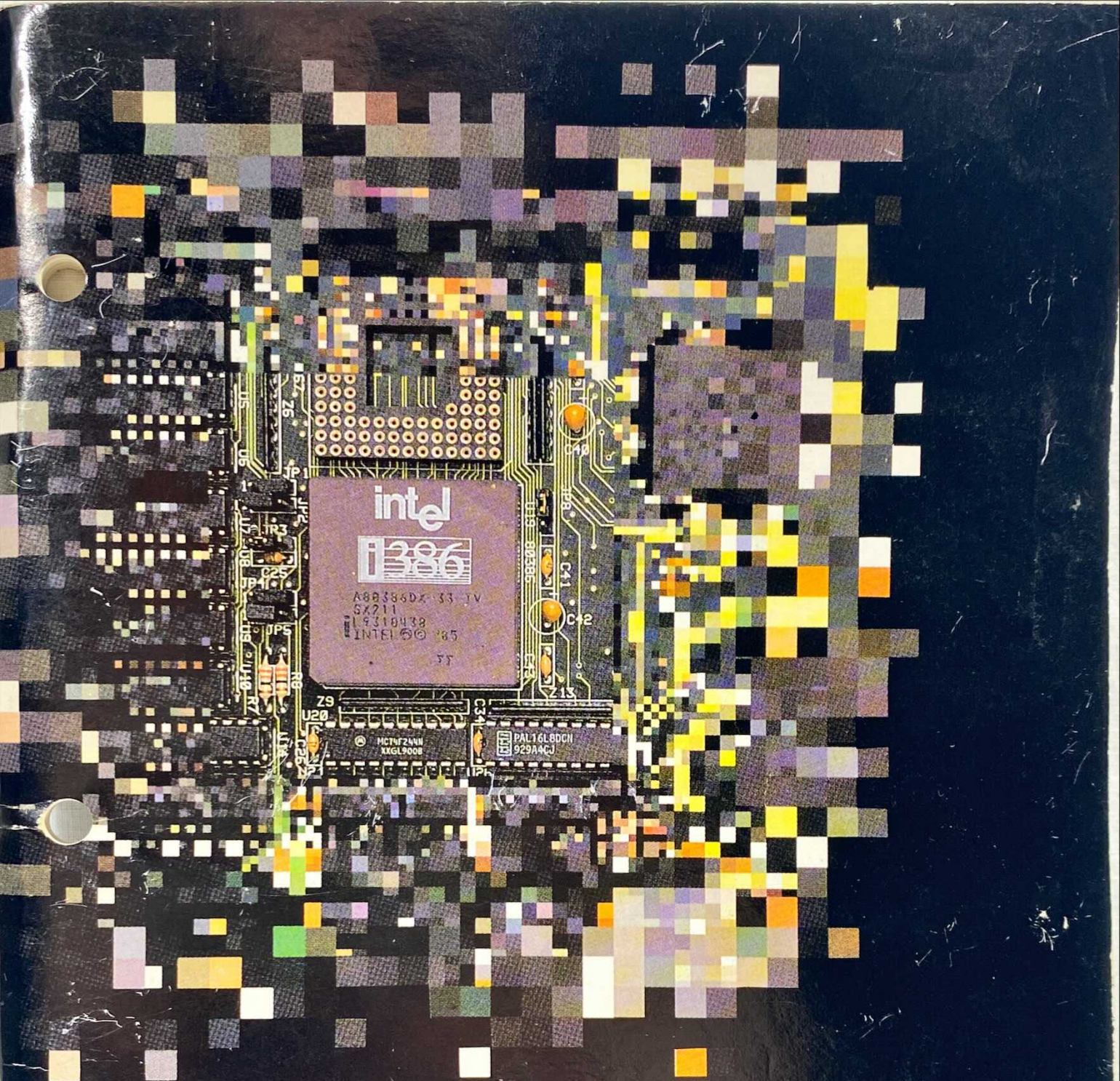


25MHz / 33MHz JAGUAR 386 MAIN BOARD

USER'S MANUAL

JAGUAR
386

The material in this manual is for information only and is subject to change without notice.

VERSION: 1.0

RADIO FREQUENCY INTERFERENCE STATEMENT

This equipment generates and uses radio frequency energy and if not installed and used properly, that is, in strict accordance with the manufacturer's instructions, may cause interference with radio and television reception.

If this equipment does cause interference to radio or TV reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

* Reorient the receiving antenna.
* Relocate the computer away from the receiver.
* Move the computer away from the receiver.
* Plug the power cord of computer into a different outlet so that computer and receiver are on different branch circuits.
* Ensure that card slot covers are in place when no card is installed.
* Ensure that card mounting screws, attachment connector screws, and ground wires are tightly secured.
* If peripherals are used with this system, it is suggested to use shielded, grounded cables, with in-line filters if necessary.

If necessary, the user should consult the dealer service representative for additional suggestions.

The manufacturer is not responsible for any radio or TV interferences caused by unauthorized modifications to this equipment. It is the responsibility of the user to correct such interferences.

Note

1. *Electronic components are sensitive to dust and dirt. Do inspect and clean the computer system regularly.*

2. *Turn off the power whenever you install or remove any connector, memory module and add-on card. Before turning on the power, make sure that all the connectors, memory modules and add-on cards are secured.*

3. *After power is on, please wait for a minute. The system BIOS are going through a self-test during this period and nothing is shown on the screen. After the self-test, the system BIOS will initialize the display adaptor and show messages.*

4. *The SIMM sockets are fragile device. Do not force the SIMM modules into the sockets. It may break the locking latches.*

Preface

The manual provides information about the installation and maintenance of OCTEK Jaguar-386 motherboard. In-depth explanations of the functions of this motherboard are provided. In the appendix, the system BIOS setup is explained.

The content in this manual is only for reference and is intended to provide basic information for the general users. There are also some technical information for hardware and software engineers.

In this manual, there are 4 chapters. Chapter 1 contains a brief introduction and specification of OCTEK Jaguar-386 motherboard. In the Chapter 2, the functions of Jaguar-386 are explained. It also outlines many advanced features of the CPU and the system architecture. Chapter 3 explains the installation of coprocessor, DRAM modules and jumpers. Some technical information are provided in the Chapter 4.

System BIOS and the system setup are described in the appendix A. All the setup procedures are explained. Appendix B contains the information about the memory expansion board.

Additional information are given in appendix C, D, E and F for the maintenance purpose.

CONTENT

Chapter 1
Introduction

OCTEK Jaguar-386 consists of 32-bit 80386 microprocessor, a large cache memory and highly integrated chipsets to provide high performance, reliability and compatibility. OCTEK Jaguar-386 is a perfect choice for CAD/CAM workstation and file server and supports sophisticated 32-bit computing applications and multi-user operating systems.

To speed up the performance of the system, a cache memory with maximum size up to 64KB is incorporated. Frequently used program codes can be fetched by CPU from the high speed cache memory without wait state. Furthermore, access to the main memory is accelerated because the cache controller and the memory controller are integrated together, and operate concurrently. Thus the overhead of accessing the main memory is minimized.

Aimed at supporting advanced CAD/CAM applications, OCTEK Jaguar-386 supports 80387 or WEITEK 3167. The total memory is 16MB. 8MB memory is installed on board and additional 8MB is on memory expansion board which is installed on a fast speed 32-bits memory expansion slot.

Compatibility and reliability are important issues. I/O channel is compatible to standard AT bus. Therefore any AT compatible peripherals may be used on OCTEK Jaguar-386. On board POWERGOOD generator is essential to ensure the reliability of the system and is well-designed to work with all power supplies.

Chapter 2
General Features

SPECIFICATION

Processor :

Intel 80386DX CPU
with optional 80387DX Math
Co-processor
or WEITEK 3167 Coprocessor

Speed :

Turbo/normal speed
Software/hardware selectable

I/O Slot :

Compatible to standard AT bus
Two 8-bit and six 16-bit slots

Cache Memory :

32KB or 64KB Cache Memory
Direct mapped with posted write through operation

Internal Cache :

Built-in 2 way set associative cache controller with integrated 128 Byte cache memory.

Memory :

Shadow RAM for System BIOS and Video BIOS
Page mode/hidden refresh
SIMM sockets for 256K or 1M modules
8M bytes on board
Up to 16M bytes with optional memory expansion board

System Support Functions :

- 8-Channel DMA (Direct Memory Access)
- 16-level interrupt
- 3 programmable timers
- CMOS RAM for system configuration
- Real time clock with battery backup

Other Features :

- On board POWERGOOD generation
- External battery connector
- Hardware turbo switch

PROCESSOR

80386DX is a 32-bit microprocessor with 32-bit external data bus and 32-bit external address bus. Therefore it processes more data at the same time than 80286 and can access a large memory size which is necessary for 32-bit applications. To combine the wider bus structure and all the advanced functions on chip, total 275,000 transistors are integrated together.

A advanced pipeline architecture is implemented. Next four bytes of instructions are prefetched into the CPU whenever the bus is idle. The size of the prefetch queue is increased to hold 12 bytes. This architecture reduces the overhead of retrieving and decoding of the instructions.

80386DX is aimed to provide advanced facilities to sophisticated software, but still remains compatible with existing software in the market. It can operate at real mode and protected mode. In Real mode the 386DX operates as a very fast 8086, but with 32-bit extensions if desired. Real mode is required primarily to setup the processor for Protected mode operation. Protected mode provides access to the sophisticated memory managememt, paging and privilege capabilities of the processor. Furthermore, new mechanism allows switching between real mode and protected mode at high speed operation.

Hence applications using EMS memory or extended memory can run efficiently although they need software driver to access the memory beyond 1MB.

The protected mode of 80386 is fully compatible with 80286. All privilege - level and I/O protection system are supported. New system control instructions, memory paging, I/O permission bit map are provided to make 80386 ideal for multi-tasking operation systems.

In addition, a virtual 8086 mode is provided. In this mode, the CPU can be considered by the programs as being divided into several 8086 CPUs and each program has their own CPU and memory space. Several programs for XT/AT as well as operating systems for 80286 and 80386DX can be executed simultaneously. Programs are isolated and protected from each other by 80386DX. Each program can be considered as running at a XT/AT.

Internal memory management unit is complicated, but provides a more flexible addressing scheme for the next generation of operation system. Multitasking, concurrent operation and manipulating huge data base can be accomplished with excellent performance. Paging mechanism is employed by 80386DX to allow powerful operating system to implement virtual memory. Each segment is divided into several pages which are 4K bytes per page. Page mechanism is transparent to software and allows software to address up to 64 terabytes.

Furthermore, the 64KB segment boundary which is an barrier of 8088 and 80286 is removed and the segment length can be increased up to 4GB. It eliminates the need for the software to manage multiple code and data segments and allows software of other operating system to be transferred to PC more easily.

80386DX includes many new instructions for system control, high level language support and processor control. These instructions are used in protected mode. New operation systems and software can make use of these instructions for their advanced features, such as concurrent operation and virtual memory.

MATH COPROCESSOR

The demand for sophisticated, number-crunching scientific and business applications has rapidly increased in recent years. 80386DX features an integer Arithmetic Logic Unit which only handles simple integer operations such as addition and multiplication. Floating-point operations which are actually utilized by applications must be accomplished through software routines.

To overcome this obstacle, external Math coprocessor is necessary. The Math coprocessor contains complex hardware and large data registers for floating-point numeric operations. In OCTEK Jaguar-386, the Math coprocessor is optional and both Intel 80387 and WEITEK 3167 are supported.

80387 is upward object-code compatible from 80287 and 8087, but runs 6 to 11 times faster than 80287 used in AT. It fully implements the IEEE 754 Binary Floating-point Arithmetic standard with a high precision 80-bits internal architecture.

WEITEK 3167 can deliver more power than 80387 and is supported by various operation systems and high level programming language compilers. It has a direct interface with the CPU. So the data are transferred between them at full speed.

CACHE MEMORY

The system performance can not simply be improved by increasing the clock rate of the system. The performance depends on many factors, such as system architecture and memory configuration.

A cache memory system with low cost DRAM as main memory and high speed SRAM as cache memory becomes the only choice for high performance system in terms of price and performance. The frequently used data code instructions are kept in the high speed cache memory. Therefore, most of the memory operations are carried out in the cache memory instead of the slow speed main memory.

The cache controller of Jaguar-386 is integrated into the chipset, which will simplify the system design and reduce the chip count. Furthermore, the cache controller is able to run at three modes: 64K bytes external cache, 32K bytes external cache and internal two-way set associative mode. The 64K bytes and 32K bytes external cache modes are adequate for single user environment as well as multitasking and network operating system. The internal cache mode is suitable for a low cost configuration with optimal performance. In all operation mode, 16MB main memory can be cached. The line size for both cache scheme is 32-byte wide.

The cache controller works jointly with the memory controller. This arrangement can speed up memory access when a cache read miss occurs and hence the overall performance is improved. For a cache read hit, the CPU operation is completed with zero wait state. Posted write mechanism is implemented. The memory write is buffered and runs at zero wait state.

The design of the cache controller is intended to provide optimum performance with simple construction. With 64KB cache memory, hit rate exceeds 95% and the wait state is almost eliminated.

Posted Write through

In a cache system with write through, the CPU has to update both the cache memory and the main memory simultaneously to keep the data consistent. However, the main memory needs many cycles to update the data and thus wait states are needed for all memory write cycles. In a posted write through system, the cache will buffer memory write to the main system memory until the memory bus is available. The CPU can continue processing once it has written to the buffer. In Jaguar-386, zero wait state for memory write operation is achieved. When the memory bus is available, the cache independently completes the write operation to the main memory. The decrease in performance of the write through strategy is thus avoided.

Internal 2-way Set Associative Cache

OCTEK Jaguar-386 provides a built-in 128-bytes two-way set associative cache to boost system performance. No external logic and SRAMs are needed. Although the cache size is 128 bytes, it deliver excellent performance with a two-way set associative architecture.

Additionally, the 128-byte internal cache SRAM or external cache are mutually exclusive, it, thus only one of these schemes can be chosen in the setup procedures.

MEMORY SYSTEM

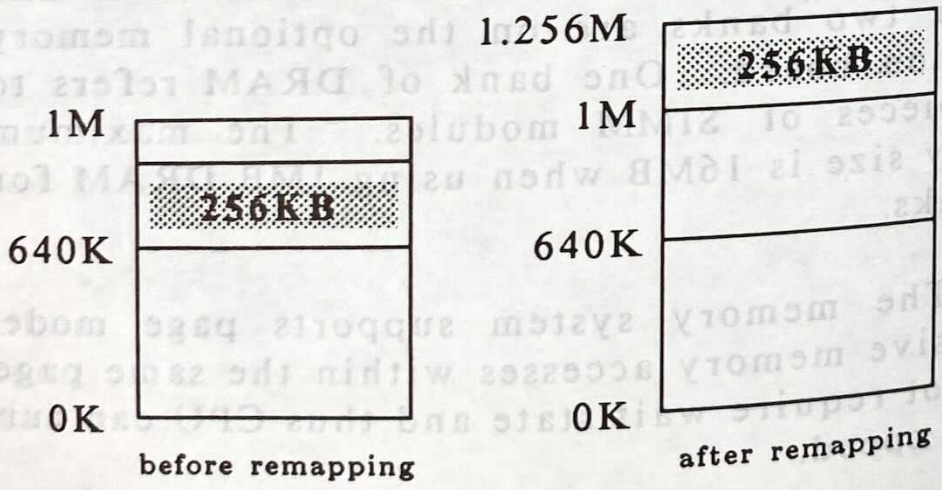
Four banks of DRAMs can be installed. Two banks are available on motherboard and another two banks are on the optional memory expansion board. One bank of DRAM refers to four pieces of SIMM modules. The maximum memory size is 16MB when using 1MB DRAM for all banks.

The memory system supports page mode. Successive memory accesses within the same page need not require wait state and thus CPU can run at full speed.

To enhance the system performance, shadow RAM mode is supported. In shadow RAM mode, system BIOS and video BIOS contained in low

speed memory such as EPROM and ROM are copied into DRAM. Improvement is significant because access to DRAM is much faster than ROM.

Another useful feature is memory remapping. 640K bytes is allocated as base memory. On the other hand, system BIOS and video BIOS occupy some locations between 640K and 1M. When 1M bytes or more are installed, there are some portions of DRAM overlapping with the BIOS which cannot be accessed. Memory remapping allows these portion of memory to be accessed at other locations and thus can be utilized by the software. Memory remapping is supported by hardware and can be enabled in system setup.



Memory Remapping

Because of the shadow RAM and memory remapping feature, the memory size may not be equal to the actual memory size. Suppose that there is 1MB on board. If the shadow RAM feature is enabled, the BIOS will show there is 896KB. 128K bytes are assigned for shadow RAM and can not be used by software. After the shadow RAM is disabled, the memory size is increased to 1MB. When the on-board memory is 4M byte, only 256KB memory can be remapped. For more than 4MB, there is no remapping scheme for Jaguar-386. So only 7808K is available when there is 8M bytes installed. The memory between 640KB to 1M can not be used. The following table is show the remapping scheme for the Jaguar-386 in different memory configuration :

Memory Remapping :

Relocation Memory Size

Memory Install	Shadow RAM Enable	Shadow RAM Disable
1M	256K	384K
2M	256K	384K
4M	256K	256K
>4M	0K	0K

Hidden Refresh

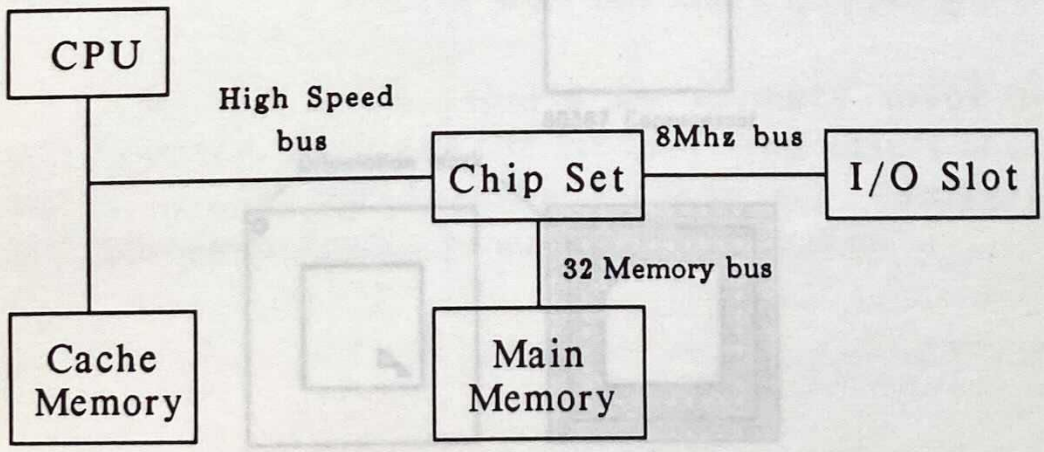
In the original PC/AT design, the CPU suspends its operation during memory refresh. The memory refresh cycle takes about 5% of CPU time which is a short period of time in a slow machine. Nevertheless, in a 33MHz machine, it will significantly downgrade the system performance since the CPU can complete more operations in the same period.

In Jaguar-386, a hidden refresh function is provided. When the hidden refresh function is enabled, the CPU will not stop its operation and the memory refresh operation is transparent to the CPU access. The chipset will monitor the whole system. If the CPU is accessing the main memory, the memory refresh operation is postponed and will be carried out when there is access to AT/expansion bus. Special refresh mechanism is implemented to reduce the period of memory refresh operation.

DUAL BUS DESIGN

It is very important that a high speed system should be compatible with existing peripherals without lowering the performance. To be compatible, the I/O slot should run at 8MHz or slower. On the other hand, the rest of the system are running at full speed.

A dual bus design is employed. A high speed bus links the CPU, coprocessor, cache memory and main memory. This bus is synchronous with the clock of the CPU and the data transfer is 32 bits. Whenever there is a request for transferring to or from I/O slot, the chipset is responsible for handling the conversion between the buses. The clock rate of the high speed bus will not be reduced, which eliminates many compatibility problem.



SYSTEM FUNCTIONS

System functions include :

- Interrupt
- DMA
- Timer
- Real time clock
- Clock and ready generation
- I/O channel control

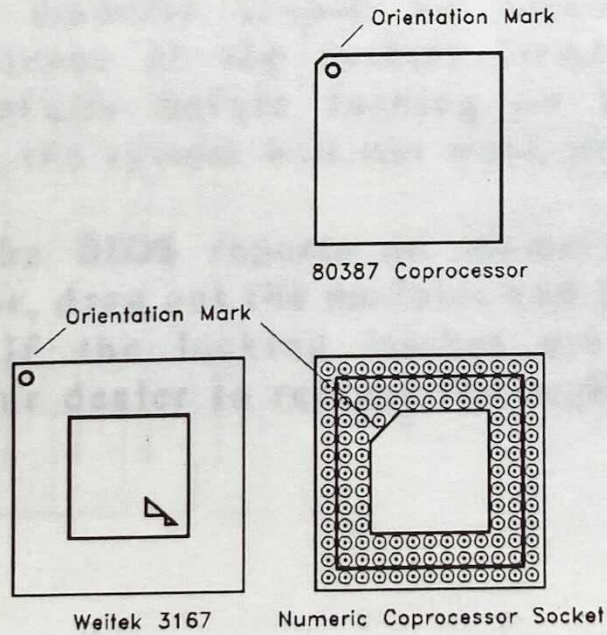
All system functions are 100% compatible to AT standard. I/O channel of OCTEK Jaguar-386 is designed to be compatible with standard AT bus. All the expansion cards conformed to the standard AT bus can be used in OCTEK Jaguar-386 without problem.

Chapter 3
Installing Components

Important Note : Turn off the power before installing or replacing any component.

INSTALLING MATH COPROCESSOR

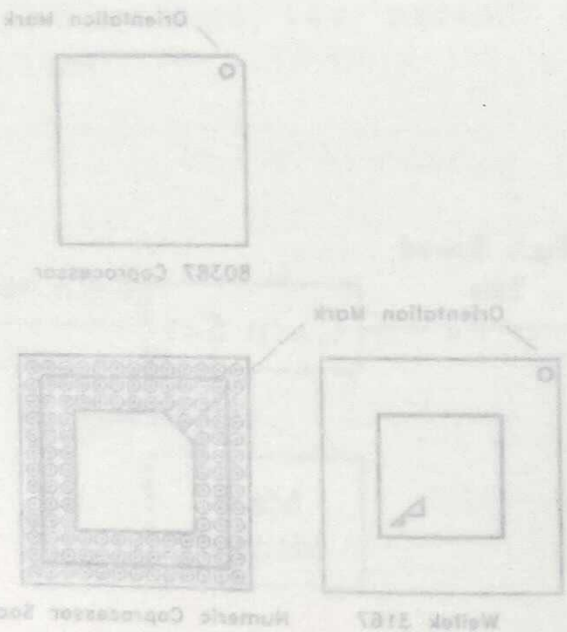
Math coprocessor 80387 and WEITEK 3167 are PGA devices. Beside the CPU, there is a 121-pin PGA socket. To install Math coprocessor, be sure to line up pin 1 of the Math coprocessor with pin 1 of the socket as shown below. Make sure that the coprocessor is firmly inserted into the socket.



The WEITEK 3167 is a 121-pin chip which matches the pin count of the socket. Align the pins and gently insert the chip into the socket. However, 80387 has 69 pins and its package is smaller and different from WEITEK 3167. So, it only occupies the inner pins of the socket.

Before installing the Math coprocessor, make sure all the pins are straight. The pins are very fragile. Once these pins are bent, the coprocessor may be damaged.

Check whether the system BIOS can find the coprocessor after reset. The system BIOS will display a list of devices on the motherboard after self-test. If the coprocessor is installed, it should show the type of coprocessor.



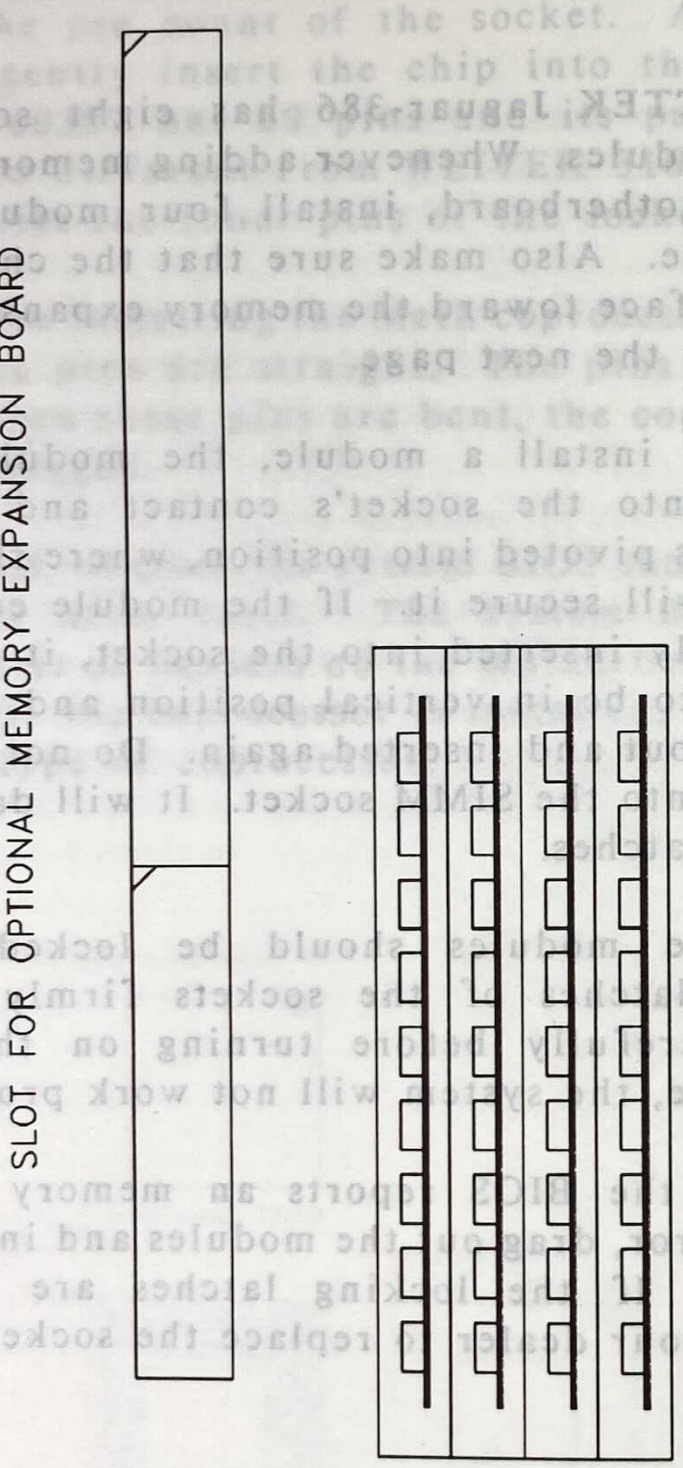
INSTALLING RAM MODULES

OCTEK Jaguar-386 has eight sockets for SIMM modules. Whenever adding memory modules to the motherboard, install four modules at the same time. Also make sure that the chips on the modules face toward the memory expansion slot as shown in the next page.

To install a module, the module edge is angled into the socket's contact and then the module is pivoted into position, where the locking latches will secure it. If the module edge is not completely inserted into the socket, it cannot be pivoted to be in vertical position and should be dragged out and inserted again. Do not force the module into the SIMM socket. It will damage the locking latches.

The modules should be locked by the locking latches of the sockets firmly. Please check carefully before turning on the power. Otherwise, the system will not work properly.

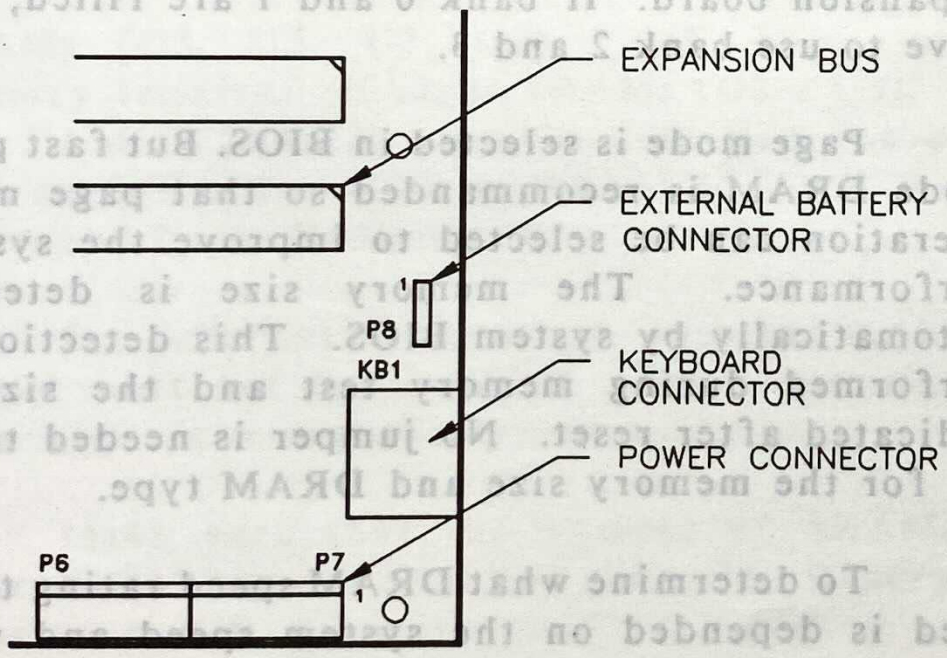
If the BIOS reports an memory error or parity error, drag out the modules and insert them again. If the locking latches are damaged, contact your dealer to replace the socket.



Installing RAM Modules

INSTALLING EXTERNAL BATTERY

To back up the information stored in CMOS RAM, an external battery is needed to provide power after the system is turned off. The connector (P8) for the battery is located beside the keyboard connector on the rear of the board. A 3.6V battery is used. Turn off the power before install the battery. The location of the connector P8 is shown below.



CONFIGURATION OF MEMORY

The configuration of the memory is very flexible. Either 256KB or 1MB SIMM modules are acceptable. There are several combinations of DRAM types you may consider. So, a basic system can be equipped with fewer memory and the system can be upgraded by installing the extended memory. The different configurations of memory is illustrated at the next page.

There are totally four banks of DRAM. Two banks (bank 0 and 1) are on the motherboard and the others (bank 2 and 3) are on the memory expansion board. If bank 0 and 1 are filled, you have to use bank 2 and 3.

Page mode is selected in BIOS. But fast page mode DRAM is recommanded so that page mode operation can be selected to improve the system performance. The memory size is detected automatically by system BIOS. This detection is performed during memory test and the size is indicated after reset. No jumper is needed to be set for the memory size and DRAM type.

To determine what DRAM speed rating to be used is depended on the system speed and wait state. The highest performance is accomplished by using zero wait state, but high speed DRAM has to be used.

The wait state setting is applied to four banks of memory. Therefore make sure to install DRAM modules with the same speed rating, or accommodate the wait state setting to the new DRAM type.

The number of wait state is assigned in the BIOS setup. Improper setting may cause the system malfunction. In this case, reset the CMOS setup using JP7. Then reset the system and go through the system setup again.

DRAM CONFIGURATION

	Bank 0 SIMM (1-4)	Bank 1 SIMM (5-8)	Bank 2 SIMM (9-12)	Bank 3 SIMM (13-16)	Total Memory
1	256K				1M
2	256K	256K			2M
3	1M				4M
4	256K	1M			5M
5	1M	1M			8M
6	1M	1M	1M		12M
7	1M	1M	1M	1M	16M

CONFIGURATION OF CACHE MEMORY

Note : If you have any question about the configuration of cache memory, consult your local dealer. Improper configuration will cause the system malfunction.

The external cache memory is either 32K or 64K bytes. 32K bytes is sufficient for general applications and the performance is improved when the size is increased to 64K bytes.

32K bytes cache memory requires four SRAMs (U3, U5, U7, U9). 64K bytes cache memory requires all eight SRAMs (U2 - U9). The tag RAM (U21-U22) must be installed for both 64K or 32K. The type of SRAM is 8K X 8 and the type of tag RAM is 16K x 4.

For internal cache mode, both tag RAM or SRAM must not be installed. Otherwise all the data will crash and the system will hang.

Make sure that the number of SRAMs is correct and they are installed properly. Otherwise the system will not work.

The speed rating of the SRAM for 25MHz and 33MHz motherboard are listed below:

System Speed	SRAM	Tag RAM
33MHz	25ns	15ns
25MHz	35ns	25ns

The jumper settings for the configuration of cache memory.

Cache Memory Size

	32KB	64KB
JP6	1-2	2-3

Internal Cache

	128 byte
JP1 - JP4	1-2

Note: For external cache, JP1 - JP4 must not be installed.

CONTROL OF SYSTEM SPEED

System Speed can be controlled by hardware switch and keyboard. Connector P3 is connected to the turbo switch of the case. When the system speed is fast, the turbo LED of the case should be turned on.

To change the speed by keyboard, use '-' and '+' of the numeric keypad. Press 'Ctrl', 'Alt' and '-' for slow speed and Press 'Ctrl', 'Alt' and '+' for fast speed.

Whenever the system speed is set to slow by turbo switch, it cannot be changed by keyboard, and vice versa.

RESET CMOS SETUP INFORMATION

Sometimes, the improper setting of system setup may make the system malfunction. In this case, turn off the power and disconnect the external battery. Then place a jumper on JP7 (1-2) for a while. The internal CMOS status register will be cleared. Then remove the jumper and turn on the power. The BIOS finds the CMOS status register is reset and regards the setup information as invalid. So it will prompt you to correct the information. In normal operation, JP7 place in (2-3).

SYSTEM BOARD JUMPER SETTING

There are several options which allow user to select by hardware switches.

Display Selection

JP8	
1-2	CGA, EGA, VGA
2-3	Monochrome display *

Parity Check

JP5	Parity Check
1-2	Enable
2-3	Disable *

Note : * factory setting

SYSTEM BOARD CONNECTORS

Under typical conditions, these connectors should be connected to the indicators and switches of the system unit.

Connector	Function
P1	Hardware reset connector
P2	Speaker connector
P3	Turbo switch connector
P4	Turbo LED connector
P5	Power LED & Ext-Lock connector
P6, P7	Power supply connector
P8	External battery connector
KB1	Keyboard connector

Pin assignments of the connectors are illustrated as follows:

P 1 - Hardware Reset Connector

Pin	Assignment
1	Selection Pin
2	Ground

P 2 - Speaker Connector

Pin	Assignment
1	Data out
2	+5 Vdc
3	Ground
4	+5 Vdc

P 3 - Turbo Switch Connector

Pin	Assignment
1	Selection Pin
2	Ground

P 4 - Turbo LED Connector

Pin	Assignment
1	+5 Vdc
2	LED signal

P 5 - Power LED & Ext-Lock Connector

Pin	Assignment
1	+5 Vdc
2	Key
3	Ground
4	Keyboard inhibit
5	Ground

P6, P7 - Power Supply Connector

Pin	Assignment
1	POWERGOOD
2	+5 Vdc
3	+12 Vdc
4	-12 Vdc
5	Ground
6	Ground

Pin	Assignment
1	Ground
2	Ground
3	-5 Vdc
4	+5 Vdc
5	+5 Vdc
6	+5 Vdc

P 8 - External Battery Connector

Pin	Assignment
1	+ Vdc
2	not used
3	Ground
4	Ground

KB 1 - Keyboard Connector

Pin	Assignment
1	Keyboard clock
2	Keyboard data
3	Spare
4	Ground
5	+5 Vdc

Chapter 4
Technical Information

This section provides technical information about OCTEK Jaguar-386 and is intended for advanced users interested in the basic design and operation of OCTEK Jaguar-386.

MEMORY MAPPING

Address	Range	Function
000000-7FFFFF	000K-512K	System Board Memory (512K)
080000-09FFFF	512K-640K	System Board Memory (128K)
0A0000-0BFFFF	640K-768K	Display Buffer (128K)
0C0000-0DFFFF	768K-896K	Adaptor ROM / Shadow RAM (128K)
0E0000-0EFFFF	896K-960K	System ROM / Shadow RAM (64K)
0F0000-0FFFFF	960K-1024K	System BIOS ROM / Shadow RAM (64K)
100000-7FFFFF	1024K-8192K	System Memory
800000-FFFFFF	8192K-16318K	System Memory