

**HIPPO 10  
486**



*User's  
Manual*

# RADIO FREQUENCY INTERFERENCE STATEMENTS

This equipment generates and uses radio frequency energy and if not installed and used properly, it may cause radio frequency interference with other electronic equipment. This interference may cause interference with radio and television reception.

If this equipment does cause interference to radio or TV reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- The CPU board
- The DRAM board
- Relocate the computer away from the receiver.
- Move the computer away from the receiver.
- Plug the computer into a different outlet so that computer and receiver are on different branch circuits.
- \* Ensure that card slot sockets are tightly secured.
- \* Ensure that card mounting screws are tightly secured.
- \* If peripherals are used with this system, it is suggested to use shielded ground wires.

## Chapter 4 Installation Information

The material in this manual is for information only and is subject to change without notice.

### REVISION: 1.2

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## RADIO FREQUENCY INTERFERENCE STATEMENT

This equipment generates and uses radio frequency energy and if not installed and used properly, that is, in strict accordance with the manufacturer's instructions, may cause interference with radio and television reception.

If this equipment does cause interference to radio or TV reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- \* Reorient the receiving antenna.
- \* Relocate the computer away from the receiver.
- \* Move the computer away from the receiver.
- \* Plug the computer into a different outlet so that computer and receiver are on different branch circuits.
- \* Ensure that card slot covers are in place when no card is installed.
- \* Ensure that card mounting screws, attachment connector screws, and ground wires are tightly secured.
- \* If peripherals are used with this system, it is suggested to use shielded, grounded cables, with in-line filters if necessary.

If necessary, the user should consult the dealer service representative for additional suggestions.

The manufacturer is not responsible for any radio or TV interference caused by unauthorized modifications to this equipment. It is the responsibility of the user to correct such interference.

## Table of Content

### Chapter 1 Introduction

Introduction..... 1-1

### Chapter 2 General Features

Specification..... 2-1

Board Layout..... 2-3

The 80486 CPU ..... 2-4

The DRAM System..... 2-5

DRAM Configuration ..... 2-6

### Chapter 3 Installation

Installing DRAM Modules ..... 3-1

Jumper Setting ..... 3-2

System Board Connectors..... 3-7

### Chapter 4 Technical Information

Memory Map..... 4-1

I/O Map..... 4-2

System Interrupts ..... 4-4

Direct Memory Access..... 4-5

## Appendix A Operation and Maintenance

Static Electricity .....	A-1
Keeping The System Cool .....	A-1
Cleaning The "Golden Finger" .....	A-2
Cleaning The Motherboard .....	A-3

## Chapter One Introduction

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The usage of PC systems in the office environment has seen dramatic increase over this few years. With increase in the power consumption due to growth of the PC installation base, the United States Environmental Protection Agency (EPA) issued a guideline stating that systems must have the capability to be put into a low power state (less than 30 W) during period of inactivity to conserve energy. Therefore the major benefit of incorporating power management to desktop PCs is to reduce electrical operating cost over the lifetime of the system.

OCTEK HIPPO 10 brings the new technology of power saving to desktop computing. Compliance with the EPA requirement, high throughput VESA Local Bus, advanced chipset with power user-programmable features and integrated on-board I/O are some of the real benefits of HIPPO 10.

The key components of the advanced power-saving capabilities are HIPPO 10's built-in support of DPMS functions (Display Power Management Standard) of VESA (Video Electronics Standard Association), support for Windows APM and CPU clock step-down hardware. The energy saving feature of HIPPO 10 is compatible with MS-DOS 5.0 (or later versions) and Windows 3.1.



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The key components of the advanced power-saving capabilities are HIPPO 10's built-in support of DPM2 functions (Display Power Management Standard) or VESA (Video Electronics Standard Association) support for Windows APM and CPU clock step-down hardware. The energy saving feature of HIPPO 10 is compatible with MS-DOS 2.0 (or later versions) and Windows 3.1.

# Chapter Two General Features

## Specifications:

- Processor:** 80486DX, 80486DX2, 80486DX4, 486 SL-enhance, UMC P5, CX 486DX, CX 486DX2, 80486SX or 80487SX
  
- Processor Clock:** 25 / 33 / 40 / 50 MHz clock selectable
  
- Speed:** Turbo/normal speed
  
- Expansion Bus:** Six 16-bit ISA slots  
Two VESA Local Bus slots (supporting Two VL master)
  
- On-board VESA Local Bus Device:** VL-IDE controller
  
- DRAM Upgrade Capacity:** 4 MB (min. config.)  
64 MB (max. config.)

## DRAM

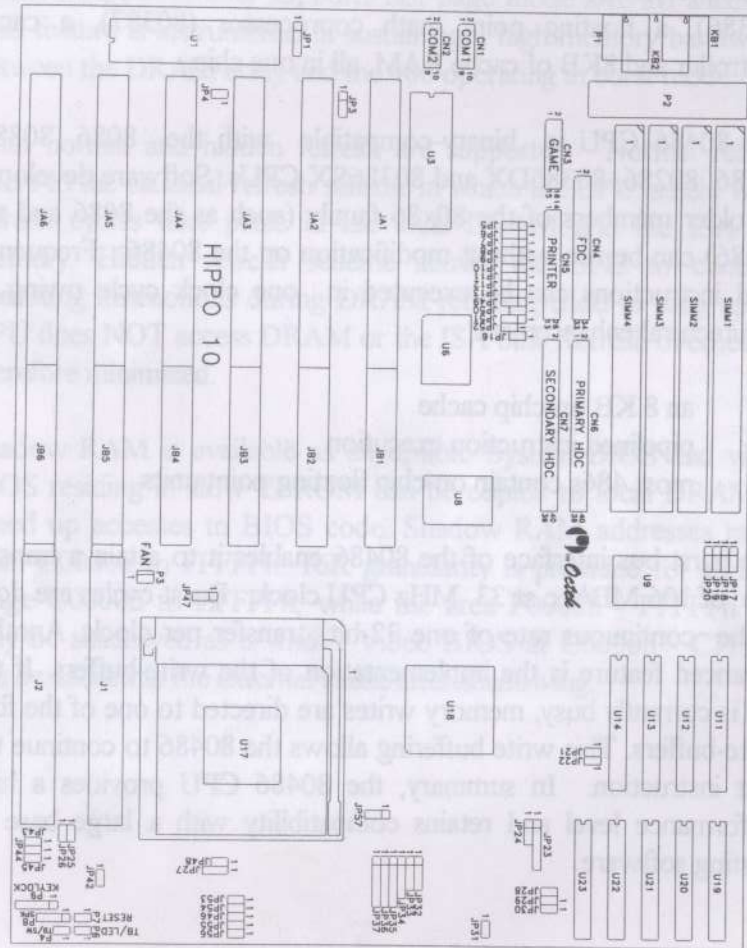
**Configuration:** 72 pin SIMM sockets for 1M x 32,  
2M x 32, 4M x 32 or x 36

**Cache :** 8 KB internal cache in CPU  
128K, 256K, 512K secondary  
cache

**On-board  
I/O Facility:** Floppy controller  
2 serial ports  
1 parallel port  
1 game port

**Power Saving  
Feature:** Support SMM for power management  
CPU with programmable SMM region

## Board Layout





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## The 80486 CPU

In simple terms, an 80486 is a combination of a microprocessor (80386), a floating point math coprocessor (80387), a cache controller and 8KB of cache RAM, all in one chip.

The 80486 CPU is binary-compatible with the 8086, 8088, 80186, 80286, 80386DX and 80386SX CPUs. Software developed for older members of the 80x86 family (such as the 8086 and the 80286) can be run without modification on the 80486. Frequently used instructions can be executed in one clock cycle owing to architectural enhancement:

1. an 8 KB on-chip cache
2. pipelined instruction execution
3. most 486s contain on-chip floating point units

The burst bus interface of the 80486 enables it to attain a transfer rate of 106 MB/sec at 33 MHz CPU clock. Burst cycles are done at the continuous rate of one 32-bit transfer per clock. Another advanced feature is the implementation of the write-buffers. If the bus is currently busy, memory writes are directed to one of the four write-buffers. This write buffering allows the 80486 to continue the next instruction. In summary, the 80486 CPU provides a high performance level and retains compatibility with a large base of existing software.

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## The DRAM System

The memory controller supports fast page mode DRAM accesses. This feature is instrumental in sustaining a high memory bandwidth between the DRAM array and the 486 operating in burst mode.

Both normal and hidden refresh are supported. Normal refresh refers to the classical refresh scheme in which the CPU is held while refresh cycles take place in the local DRAM and the ISA bus memory. Hidden refresh scheme allows the CPU to continue executing instructions during DRAM refresh period as long as the CPU does NOT access DRAM or the ISA bus. Refresh overhead is therefore minimized.

Shadow RAM is available as an option. System BIOS and video BIOS residing in slow EPROM can be copied to local DRAM to speed up accesses to BIOS code. Shadow RAM addresses range from C0000h to FFFFFh. 16K granularity is provided for address range C0000h to EFFFFh, while the area F0000h - FFFFFh can only be shadowed as a whole. Video BIOS at C0000h - C7FFFh can be cached in the external cache after shadowing.



## DRAM Configuration

Bank 1	Bank 2	Bank 3	Bank 4	Total
1Mx32				4M
1Mx32	1Mx32			8M
2Mx32				8M
1Mx32	1Mx32	1Mx32		12M
1Mx32	2Mx32			12M
1Mx32	1Mx32	1Mx32	1Mx32	16M
1Mx32	2Mx32	1Mx32		16M
2Mx32	2Mx32			16M
4Mx32				16M
1Mx32	4Mx32			20M
1Mx32	1Mx32	4Mx32		24M
2Mx32	4Mx32			24M
1Mx32	2Mx32	4Mx32		28M
4Mx32	4Mx32			32M
1Mx32	4Mx32	4Mx32		36M
4Mx32	2Mx32	4Mx32		40M
1Mx32	1Mx32	4Mx32	4Mx32	40M
4Mx32	4Mx32	4Mx32		48M
1Mx32	4Mx32	4Mx32	4Mx32	52M
4Mx32	4Mx32	4Mx32	4Mx32	64M

70ns DRAM can be used in all operating frequencies. System BIOS is auto enable the parity check when 36-bit SIMM modules is inserted.

## The External Cache System

An external cache is available to boost the system performance. The external cache is direct-mapped and employs a write-back scheme. The cache sizes are 128K, 256K, 512K.

## VESA Local Bus

Connecting devices to a CPU local bus can dramatically increase the speed of the I/O bound peripherals. The Video Electronics Standards Association (VESA) VL Bus is a widely accepted local bus standard.

## Maximum Number of VL-Bus Devices And Slots

The following guidelines are recommended by VESA:

Speed	Max. no. of VL adapter cards installed
33MHz	2
40MHz	2
50MHz	1



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## The On-board VL IDE

The VL Local Bus IDE controller supports enhance IDE mode 3 features. The IDE controller is fully compatible with ANSI ATA rev 3.x - 4.0 specification for IDE hard disk operations. The chip incorporates 32 bit late read/write operation up to 50Mhz. Double-word read and write operation are provided via internal control and conversion logic. It supports anti-virus write protection by hardware controlled disk accuracy range for one partition table or whole drive.

## The On-board I/O Controller

The on-board I/O controller offers

1. support for two floppy drives ( 360K 5 1/4", 1.2M 5 1/4", 720K 3 1/2", 1.44M 3 1/2" )
2. one parallel port
3. two serial ports
4. game port
5. Optional ECP,EPP high performance parallel port

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## Control Of System Speed

System speed can be controlled by the keyboard and the turbo switch. When the keys "Ctrl", "Alt", "-" are pressed simultaneously, the system switches to low speed. When the keys "Ctrl", "Alt", "+" are pressed at the same time, the system returns to high speed mode (turbo mode).

The header P4 should be connected to the turbo switch of the cabinet. Whenever the system speed is set low by the turbo switch, the key strobes "Ctrl", "Alt", "+" and "Ctrl", "Alt", "-" will have NO impact on the system speed.

## Power Saving Features

Whenever the system is not in used (e.g. No key has been hit in the keyboard for a certain period of time), the clock chip of the main board will be signaled to slow down the CPU clock. The system subsequently enters a "sleep" mode. When an external request for system usage is detected (as the pressing of a key or the movement of a mouse), the clock is stepped up to full operating frequency. The time limit for entry to "sleep" mode is selectable in CMOS setup.

IDE drive spin-down is also controllable. The fixed disk will stop spinning after a pre-selected time interval of inactivity.

## Reset CMOS Setup Information

Sometimes it may be desirable to clear the existing content of the CMOS RAM. This may be accomplished by allowing the shunt connector to join pin 3 and pin 4 of the header at JP1 for a while. When the system is re-booted, CMOS RAM content is regarded as invalid and the user is prompted to setup the CMOS again. In normal operation, JP1 place (2-3).

# Chapter Three Installation

## Installing DRAM modules

Follow the steps below to install DRAM SIMMs :

- (a) Turn off the PC.
- (b) The SIMM RAM is inserted in SIMM socket 0 first. The memory modules should be carefully installed into the SIMM sockets in such a way that the modules are properly oriented and aligned.
- (c) Allow the two metal latches at each end of the socket to lock onto the memory module.
- (d) Further memory capacity upgrade should be directed to SIMM 1.



## Jumper Setting

### Cache Configuration

	512K (128Kx8) U11-U14	256K (32Kx8) U11-U14, U19-U22	256K (64Kx8) U11-U14	128K (32Kx8) U11-U14
JP21	Close	Open	Open	Open
JP22	Close	Close	Close	Open
JP23	1-2,3-4, 5-6	3-4	2-3, 4-5	2-3
JP24	1-2	2-3	1-2	1-2

For 33MHz clock, the tag RAM 32Kx8 is used 20ns and 40mhz or 50mhz system, 15ns RAM is used (U23).

### Clock Selection

JP28	JP29	JP30	Clock Frequency	CPU
Close	Open	Open	50MHz	DX50
Close	Close	Close	33MHz	DX33,DX2-66 DX4-100
Open	Close	Close	40MHz	DX40,DX2-80
Open	Open	Close	25MHz	DX25,DX2-50

### On-board Floppy Controller

JP7	
1-2	enabled
2-3	disabled

### On-board Game Port

JP9	
1-2	enabled
2-3	disabled

### On-board Printer Port

JP5	JP6	
2-3	2-3	disable
1-2	2-3	SPP mode
2-3	1-2	EPP mode
1-2	1-2	ECP mode

### Printer Port Selection

JP8	
1-2	LPT1 (378H)
2-3	LPT2 (278H)

### Serial Port 1

JP10	
1-2	enabled
2-3	disabled

JP11	
1-2	COM1 (3F8 - 3FFh)
2-3	COM3 (3E8 - 3EFh)



## Serial Port 2

JP12	
1-2	enabled
2-3	disabled

JP13	
1-2	COM2 (2F8 - 2Ffh)
2-3	COM4 (2E8 - 2EFh)

## VL Slot configuration

JP25	
Close	1 WS VL-write cycle
Open	0 WS VL-write cycle

JP26 VL-bus ID3	
Close	VL slot clock greater than 33.333MHz
Open	VL slot clock less than or equal to 33.333mhz

## CPU Voltage

TYPE	CPUVCC	JP46	JP48	JP53	JP54	JP55	JP56
AUTO	5V/3.45V	OPEN	OPEN	1-2	OPEN	OPEN	OPEN
FIXED	5V	OPEN	OPEN	OPEN	1-2	OPEN	OPEN
FIXED	4V	OPEN	OPEN	OPEN	OPEN	OPEN	1-2
FIXED	3.8V	OPEN	OPEN	OPEN	OPEN	1-2	OPEN
FIXED	3.6V	1-2	OPEN	OPEN	OPEN	OPEN	OPEN
FIXED	3.45V	OPEN	OPEN	OPEN	OPEN	OPEN	OPEN
FIXED	3.3V	OPEN	1-2	OPEN	OPEN	OPEN	OPEN

AND 103

pro NB rev. 1.11 adylousens  
 5V 1-2 OPEN  
 3.6V OPEN OPEN  
 3.45V OPEN 1-2  
 AND 103 →

JP 37 pin 6 GAP VOLDET

## CPU Type

	JP32	JP33	JP34	JP35	JP36	JP37	JP57
Intel 486SX	Open	2-3	Open	Open	Open	2-3	Open
Intel 486DX/DX2	1-2	1-2	Open	Open	Open	2-3	Open
Intel SL 486DX/DX2/DX4	1-2	1-2	1-2	1-2	5-6	1-2	Open
AMD Enhanced AM486DX/DX2/DX4		3-4	3-4				
Intel P24D	1-2	1-2	1-2	1-2	3-4	1-2	Open
Intel P24T	2-3	1-2	1-2	1-2	5-6	1-2	Open
Cyrix SX	Open	2-3	2-3	1-2	2-3	1-2	Open
			4-5	3-4	4-5	3-4	
				5-6		5-6	
Cyrix DX/DX2	1-2	1-2	2-3	1-2	2-3	1-2	Open
		3-4		3-4	4-5	3-4	
				5-6		5-6	
UMC CPU Am486DX2	3-4	2-3	Open	2-3	1-2	2-3	Open
Am486DX4	1-2	1-2	Open	2-3	1-2	2-3	2-3
	3-4	3-4					

AND 486x5-113 1-2 1-2 1-2 1-2 3-4 1-2 OPEN  
 3-4 3-4

JP27 INTEL 486DX4 / AMD Enhanced 486DX4 CLK Multiple	
Open	CLK 3x
1-2	CLK 2.5x
2-3	CLK 2x

AND 486x5-113  
 new find new end  
 4x

with bios 096003

## Suspend Mode

JP43	
Open	Normal
Close	System Suspend



## Reserved Jumpers

JP2	open
JP3	1-2
JP4	close
JP16	open
JP31	1-2
JP42	open
JP46	open
JP47	2-3
JP48	open
JP49	open
JP50	1-2
JP51	open
JP52	1-2

## On-board IDE

JP19 Secondary IDE	
1-2	enabled
2-3	disabled

JP20 Primary IDE	
1-2	enabled
2-3	disabled

JP17	JP18	speed
2-3	2-3	faster
2-3	1-2	fast
1-2	2-3	slow
1-2	1-2	slower

The JP18, JP19 jumper can be override by CMOS setting.

## System Board Connectors

	Description
P2	Power Connectors
P3	Cooling Fan Connector
P4	Turbo Switch
P6	Turbo LED Connector
P7	Hardware Reset Switch
P8	Speaker Connector
P9	Power LED and Keylock Connector
JP44	Hard Disk LED Connector (primary)
JP45	Hard Disk LED Connector (secondary)
CN1	COM 1/3 Serial Port Connectors
CN2	COM 2/4 Serial Port Connector
CN3	Game Port Connector
CN4	Floppy Drive Connector
CN5	Parallel Port Connector
CN6	IDE Hard Disk Connector (primary)
CN7	IDE Hard Disk Connector (secondary)
JP1	External Battery Connector
KB2	Keyboard Connector

## P2 Power Connectors

Pin	Assignment
1	Power Good
2	+5V
3	+12V
4	-12V
5	Ground
6	Ground

Pin	Assignment
1	Ground
2	Ground
3	-5V
4	+5V
5	+5V
6	+5V

## P3 Cooling Fan Connector

Pin	Assignment
1	GND
6	+5V

## P4 Turbo Switch

Pin	Assignment
1	Signal pin
2	Ground

## P6 Turbo LED Connector

Pin	Assignment
1	LED Signal
2	+5V

## P7 Hardware Reset Switch

Pin	Assignment
1	Signal pin
2	GND

## P8 Speaker Connector

Pin	Assignment
1	Data out
2	NC
3	Ground
4	+5V

## P9 Power LED & Keylock Connector

Pin	Assignment
1	+5V
2	Key
3	Ground
4	Keyboard inhibit
5	Ground



## JP1 External Battery Connector

Pin	Assignment
1	External Battery Input
2	On-board Battery +3.6V
3	On-board Battery Input
4	Ground

# Chapter Four Technical Information

This section provides technical information about Hippo 10 and is particularly useful to advanced users.

## Memory Map

Address	Range	Function
0-9FFFFh	0K-640K	Base Memory
A0000-BFFFFh	640K-768K	Video Display Buffer
C0000-DFFFFh	768K-896K	Adapter ROM
E0000-EFFFFh	896K-960K	System ROM (optional)
F0000-FFFFFFh	960K-1024K	System ROM
100000-1FFFFFFh	1024K-2048K	Extended Memory

## I/O Address Map

ADDRESS (HEX)	DEVICE
000-01Fh	DMA Controller 1
020-03Fh	Interrupt Controller 1
040-05Fh	Timer
060-06Fh	Keyboard Controller
070-07Fh	Real Time Clock
080-09Fh	DMA Page Register
0A0-0BFh	Interrupt Controller
0C0-0DFh	DMA Controller 2
0F0	Clear Math Coprocessor Busy Flag
0F1	Reset Math Coprocessor
0F8-0FFh	Math Coprocessor Port

ADDRESS (HEX)	DEVICE
170-177h	Fixed Disk (secondary)
1F0-1F7h	Fixed Disk (primary)
200-207h	Game Port
278-27Fh	Parallel Port 2
2E8-2EFh	Serial Port 4
2F8-2FFh	Serial Port 2
300-31Fh	Prototype Card
360-36Fh	Reserved
370-377h	Floppy Disk Controller (secondary)
378-37Fh	Parallel Port 1
380-38Fh	SDLC, bisync 2
3A0-3AFh	Bisync 1
3B0-3BFh	Monochrome Display and Printer Adapter
3C0-3CFh	Reserved
3D0-3DFh	Color Graphics Adapter
3E8-3EFh	Serial Port 3
3F0-3F7h	Floppy Disk Controller (primary)
3F8-3FFh	Serial Port 1



## System Interrupts

Level	Function
Microprocessor NMI	Parity or I/O Channel Check
Interrupt Controllers	
CTLR 1	CTLR 2
IRQ0	Timer Output 0
IRQ1	Keyboard
IRQ2	<ul style="list-style-type: none"> <li>IRQ8 Real-time Clock Interrupt</li> <li>IRQ9 Software Redirected to INT 0AH (IRQ2)</li> <li>IRQ10 Reserved</li> <li>IRQ11 Reserved</li> <li>IRQ12 Reserved</li> <li>IRQ13 Coprocessor</li> <li>IRQ14 Fixed Disk Controller</li> <li>IRQ15 Reserved</li> </ul>
IRQ3	Serial Port 2
IRQ4	Serial Port 1
IRQ5	Parallel Port 2
IRQ6	Diskette Controller
IRQ7	Parallel Port 1

## Direct Memory Access (DMA)

Channel	Function
0	Spare (8 bit transfer)
1	SDLC (8 bit transfer)
2	Floppy Disk (8 bit transfer)
3	Spare (8 bit transfer)
4	Cascade for DMA Controller 1
5	Spare (16 bit transfer)
6	Spare (16 bit transfer)
7	Spare (16 bit transfer)

## VL-slot Pinout

The "A" side of the connector is the add-in board component side. The "B" side of the connector is the add-in board solder side.

### VL-slot (side A)

I/O Pin	Signal Name
A1	D1
A2	D3
A3	GROUND
A4	D5
A5	D7
A6	D9
A7	D11
A8	D13
A9	D15
A10	GROUND
A11	D17
A12	VCC
A13	D19
A14	D21
A15	D23
A16	D25
A17	GROUND
A18	D27
A19	D29
A20	D31
A21	A30
A22	A28
A23	A26
A24	GROUND
A25	A24
A26	A22
A27	VCC
A28	A20

I/O Pin	Signal Name
A29	A18
A30	A16
A31	A14
A32	A12
A33	A10
A34	A8
A35	GROUND
A36	A6
A37	A4
A38	WBACK#
A39	BEO#
A40	VCC
A41	BE1#
A42	BE2#
A43	GROUND
A44	BE3#
A45	ADS#
A48	LRDY#
A49	LDEV#
A50	LREQ#
A51	GROUND
A52	LGNT#
A53	VCC
A54	ID2
A55	ID3
A56	ID4
A57	LKEN#
A58	LEADS#



VL-slot (side B)

I/O Pin	Signal Name
B1	D0
B2	D2
B3	D4
B4	D6
B5	D8
B6	GROUND
B7	D10
B8	D12
B9	VCC
B10	D14
B11	D16
B12	D18
B13	D20
B14	GROUND
B15	D22
B16	D24
B17	D26
B18	D28
B19	D30
B20	VCC
B21	A31
B22	GROUND
B23	A29
B24	A27
B25	A25
B26	A23
B27	A21
B28	A19

A21	A21
A22	A23
A23	A25
A24	GROUND
A25	A27
A26	A29
A27	VCC
A28	A31

ISA Slot (side B)

I/O Pin	Signal Name
B29	GROUND
B30	A17
B31	A15
B32	VCC
B33	A13
B34	A11
B35	A9
B36	A7
B37	A5
B38	GROUND
B39	A3
B40	A2
B41	N/C
B42	RESET#
B43	D/C#
B44	M/IO#
B45	W/R#
B48	RDYRTN#
B49	GROUND
B50	IRQ9
B51	BRDY#
B52	BLAST#
B53	ID0
B54	ID1
B55	GROUND
B56	VLCLK
B57	VCC
B58	LBS16#

B29	GROUND
B30	A17
B31	A15
B32	VCC
B33	A13
B34	A11
B35	A9
B36	A7
B37	A5
B38	GROUND
B39	A3
B40	A2
B41	N/C
B42	RESET#
B43	D/C#
B44	M/IO#
B45	W/R#
B48	RDYRTN#
B49	GROUND
B50	IRQ9
B51	BRDY#
B52	BLAST#
B53	ID0
B54	ID1
B55	GROUND
B56	VLCLK
B57	VCC
B58	LBS16#

ISA slot (side A)

I/O Pin	Signal Name
A1	-I/O CH CK
A2	SD7
A3	SD6
A4	SD5
A5	SD4
A6	SD3
A7	SD2
A8	SD1
A9	SD0
A10	-I/O CH RDY
A11	AEN
A12	SA19
A13	SA18
A14	SA17
A15	SA16
A16	SA15
A17	SA14
A18	SA13
A19	SA12
A20	SA11
A21	SA10
A22	SA9
A23	SA8
A24	SA7
A25	SA6
A26	SA5
A27	SA4
A28	SA3
A29	SA2
A30	SA1
A31	SA0

ISA Slot (side B)

I/O Pin	Signal Name
B1	GND
B2	RESET DRV
B3	+5 Vdc
B4	IRQ9
B5	-5 Vdc
B6	DRQ2
B7	-12 Vdc
B8	0WS
B9	+12 Vdc
B10	GND
B11	-SMEMW
B12	-SMEMR
B13	-IOW
B14	-IOR
B15	-DACK3
B16	DRQ3
B17	-DACK1
B18	DRQ1
B19	-Refresh
B20	CLK
B21	IRQ7
B22	IRQ6
B23	IRQ5
B24	IRQ4
B25	IRQ3
B26	-DACK2
B27	T/C
B28	BALE
B29	+5 Vdc
B30	OSC
B31	GND



### ISA slot (side C)

I/O Pin	Signal Name
C1	SBHE
C2	LA23
C3	LA22
C4	LA21
C5	LA20
C6	LA19
C7	LA18
C8	LA17
C9	-MEMR
C10	-MEMW
C11	SD8
C12	SD9
C13	SD10
C14	SD11
C15	SD12
C16	SD13
C17	SD14
C18	SD15

### ISA slot (side D)

I/O Pin	Signal Name
D1	-MEM CS16
D2	-I/O CS16
D3	IRQ10
D4	IRQ11
D5	IRQ12
D6	IRQ15
D7	IRQ14
D8	-DACK0
D9	DRQ0
D10	-DACK5
D11	DRQ5
D12	-DACK6
D13	DRQ6
D14	-DACK7
D15	DRQ7
D16	+5 Vdc
D17	-MASTER
D18	GND

## Appendix A

# Operation and Maintenance

### Static Electricity

When installing or removing any add-on card, DRAM module or processor, you should discharge the static electricity on your body. Static electricity is dangerous to electronic device and can build-up on your body. When you touch the add-on card or motherboard, it is likely to damage the device. To discharge the static electricity, touch the metal of your computer. When handling the add-on card, don't contact the components on the cards or their "golden finger". Hold the cards by their edges.

### Keeping The System Cool

The motherboard contains many high-speed components and they will generate heat during operation. Other add-on cards and hard disk drive can also produce a lot of heat. The temperature inside the computer system may be very high. In order to keep the system running stably, the temperature must be kept at a low level. A easy way to do this is to keep the cool air circulating inside the case. The power supply contains a fan to blow air out of the case. If you find that the temperature is still very high, it would be better to install another fan inside the case. Using a larger case is recommended if there are a number of add-on cards and disk drives in the system.



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## Cleaning The "Golden Finger"

Whenever inserting an add-on card to the motherboard, make sure that there is no dirt on the "golden finger" of the add-on card. If not, the contact between the "golden finger" and the slot may be poor and thus the add-on card may not work properly. Use a pencil eraser to clean the "golden finger" if dirt is found.

## Cleaning The Motherboard

The computer system should be kept clean. Dust and dirt is harmful to electronic devices. To prevent dust from accumulating on the mother-board, installing all mounting plates on the rear of the case. Regularly examine your system, and if necessary, vacuum the interior of the system with a miniature vacuum.