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Motherboard Layout and Information for Models With a Via 694X Chipset and an Intel Pentium (R) III Processor

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HP Pavilion models with this motherboard

The following HP Pavilion PC models ship with a motherboard containing the Via 694X Chipset and Pentium III Processor:

| HP Pavilion X6xx Series | HP Pavilion X7xx and XLxxx Series |
|--------------------------------|-----------------------------------|
| 8628 (AP) | 8700I (US) |
| 8629 (AP) | 8705I (US) |
| 8631 (AP) | 8722 (France) |
| 8632 (AP) | 8725 (France) |
| 8636 (AP) | 8740 (France) |
| 8660 (Sweden) | 8760C (US) |
| 8660 (Norway) | 8775C (US/Canada) |
| 8674D (US) | 8785C (US/Canada) |
| 8674F (US) | XL766 (US) |
| 8680 (France) | |
| 8680 (Norway) | |
| 8680 (Sweden) | |

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| 9000L (US) |
|------------|

System board layout

Figure 1: Motherboard layout



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1 - TV out chip

2 - System battery

3 - PCI connectors

4 - AGP port

5 - Socket 370 processor connector

6 - DIMM sockets (memory)

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Jumper locations and functions

There are no jumper blocks to set on this motherboard.

About system memory

The motherboard has three dual in-line memory module (DIMM) sockets. Minimum memory size is 16 MB; maximum memory size is 768 MB. The BIOS automatically detects memory type, size, and speed.

The motherboard supports the following memory features:

- 168-pin DIMMs with gold-plated contacts
- 100 MHz SDRAM depending on system
- Non-ECC (64-bit) and ECC (72-bit) memory
- 3 V memory only
- Single- or double-sided DIMMs

SDRAM

Synchronous DRAM (SDRAM) improves memory performance through memory access that is synchronous with the memory clock. This simplifies the timing design and increases memory speed because all timing is dependent on the number of memory clock cycles.

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NOTE: To function properly, SDRAM DIMMs must meet the Intel 4-clock, 100 MHz, unbuffered SDRAM specification for either 64-bit or 72-bit SDRAM.

System memory configuration

| SDRAM | SDRAM | SDRAM | |
|--------|--------|--------|---------------------|
| Bank 0 | Bank 1 | Bank 2 | Total System Memory |
| Empty | Empty | 16 MB | 16 MB |
| Empty | Empty | 32 MB | 32 MB |
| Empty | Empty | 64 MB | 64 MB |
| Empty | Empty | 128 MB | 128 MB |
| Empty | 16 MB | Empty | 16 MB |
| Empty | 16 MB | 16 MB | 32 MB |
| Empty | 16 MB | 32 MB | 48 MB |
| Empty | 16 MB | 64 MB | 80 MB |
| Empty | 16 MB | 128 MB | 144 MB |
| Empty | 32 MB | Empty | 32 MB |
| Empty | 32 MB | 16 MB | 48 MB |
| Empty | 32 MB | 32 MB | 64 MB |
| Empty | 32 MB | 64 MB | 96 MB |
| Empty | 32 MB | 128 MB | 160 MB |
| Empty | 64 MB | Empty | 64 MB |
| Empty | 64 MB | 16 MB | 80 MB |
| Empty | 64 MB | 32 MB | 96 MB |
| Empty | 64 MB | 64 MB | 128 MB |
| Empty | 64 MB | 128 MB | 192 MB |
| Empty | 128 MB | Empty | 128 MB |
| Empty | 128 MB | 16 MB | 144 MB |
| Empty | 128 MB | 32 MB | 160 MB |

| Empty | 128 MB | 64 MB | 192 MB |
|--------|--------|--------|--------------|
| Empty | 128 MB | 128 MB | 256 MB |
| 16 MB | 16 MB | 16 MB | 48 MB |
| 256 MB | 256 MB | 256 MB | 768 MB |
| | | | De aluta tan |

IDE support

The motherboard provides 2 independent high performance bus-mastering PCI IDE interfaces capable of supporting PIO Mode 3, Mode 4, and ATAPI devices (e.g., CD-ROM). The system BIOS supports logical block addressing (LBA) and extended cylinder sector head (ECSH) translation modes. IDE device transfer rate and translation mode are automatically detected by the system BIOS.

Usually programmed I/O operations require a substantial amount of processor bandwidth. However, in multitasking operating systems, the bandwidth freed by bus mastering IDE can be devoted to other tasks while disk transfers are occurring.

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Universal Serial Bus (USB) support

The motherboard features 4USB ports that permit the direct connection of 4 USB peripherals, one to each port. The motherboard fully supports the universal host controller interface (UHCI) and uses software drivers that are UHCI-compatible.

Features of USB include:

- Self-identifying peripherals that can be hot-plugged
- Automatic mapping of function to driver and configuration
- Support for isochronous and asynchronous transfer types over the same set of wires
- Support for up to 127 physical devices
- Guaranteed bandwidth and low latencies appropriate for telephony, audio, and other applications
- Error-handling and fault-recovery mechanisms built into the protocol

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Primary power supply connector

| Pin | Signal Name | Pin | Signal Name |
|-----|--------------------|-----|-------------|
| 1 | +3.3 V | 11 | +3.3 V |
| 2 | +3.3 V | 12 | -12 V |
| 3 | Ground | 13 | Ground |
| 4 | +5 V | 14 | PW_ON |
| 5 | Ground | 15 | Ground |
| 6 | +5 V | 16 | Ground |
| 7 | Ground | 17 | Ground |
| 8 | PWRGD (Power Good) | 18 | -5 V |

| 9 | +5 VSB (Standby for real-time clock) | 19 | +5 V |
|----|---|----|---------|
| 10 | +12 V | 20 | +5 V |
| | | | D 1 1 1 |

Power supply fan connector

| | Pin | Signal Name |
|---|-----|-----------------|
| 1 | | Rotation |
| 2 | | +12 V (Suspend) |
| 3 | | Ground |
| | | Back to top |

CPU fan connector

| Pin | Signal Name |
|-----|-------------|
| 1 | Rotation |
| 2 | +12 V |
| 3 | Ground |
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Front panel connector

The front panel connector includes headers for the following connections; Power LED, Speaker, Reset switch, Power switch., Sleep switch.

Figure 2: Front Panel Connector



- 1 Message LED
- 2 Keyboard Lock
- 3 SMI Lead
- 4 Speaker Connector

- 5 Reset SW
- 6 Power LED
- 7 IDE LED
- 8 ATX Power Switch

PS/2 keyboard and mouse ports

| Pin | Signal Name |
|-----|----------------|
| 1 | Data |
| 2 | No Connect |
| 3 | Ground |
| 4 | +5 Vcc (fused) |
| 5 | Clock |
| 6 | No Connect |

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USB connectors

| Pin | Signal Name |
|-----|-----------------|
| 1 | Power |
| 2 | USBP0# (USBP1#) |
| 3 | USBPO (USBP1) |
| 4 | Ground |
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Serial port connector

| Pin | Signal Name |
|-----|---------------------------|
| 1 | Data Carrier Detect (DCD) |
| 2 | Receive Data (RXD) |
| 3 | Transmit Data (TXD) |
| 4 | Data Terminal Ready (DTR) |
| 5 | Ground |
| 6 | Data Set Ready (DSR) |
| 7 | Request to Send (RTS) |
| 8 | Clear to Send (CTS) |
| 9 | Ring indicator |

Parallel port

| Signal Name | Pin | Pin | Signal Name |
|-------------|-----|-----|-------------|
| STROBE- | 1 | 14 | AUTO FEED |
| Data Bit 0 | 2 | 15 | ERROR* |
| Data Bit 1 | 3 | 16 | INIT* |
| Data Bit 2 | 4 | 17 | SELECT IN* |
| Data Bit 3 | 5 | 18 | Ground |
| Data Bit 4 | 6 | 19 | Ground |
| Data Bit 5 | 7 | 20 | Ground |
| Data Bit 6 | 8 | 21 | Ground |
| Data Bit 7 | 9 | 22 | Ground |
| ACK* | 10 | 23 | Ground |
| BUSY | 11 | 24 | Ground |
| Error | 12 | 25 | Ground |
| SELECT | 13 | | |
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IDE connectors

| Signal Name | Pin | Pin | Signal Name |
|----------------|-----|-----|--------------|
| Reset IDE | 1 | 2 | Ground |
| Host Data 7 | 3 | 4 | Host Data 8 |
| Host Data 6 | 5 | 6 | Host Data 9 |
| Host Data 5 | 7 | 8 | Host Data 10 |
| Host Data 4 | 9 | 10 | Host Data 11 |
| Host Data 3 | 11 | 12 | Host Data 12 |
| Host Data 2 | 13 | 14 | Host Data 13 |
| Host Data 1 | 15 | 16 | Host Data 14 |
| Host Data 0 | 17 | 18 | Host Data 15 |
| Ground | 19 | 20 | Кеу |
| DDRQ0(DDRQ1) | 21 | 22 | Ground |
| I/O Write | 23 | 24 | Ground |
| I/O Read | 25 | 26 | Ground |
| IORDY | 27 | 28 | Vcc pull-up |
| DDACKO(DDACK1) | 29 | 30 | Ground |
| IRQ14(IRQ15) | 31 | 32 | Reserved |
| Addr 1 | 33 | 34 | Reserved |
| Addr O | 35 | 32 | Addr 2 |

| Chip Select 1P(1S) | 37 | 38 | Chip Select 3P (3S) |
|--------------------|----|----|---------------------|
| Activity | 39 | 40 | Ground |

Floppy connector

| Signal Name | Pin | Pin | Signal Name |
|-------------|-----|-----|-----------------|
| Ground | 1 | 2 | DENSEL |
| Ground | 3 | 4 | Reserved |
| Key | 5 | 6 | FDEDIN |
| Ground | 7 | 8 | Index |
| Ground | 9 | 10 | Motor Enable A |
| Ground | 11 | 12 | Drive Select B |
| Ground | 13 | 14 | Drive Select A |
| Ground | 15 | 16 | Motor Enable B |
| MSEN1 | 17 | 18 | DIR |
| Ground | 19 | 20 | STEP |
| Ground | 21 | 22 | Write Data |
| Ground | 23 | 24 | Write Enable |
| Ground | 25 | 26 | Track 00 |
| MSENO | 27 | 28 | Write Protect |
| Ground | 29 | 30 | Read Data |
| Ground | 31 | 32 | Side 1 Select |
| Ground | 33 | 34 | Diskette Change |
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