54CPI

Pentium ISA/PCI System Board

USER'S MANUAL

Revision 2.00

Quick Reference Section

Warning !!!

Cooling fan and heat sink must be placed
on the Pentium CPU at all times.
Manufacturers of motherboard and CPU
are not responsible for any damages
due to the absence of cooling fan and heat sink.

QUICK INTRODUCTION

CPU installation

The 54CPI supports Intel Pentium 75/90/100/120/133/150/167 MHz Microprocessors. Carefully install the Pentium processor into the ZIF socket at location U25. Make sure pin one of the CPU corresponds to pin 1 of the socket.

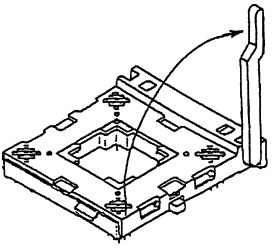
Power supply

The 54CPI system board has a built-in voltage regulator to convert the typical 5.0 Volt output from the regular PC/AT compatible power supply to 3.3 Volts required for the Pentium processor. You do not need to have a special power supply with 3.3 Volts output for the board.

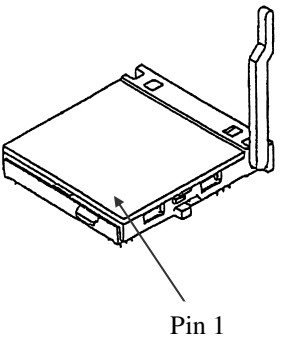
CPU INSTALLATION INSTRUCTIONS

54CPI uses a Single Lever ZIF (Zero Insertion Force) PGA (Pin Grid Array) socket for your CPU. To install your CPU, follow the steps below:

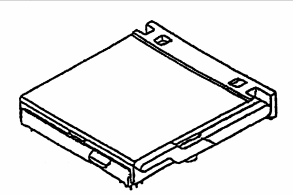
1. Rotate the actuator arm 90 degrees to its fully up right position.



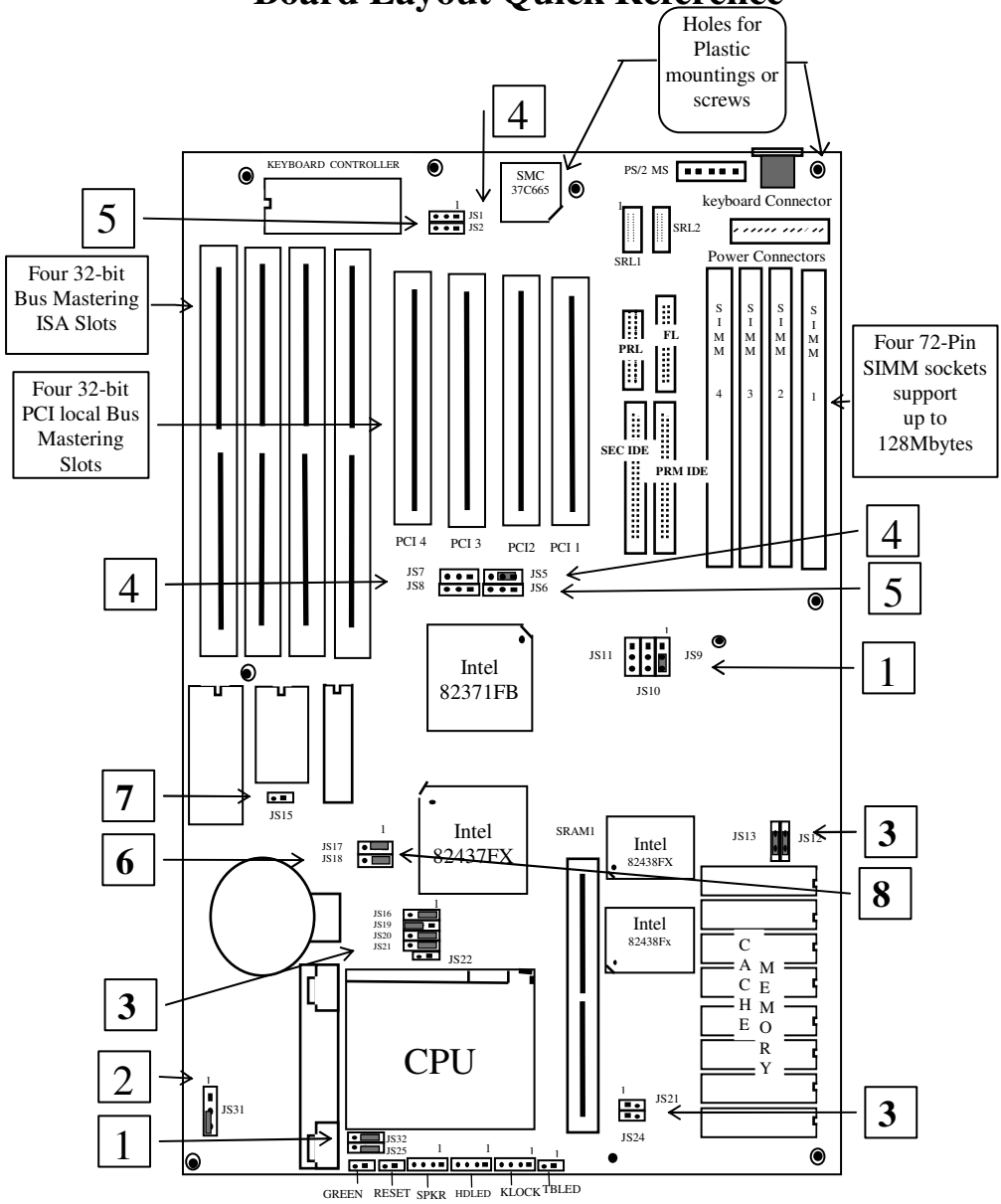
2. To insert the CPU, make sure the notched corner of the CPU is placed adjacent to the Pin one on the socket. The pins of CPU must be aligned with the holes of the sockets. **No force should be required to insert the CPU into the socket.**



3. Rotate the actuator to a horizontal position, making sure it locks under the detent.
   The CPU is now installed!
   To remove the CPU, simply reverse the same procedure as shown and gently lift the CPU out of the socket.



Board Layout Quick Reference



Note: *The sample jumper setting shown above is set at Pentium-90MHz, 256K cache size.*

JUMPER SETTING QUICK REFERENCE:

1) CPU clock Frequency Selection Jumpers

CPU speed	JS9	JS10	JS11	JS25	JS32
75 MHz	1-2	2-3	1-2	1-2	1-2
90 MHz (Default)	***1-2***	***1-2***	***2-3***	***1-2***	***1-2***
100 MHz	2-3	2-3	2-3	1-2	1-2
120 MHz	1-2	1-2	2-3	1-2	2-3
133MHz	2-3	2-3	2-3	1-2	2-3
150MHz	1-2	1-2	2-3	2-3	2-3
167MHz	2-3	2-3	2-3	2-3	2-3

2) CPU Voltage Type Jumpers

CPU Voltage	JS31
Standard(STD) or VR	***2-3***
VRE	1-2

3) Jumper Settings for Cache Size and SRAM Location

CACHE	JS16	JS19	JS20	JS21	TAG RAM SR1	DATA RAM SR2 TO SR9	MODULE SRAM1
256K/ASYNC	***1-2***	***2-3***	***1-2***	***1-2***	***32KX8***	***32KX8***	***EMPTY***
512K/ASYNC	2-3	1-2	1-2	2-3	32KX8	64KX8	EMPTY
MODULE	2-3	2-3	2-3	2-3	EMPTY	EMPTY	MODULE

SRAM Type

SRAM Type	JS12, JS13	JS23,JS24
Mixed Mode	***SHORT***	***OPEN***
Pure 3.3volt	OPEN	SHORT

4) Parallel Port Interrupt Select

Interrupt	JS5
Interrupt7	***1-2***
Interrupt 5	2-3

ECP DMA Channel Setting

ECP Mode	JS1	JS7	JS8
Normal Mode	***Open***	***Open***	***Open***
DMA 3 Selected	SHORT	1-2	1-2
DMA 1 Selected	SHORT	2-3	2-3

5) Enhanced Floppy

Floppy Mode	JS2	JS6
Normal	***Open***	***Open***
Enhanced	Short	2-3

6) CMOS Clear Jumper

CMOS	JS18
Normal CMOS Operation	***1-2***
Clear CMOS Data	2-3

7) Display Type Jumper

Display Type	JS15
Monochrome, EGA, VGA	***OPEN***
CGA	SHORT

8) Flash BIOS Programming

Flash BIOS	JS17
+12V Programming	***1-2***
+5V Programming	2-3

CPU Pipeline Mode

Pipeline Mode	JS22
Disable Pipeline Mode	***Open***
Enable Pipeline Mode	Closed

Note: If using a Pipeline or Pipeline Burst Cache module, jumper JS22 must be in the Closed position.

NOTE: Refer to chapter 2 “System Board Jumpers” Section for more detailed information.

CMOS SETUP QUICK REFERENCE

For Quick Setup (recommended)

1. Go to STANDARD CMOS SETUP to set Date, Time, Hard drive type, and Floppy drives type.
2. From main menu, use the TAB key or mouse to go to the DEFAULT SETUP menu. Select ***Optimal*** icon. Select Yes to load the Optimal values.

For manual setup (For advanced user who has high technical understanding)

3. Select ADVANCED CMOS SETUP, ADVANCED CHIPSET SETUP, and POWER MGMT SETUP menus to set each option individually.

I. STANDARD SETUP:

Date/Time	:Current date/time
Primary Master Type	:Not Installed
Primary Slave Type	:Not Installed
Floppy Drive A	:Not Installed
Floppy Drive B	:Not Installed
Base Memory Size (KB)	:640
Ext. Memory Size (KB)	:Size of Ext. Memory installed

II. ADVANCED CMOS SETUP

Option Name	OPTIMAL	FAIL-SAFE
System Keyboard	**Present**	**Present**
Primary Display	**VGA/EGA**	**VGA/EGA**
PS/2 Mouse Support	**Enabled**	**Disabled**
Above 1 MB Memory Test	**Disabled**	**Disabled**
System BootUp NumLock	**On**	**On**
Floppy Drive Seek At Boot	**Disabled**	**Disabled**
Floppy Drive Swapping	**Disabled**	**Disabled**
System Boot Up Sequence	**C: , A:**	**A: , C:**
Password Checking	**Setup**	**Setup**
Cache Memory	**Both**	**Internal**
System BIOS Shadow Cacheable	**Disabled**	**Disabled**
Video ROM C000, 32K	**Shadow**	**Disabled**
Adapter ROM C800, 16K	**Disabled**	**Disabled**
Adapter ROM CC00, 16K	**Disabled**	**Disabled**
Adapter ROM D000, 16K	**Disabled**	**Disabled**
Adapter ROM D400, 16K	**Disabled**	**Disabled**
Adapter ROM D800, 16K	**Disabled**	**Disabled**
Adapter ROM DC00, 16K	**Disabled**	**Disabled**
IDE Block Mode	**Auto**	**Disabled**
Onboard PCI IDE	**Both**	**Disabled**
Onboard PCI IDE Prim. PIO Mode	**Auto**	**Mode 0**
Onboard PCI IDE Sec. PIO Mode	**Auto**	**Mode 0**
Onboard PCI IDE 32 bit Mode	**Enabled**	**Disabled**
Primary Master LBA Mode	**Disabled**	**Disabled**
Primary Slave LBA Mode	**Disabled**	**Disabled**

Secondary Master LBA Mode	**Disabled**	**Disabled**
Secondary Slave LBA Mode	**Disabled**	**Disabled**
Secondary Ctrl Drives Present	**None**	**None**

III. ADVANCED CHIPSET SETUP

Memory Hole	**Disabled**	**Disabled**
DRAM Speed	**70 ns**	**70ns**
IRQ 12/M Mouse Functiion	**Enabled**	**Disabled**
8 bit I/O Recovery Time	**1 Sysclk**	**1 Sysclk**
16 bit I/O Recovery Time	**1 Sysclk**	**1 Sysclk**
PCI Burst Mode	**Enabled**	**Disabled**
PCI VGA Palette Snooping	**Disabled**	**Disabled**
PCI IDE Card Selection	**Absent**	**Absent**
PCI Primary IDE INT# LINE	**N/A**	**N/A**
PCI Secondary IDE INT# LINE	**N/A**	**N/A**
IRQ5 Available to	**ISA/EISA**	**ISA/EISA**
IRQ 9 Available to	**PCI / PNP**	**PCI / PNP**
IRQ 10 Available to	**PCI / PNP**	**PCI / PNP**
IRQ 11 Available to	**PCI / PNP**	**PCI / PNP**
IRQ 14 Available to	**PCI / PNP**	**PCI / PNP**
IRQ 15 Available to	**PCI / PNP**	**PCI / PNP**

IV.POWER MANAGEMENT

Advanced Power Management	**Disabled**	**Disabled**
Fall-on to stand by Timeout value	**Disabled**	**Disabled**
Standby to Suspend Timeout Value	**Disabled**	**Disabled**
IDE Drive Power Down in	**Disabled**	**Disabled**
VESA Video Power Down in	**Disabled**	**Disabled**
VESA Power Down Mode	**Standby**	**Standy**
Slow Clock Ratio	**1:1**	**1:1**

V. PERIPHERAL SETUP

Option Name	**OPTIMAL**	**FAIL-SAFE**
Programming Mode	**Auto**	**Manual**
Onboard FDC	**Disabled**	**Disabled**
Onboard IDE	**Disabled**	**Reserved**
Serial Port 1	**3E8H**	**Disabled**
Serial Port 2	**2E8H**	**Disabled**
Parallel Port	**Disabled**	**Disabled**
IRQ Active	**High**	**High**
Parallel Port Mode	**Normal**	**Normal**

MEMORY CONFIGURATION QUICK REFERENCE

The 54CPI's on-board DRAM memory subsystem support 1Mx36, 2Mx36, 4Mx36 and 8Mx36 DRAM Modules. DRAM speed must be 70ns or faster. The table below shows some of the variety of ways to configure the memory.

SIM1 & SIM2	SIM3 & SIM4	TOTAL
1Mx36	None	8 Mbyte
1Mx36	1Mx36	16 Mbyte
1Mx36	4Mx36	40 Mbyte
2Mx36	None	16 Mbyte
2Mx36	2Mx36	32 Mbyte
2Mx36	4Mx36	48 Mbyte
2Mx36	8Mx36	80 Mbyte
4Mx36	none	32 Mbytes
4Mx36	4Mx36	64 Mbyte
8Mx36	None	64 Mbyte
8Mx36	8Mx36	128 Mbyte

Note: 1. You can use 70ns or faster memory for 54CPI. Please see chapter 3, Hardware Installation, for more detailed information.

2. SIMMs must installed by groups of SIM & SIM2 or SIM3 & SIM4.

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54CPI

Pentium ISA/PCI System Board

USER'S MANUAL

Revision 2.00

PREFACE

Thank you for purchasing the 54CPI system board. This document will aid you to properly configure and install this system board into your computer system. The document is prepared with best of our knowledge; however, we make no representation or warranty concerning the contents or use of this manual, and specifically disclaim any expressly implied warranties or merchant ability or fitness of any particular purpose. The information in this document is subject to change without notice.

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- Microsoft is a registered trademark of Microsoft Corporation.
- PCI is a registered trademark of PCI Special Interest Group.
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Technical References

- Pentium[tm] Microprocessor Family User's Manual.
- Intel PCIset 82437FX (TSC) Cache/Memory Subsystem.
  Intel PCIset 82438FX (TDP) Data Buffer
  Intel PCIset 82371FB (PIIX) ISA/IDE Controller
- The Peripheral Component Interconnect (PCI) Specification

TABLE OF CONTENTS

CHAPTER 1: INTRODUCTION

PRODUCT OVERVIEW

The 54CPI system board is a powerful combination of performance, quality, and innovative system board designed to address the needs of today's high performance systems. With Pentium 75/90/100/120/133150/167MHz support, optional 256K/512K external Level 2 fast write-back Cache Memory, and 64-bit Memory BURST Read, the board brings exceptional processing power to the Personal Computer (PC) that could only be achieved by High-end workstations just a few years ago. Incorporating the new emerging industry standard Peripheral Component Interconnect (PCI) Local Bus together with the standard 16-bit Industry Standard Architecture (ISA) bus, the board dramatically boosts system I/O throughput for even the most demanding applications in today's market.

Features

CPU Support

- 320-pin ZIF socket for P54C & P54CT(Intel Pentium 75/90/100/120/133/150/167MHz) with built-in 16KB of fast Cache Memory.

Cache Memory

- Supports 256K and 512K High speed External Write-back 3.3V or mixed mode low power consumption Cache RAM.

System Memory DRAM

- 2 Banks of Memory that support EDO or Fast Page Mode 72 pins SIMMs, with a capacity of 4MB, 8MB, 16MB, and 32MB per SIMM, Both x32 and x36 bits SIMM types can be used.

  70ns or faster; 64-bits Interleaved. (Minimum 2 pieces of

  DRAM modules must be installed.)

- Up to 128MBytes on-board memory.

System BIOS

- 1 Megabit of AMI BIOS with Built-in Window standard CMOS, Advanced CMOS, Advanced Chipset, Configuration Utilities, Password, Power Management Setup Menus.

System Chipset

- Intel Triton, Pentium-to-PCI/ISA Chipset. Provides excellent PCI/ISA compatibility.

PCI/ISA Bus

- Four 32-bit Bus Master PCI bus slots.
- Four ISA slots.

Real Time Clock:

- Real Time Clock with built-in Battery or external Lithium Battery provides very accurate timer clock.

Board Form Factor

- Baby AT, 8.7 inches by 12.0 inches.

Product Specifications

Electrical

Power (System board only):	26 Watts @ 5VDC
	0.06 Watts @ ± 12VDC

Environmental

Operating temperature (ambient):	O^0C to 55^0C
Non-Operating temperature:	-42^0C to 70^0C
Relative Humidity:	90% RH @ 36^0C
MTBF	120,000 Hours
Airflow Requirement:	100LFM with on-board fan.

Dimensions

Width:	8.700 inches (221.98 mm)
Length:	12.000 inches (330.20 mm)

TECHNICAL OVERVIEW

Pentium[tm] Microprocessor

The 54CPI supports P54C and P54CT(75/90/100/120/133/150/167 MHz). The microprocessor incorporates the following features:

- 16KB Internal Cache Memory in a 2-way 32-Byte Line Size. The Cache Memory is separated into two 8KB each for Data and Code for performance improvement.
- 32-bit Address and 64-bit Data interfaces
- 4 Gigabytes (Giga = 1,073,741,824) of physical address space
- 64 Terabytes (Tera = 2 to the power of 40) of virtual address space
- Binary Compatible with Large Software Base such as DOS, OS/2, UNIX, Windows,Window NT, Netware, etc.,
- Advanced Design Features such as Branch Prediction, Virtual Mode Extensions
- Built-in 80387 Compatible high performance Floating-point Instruction Execution Unit.

Cache Memory

The increase in speeds of DRAM over the last few years has not kept pace with the increase in microprocessor speeds. This requires very fast and unavailable DRAMs or the addition of wait states into the CPU memory cycles. System performance decreases as the number of wait states increases.

Cache memory is small but can be accessed very fast. The code and data frequently accessed by the CPU normally is stored here. The Pentium Microprocessor has a built-in 16KB cache that is separated into two 8KB segments of Code and Data

Cache. When the Pentium processor accesses memory, it checks if data is in the cache memory and, if the data is there, it will get from there instead of going to much slower main system memory. This is a cache hit situation. It is possible that 95 to 99 memory accesses out of 100 memory accesses are cache hits depending on the application software.

An optional 256KB to 512KB external write-back OR write-through cache memory is provided on the 54CPI system board to achieve an even higher performance. This external cache requires eight pieces of 32Kx8, 64Kx8 fast SRAM chips, or a cache module. With external cache memory, the memory hit rate of the system will be further improved so that the overall performance is higher. Please see Appendix C section for system memory mapping with cached and non-cached locations.

Main System Memory (DRAM)

The main memory subsystem of the 54CPI consists of 640KB of DRAM memory below 1 Megabyte address space, 256KB of I/O ROM BIOS, 128KB of system BIOS ROM, and up to 127MB (128MB - 1MB of Base and reserve mem) of extended system memory.

System ROM

The BIOS ROM is provided in a single 8-bit EPROM, which can hold up to 128KB of code and data. It is accessible at the top of the system's 4 GB memory address space and at the top of the first Megabyte of memory. The BIOS ROM supports all PCI/ISA compatible features. In addition, a Shadow RAM feature is provided to allow the BIOS code and VIDEO BIOS to be executed from 64-bit system DRAM resident at the same physical address..

The processor is reset when power is turned on or when the RESET switch is used. After RESET, the Pentium CPU is initialized to a known internal state and begins fetching instructions, out of the BIOS ROM, from the reset address FFFFFFF0. This address leads to the entry point of the power-on system initialization procedure stored in BIOS ROM. The

BIOS system initialization procedure consists of the following functions:

- Power-on self-tests such as BIOS Check Sum Test, system DRAM Test, Battery- Backed CMOS RAM Test.
- Initializing all the standard compatible I/O components such as Interrupt Controllers, DMA Controllers (Intel 8237A register compatible), Keyboard Controller (Intel 8742 register compatible), Video Controller (CGA, EGA, VGA, etc..), System Timers (Intel 8254 register compatible).
- Initializing all the PCI/ISA add-on cards based on the information stored in the CMOS.
- Built-in SETUP program, if allowed, is used for system configuration such as:
  - . Day/Time setting
  - . Selection for floppy disk and hard disk types
  - . Shadow RAM, Cache Memory Enable, Disable options.
  - . Auto Detect IDE Hard Drives
  - . Virus Protection and Password for Security

Besides initializing the system, the BIOS ROM also provides BIOS interrupt calls for such functions as video access, floppy disk access, printer access, etc..

DRAM control Logic

The DRAM control logic on the 54CPI system board is designed and optimized for the Pentium CPU. Unlike most other systems with a separate cache controller, the DRAM control logic is tightly coupled with the on-chip cache controller. When CPU address becomes available for a new memory cycle, both controllers operate in parallel. If the cycle is a read hit or a write hit, the cache controller will take control of the cycle while the DRAM controller stays in idle. If the cycle is a read 'miss', the DRAM controller will cooperate with the cache controller to generate appropriate cycles to write the data from the cache memory back to the system memory, if the cache data line is

dirty, then data is read from the system memory to the CPU and updated in the cache memory. If the cycle is a write miss, the DRAM controller simply takes control to write the data to the system memory while the cache controller stays in idle. The DRAM controller and the system memory support the Pentium 128Byte-burst memory read cycles and fast-page mode cache write back cycles for the highest performance.

The on-board DRAM is configured in a 72-bit-wide arrangement consisting of 64 bits of data and 8 bits of parity. Each parity bit is directly associated with one of the 8 bytes in the 72-bit double long word. At least two SIMMs are required to have a system running at full 64-bit data path.

Shadow DRAM Feature

The 54CPI supports the Shadow DRAM feature which allows the BIOS ROM, VIDEO ROM, and I/O ROM codes to be executed from the system DRAM resident at the same physical address space. The Shadow DRAM feature significantly improves the system performance in BIOS-call intensive applications because executing code out of 64-bit DRAM is faster than from an 8-bit EPROM.

PCI/ISA Compatible Expansion Bus

The 54CPI system board has 4 32-bit PCI Expansion Bus connectors and 4 16-bit ISA Expansion Bus connectors for interfacing with all PCI and ISA compatible I/O, memory, and bus mastering adapters.

Introduction to PCI Local Bus

PCI is an electrical specification and logic requirement for a local bus standard, i.e. a multiplexed extension of the CPU bus.

PCI defines a standard I/O component level interface that permits all PCI Local Bus products to be totally interchangeable and directly connected without using any glue logic.

What PCI Accomplishes

PCI is a way to physically interconnect highly integrated peripheral components and processor/memory systems.

PCI Features

- Up to 4 PCI loads can be used in the same system on the PCI expansion slots, not including the PCI Controller and an expansion bus controller for ISA, or MCA. PCI de-couples the CPU from the expansion bus and works at 33 MHz but can use either a 32-bit or 64-bit data path to the CPU.
- Has multiplexed address, command, and data bus and supports burst mode operation on reads and writes.
- Runs synchronous with the CPU at speeds up to 33 Mhz, has a maximum data transfer rate of 120 MBs (with a peak rate of 132 MBs on a 32-bit data path).
- Has an optional 64-bit data path that is transparently inter-operable with the 32-bit data path.
- Has low latency random accesses (about 60ns write access latency) to slave registers from a PCI bus master on the PCI bus.
- Is capable of full concurrence with the processor and PCI bus masters.
- Has full multi-master capability, allowing any PCI Master peer-to-peer access to any PCI slave.
- Has hidden and overlapped central arbitration.
- Has a low pin count (master - 47; slave - 45),
- Has address and data parity, and uses three physical address spaces: 32-bit memory, 32-bit I/0, and a 256 byte-per-agent configuration space.
- The PCI Controller buffers reads and writes between the memory/CPU and PCI peripheral devices.

- The CPU in a PCI system runs concurrently with PCI bus mastering peripherals. Although bus mastering peripheral devices are arbitrated, significant data transfer rate improvements can be achieved without splitting resource utilization between the CPU and a bus mastering device. Peripheral devices can operate at up to 33 MHz in a PCI environment.
- PCI devices can be bus masters, slaves, or a combination of bus master and slave.
- The PCI specification also provides for burst cycles of any length for both reads and writes.
- PCI is a multiplexed bus. Multiplexing allows more than one signal to be sent on the same electrical path. The control mechanisms have been modified and extended to optimize I/0 support.

ISA BUS

The Industry Standard Architecture(ISA) is 16-bit data transfer, addressing capabilities to the AT Bus Architecture.

ISA Features

- 16-bit addressing and data transfers
- Data transfer rates up to 8MB/s.

Setup information writes to system board battery backed CMOS RAM and to special I/O ports.

ISA Compatible Peripherals

The 54CPI system board provides the following standard peripherals:

- Enhanced DMA functions with seven independently programmable channels.

- Two 82C59A compatible Interrupt Controllers.
- Four 82C54 compatible programmable interval timers.
- One keyboard controller.
- Real time Clock controller with 114Bytes of CMOS SRAM

CHAPTER 2: BOARD'S JUMPERS & CONNECTORS

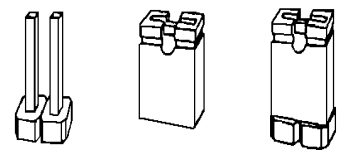
When working with the 54CPI, it is extremely important that you avoid Electrical Static Discharge (ESD). Always ground yourself by wearing a grounded wristband or ankle strap.

Figure 1 on the next page shows the component layout of the 54CPI system board with locations of the system board jumpers and connectors. Note that most jumpers and connectors on the system board are labeled with proper names with pin 1 marked as '**1**'. To avoid damaging the board and to have proper operation, caution should be taken when connecting these jumpers and connectors.

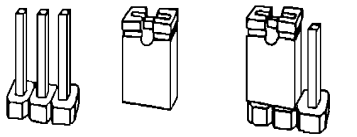
JUMPER DESCRIPTIONS

Jumpers are used to select between various operating modes. A jumper switch consists of two, three, or four gold pins projecting from the system board. Placing the plastic jumper cap over two pins connects those pins and makes a particular selection. Using the jumper cap to cover two pins in this way is referred to as shorting those pins. If the cap is not placed on any pins at all or placed on only one pin, this is referred to as leaving the pins open.

Note: When you open a jumper, leave the plastic jumper cap attached to one of the pins so you don't lose it.

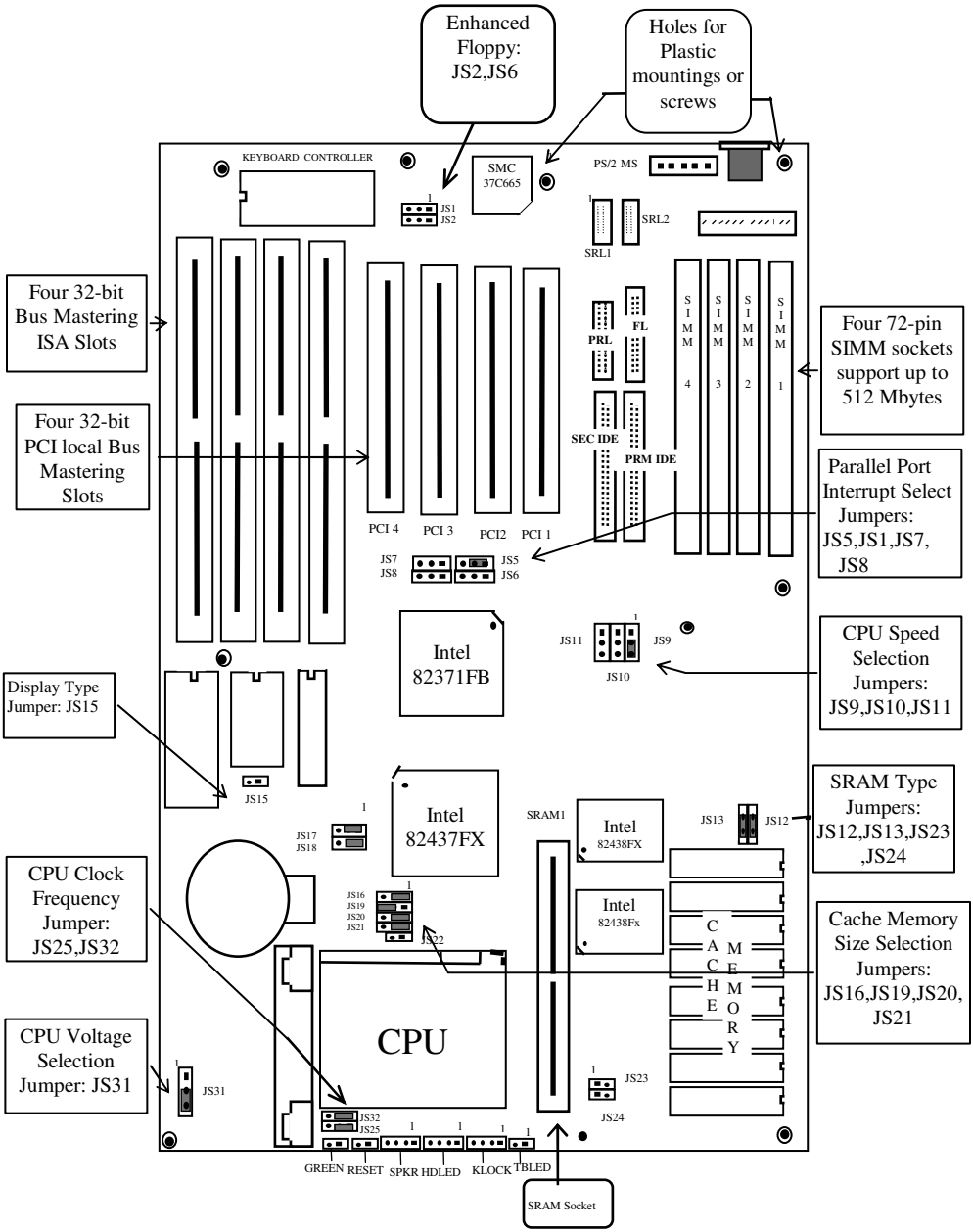


2-pin jumper



3-pin jumper

Figure 1: 54CPI Component Layout



Remark: *The sample jumper setting shown above is set at Pentium-90MHz, 256K cache size.*

CPU Jumpers

CPU Clock Frequency Jumpers

The 54CPI supports 75 / 90 / 100 / 120/133MHz Pentiums. The jumpers should be set to the corresponding CPU speeds.

CPU speed	JS9	JS10	JS11	JS25	JS32
75 MHz	1-2	2-3	1-2	1-2	1-2
90 MHz (Default)	**1-2**	**1-2**	**2-3**	**1-2**	**1-2**
100 MHz	2-3	2-3	2-3	1-2	1-2
120 MHz	1-2	1-2	2-3	1-2	2-3
133MHz	2-3	2-3	2-3	1-2	2-3

CPU Voltage Type

CPU Voltage	JS31
Standard (STD) or VR	2-3
VRE	1-2

Cache Memory Jumpers

Cache Memory Size Jumpers

Two cache memory sizes are supported. The jumper is set according to the size of Cache Memory. All the SRAM chips have speeds of 15ns or faster.

CACHE	JS16	JS19	JS20	JS21	TAG RAM SR1	DATA RAM SR2 TO SR9	MODULE SRAM1
256K/ ASYNC	***1-2***	***2-3***	***1-2***	***1-2***	***32KX8***	***32KX8***	***EMPTY***
512K/ ASYNC	2-3	1-2	1-2	2-3	32KX8	64KX8	EMPTY
MODULE	2-3	2-3	2-3	2-3	EMPTY	EMPTY	MODULE

System Board Standard Jumpers

CMOS Discharge Jumper

The jumper JS18 is used to clear all information, including password, currently stored in the CMOS RAM. (12887A or 12885 on 54CPI board at location U18). It is typically used when you forget the password that you selected previously and you cannot get into the CMOS setup menu.

Function	JS18
Normal Operation (Default)	***1-2***
Clear CMOS Data	2-3

Monitor Type Select Jumper

This is PC/AT compatible jumper to inform the system BIOS that the graphic card installed is CGA or other types. Thus, the jumper should be set according to the type of graphic card installed in the system.

Display Type	JS15
VGA, EGA, or Monochrome (Default)	***OPEN***
CGA	SHORT

Peripheral Jumpers

Enhanced Floppy

Floppy Mode	JS2	JS6
Normal	OPEN	OPEN
Enhanced	Short	2-3

Parallel Port Interrupt Select Jumper

Interrupt for Parallel Port can be optionally set to IRQ7 or IRQ5 by this jumper.

Parallel Port Interrupt	JS5
IRQ7 for Parallel port. (Default)	***1-2***
IRQ5 for Parallel port.	2-3

Extended Capabilities Port (ECP) Jumpers

The onboard Parallel Port Controller supports PC/AT Compatible Mode (Normal mode), High Speed HP and Microsoft Compatible Extended Capabilities Port mode (ECP). In Normal mode, system CPU will handle data transfer from the FIFO buffers of the Parallel Port Controller to system memory. In ECP mode, to improve data transfer rate, system DMA will be used to handle the data transfer. (For more information about ECP mode, please refer to Extended Capabilities Port Protocol and ISA Interface Standard specification that is available from Microsoft Corporation)

ECP Mode	JS1	JS7	JS8
Disable ECP Mode for Parallel Port (Default)	***Open***	***Open***	***Open***
Enable ECP Mode with DMA Channel 3	Short	1-2	1-2
Enable ECP Mode with DMA Channel 1	Short	2-3	2-3

Manufacturer Reserved Jumpers

The jumper settings shown below are factory installed. Manufacturer has reserved these jumpers. No modification is needed.

SRAM Type

SRAM Type	JS12, JS13	JS23, JS24
Mixed Mode	SHORT	OPEN
Pure 3.3-Volt	OPEN	SHORT

SRAM Socket

This Socket can be used for Sync SRAM or Async SRAM modules.

Flash BIOS Programming

Flash BIOS	JS17
+12V Programming	1-2
+5V Programming	2-3

CPU Pipeline Mode

Pipeline Mode	JS22
Disable Pipeline Mode	Open
Enable Pipeline Mode	Closed

CONNECTOR DESCRIPTIONS

Following is the list of 54CPI system board connectors required to be installed for proper system operation. For detailed descriptions of these components, please refer to the next section. To avoid damaging the board and to have proper operation, caution should be taken when connecting these components.

- Power supply connectors (PS8 and PS9)
- Keyboard connector (KBCN)

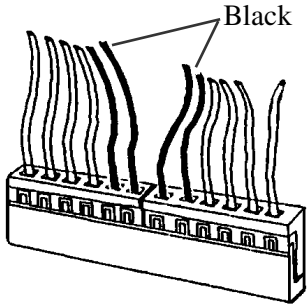
- Reset connector (RESET)
- Power LED and keyboard lock connector (KEYLOCK)
- Speaker connector (SPKR)
- Turbo LED connector (TBLED)
- Hard Disk Activity LED connector (HDLED)

- Parallel Port connector (LPT1)
- Serial Port 1 & 2 connectors (SRL1, SRL2)
- Floppy Interface connector (FDC1)
- IDE Interface connectors (IDE1, IDE2)

Power Supply Connectors (PS8 and PS9)

The two Power Supply connectors (PS8 and PS9) are 6-pin AT standard power connectors. Most power supplies have two six-wire connectors, two of the wires on each connector are black. Align the two six-wire connectors so that the two black wires on each connector are in the middle as shown below.

Pin	Connector PS8	Connector PS9
1	Power Good	Ground
2	+5 VDC	Ground
3	+12 VDC	-5 VDC
4	-12 VDC	+5 VDC
5	Ground	+5 VDC
6	Ground	+5 VDC



Keyboard Connector

The keyboard connector (KBCN) is a 5-pin, circular-type DIN socket. It is used to connect the system board keyboard interface to any standard AT-compatible keyboard. (84 or 101 -key type keyboards). The pin assignments are listed below:

Pin	Description
1	Keyboard Clock Signal
2	Keyboard Data Signal
3	Not Used
4	Ground
5	+5V Fused VDC

Reset Connector

The system RESET connector (RESET) is a 2-pin BERG strip. It is used to connect the push button reset switch located on the front panel to the system board. System reset can be done by shorting pin 1 to pin 2 with the same effect as turning the power off and then on again.

Pin	Description
1	Ground
2	Reset Input

Power LED and Keyboard Lock Connector

The Power LED and Keyboard Lock connector (KEYLOCK) is 5-pin keyed BERG strip. It is used to connect +5 VDC power to the power indicator LED at the front panel and connect security keyboard lock to the keyboard controller. This allows you to switch off the keyboard and so provide limited security against casual intruders. The pin assignments are indicated below:

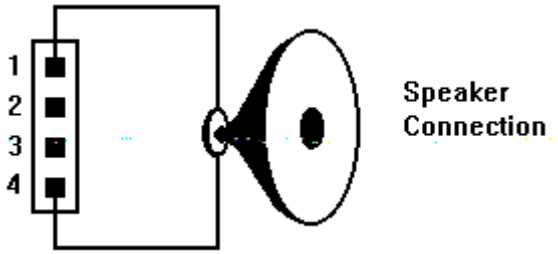
Pin	Description

1	LED Power
2	Key (No Connection)
3	Ground
4	Keyboard Lock
5	Ground

Speaker Connector

The Speaker connector (SPKR) is a 4-pin keyed BERG strip. It is used to connect an external 2-inch, 8-ohm speaker to the system board to provide sound capability. The pin assignments are defined below:

Pin	Description
1	Speaker Data Out
2	Ground
3	Ground
4	+5 VDC



Turbo LED Connector

The Turbo LED connector (TBLED) is a 2-pin BERG strip. It is used to connect a CPU operating frequency indicator LED from the front panel to the system board. The pin assignments are indicated below:

Pin	Description
1	LED Anode
2	LED Cathode

Hard disk Activity LED Connector

The hard disk activity LED connector (HDLED) is a 4-pin keyed BERG strip. It is used to connect to front pannel hard disk LED.

Pin	Description
1	LED Anode (+)
2	LED Cathode (-)
3	LED Cathode (-)
4	LED Anode (+)

Peripheral Connectors

Parallel Port Connector

The on-board parallel port connector (LPT1) is a 2x13-pin male header connector. The On-board Parallel Port can be disabled through the BIOS Setup. Please refer to Chapter 3 "Peripheral Management Setup" section for more detail information. The pin assignment is shown below:

Pin	Description	Pin	Description
1	STROBE	14	AUTO FEED XT
2	Data Bit 0	15	ERROR
3	Data Bit 1	16	INIT
4	Data Bit 2	17	SLCT IN
5	Data Bit 3	18	Ground
6	Data Bit 4	19	Ground
7	Data Bit 5	20	Ground
8	Data Bit 6	21	Ground
9	Data Bit 7	22	Ground
10	ACK	23	Ground

Pin	Description	Pin	Description
11	BUSY	24	Ground
12	PE	25	Ground
13	SLCT	26	No Connection

The Integrated Parallel Port supports Extended Capabilities Port protocol (ECP) to provide a number of advantages for the parallel port as listed below:

- Use DMA channel 1 or 3 to transfer data across the Parallel port in both forward and reverse directions; therefore, processor time is saved for other tasks. This is especially important in multi-tasking operating systems such as Windows NT.

- Peer-to-peer capability for networking.

  Single byte run length encoded (RLE) compression for improved throughput (64:1.)

Serial Port 1 & 2 Connectors

The Serial Port 1 and 2 connectors are the 2x5-pin male headers SRL1 and SRL2. Users should use a flex cable with a 9 or 25 - pin male D-subminiature receptacle at one end and a 2x5-pin female header at the other end to provide RS-232 serial interface. The On-board Serial Ports can be disable through BIOS setup. Please refer to Chapter 3 “Peripheral Management Setup” section for more detail information. The pin assignment is defined below:

Pin	Description	Pin	Description
1	Carrier Detect (CD)	2	Receive Data (RXD)
3	Transmit Data (TXD)	4	Data Terminal Ready (DTR)
5	Signal Ground	6	Data Set Ready (DSR)
7	Request To Send (RTS)	8	Clear To Send (CTS)
9	Ring Indicator (RI)	10	No Connection

Floppy Interface Connector

The On-board Floppy Interface connector (FDC1) is 2x17-pin male headers. This interface supports two 5.25" or 3.5" floppy drives in any combination and also can be disabled if no floppy drives are present on the system. The On-board Floppy Port can be disabled through the BIOS setup. Please refer to Chapter 3 "Peripheral Management Setup" section for more detail information. Pin assignment is as follow:

Pin	Description	Pin	Description
2	RPM	1	Ground
4	No Connection	3	Ground
6	No Connection	5	Ground
8	Index	7	Ground
10	Motor 1	9	Ground
12	Drive 2	11	Ground
14	Drive 1	13	Ground
16	Motor 2	15	Ground
18	Direction	17	Ground
20	Step	19	Ground
22	Write Data	21	Ground
24	Write Enable	23	Ground
26	Track0	25	Ground
28	Write Protect	27	Ground
30	Read Data	29	Mode Detect 2
32	Head Select	31	Ground
34	Disk Change	33	Mode Detect 1

IDE Interface Connectors

The on-board IDE Interface connectors (IDE1 and IDE2) are 2x20-pin male headers. JC5 is the Primary IDE port. JC6 is the Secondary IDE port. Each port supports up to two IDE devices. This interface can be disabled through BIOS setup. Please refer to Chapter 4 "Peripheral Management Setup" section for more detail information. Pin assignment of IDE is as follow:

Pin	Description	Pin	Description
2	Ground	1	IDE Reset/
4	Data 8	3	Data 7
6	Data 9	5	Data 6
8	Data 10	7	Data 5
10	Data 11	9	Data 4
12	Data 12	11	Data 3
14	Data 13	13	Data 2
16	Data 14	15	Data 1
18	Data 15	17	Data 0
20	No Connection	19	Ground
22	Ground	21	DRQ
24	Ground	23	I/O Write/
26	Ground	25	I/O Read/
28	No Connection	27	IORDY DAK
30	Ground	29	No Connection
32	No Connection	31	IDE IRQ 14
34	No Connection	33	Address A1
36	Address A2	35	Address A0
38	IDE Chip Select 1/	37	IDE Chip Select 0/
40	Ground	39	IDE Active/

CHAPTER 3: HARDWARE INSTALLATION

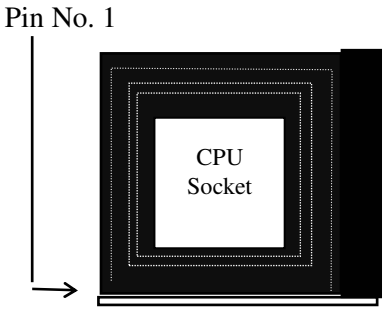
BUILDING A HIGH PERFORMANCE SYSTEM

The dimensions of the 54CPI system board are designed to fit perfectly in a PC/AT standard case. To build a complete high performance system based on the 54CPI system board, the following equipments are needed:

1. A chassis (Case) with dimensions similar to PC/AT standard chassis. The chassis should have a front Panel with connectors for Reset, Power, Keylock, Turbo switch, Turbo LED, Speaker, and Hard drive LED. AC Power cable is included with the chassis. The standard AT 200W power supply should be capable of providing a continuous power within a +4.75 VDC to +5.25 VDC range. A power line filter may be needed for areas with noisy transmission
2. One or two floppy drives (360K/1.2M/1.44M/2.88M).
3. A SCSI Hard disk drive or IDE hard disk drive with a hard drive controller.
4. A Video card (Monochrome, CGA, EGA, VGA). If the Video card is VGA, then it could be PCI interface type for the best display performance.
5. A video display monitor.
6. An AT-compatible keyboard (84 0r 101 Keyboard).
7. The following additional peripherals will be useful to enhance the system:
   - A bus or serial mouse or PS/2 mouse.
   - A tape back up drive.
   - A CD-ROM drive.
8. Cables
   - A set of flat cables for floppy drive & hard disk drive.
9. Tools
   - Set of Screw drivers, Cutter, Pliers

CPU INSTALLATION

Care should be taken when installing the CPU into the Zero Insertion Force (ZIF) socket on the system board. Lift the handle of ZIF socket up. Place the Pentium processor into the ZIF socket. No force should be required to insert the CPU. On Pentium processors pin 1 is with the square base and it goes to particular hole on the socket. Match the hole and pin one first and then easily insert the processor into the socket. Press the handle gently down.



!! Important !!

Cooling fan installation

Mount the cooling kit with fan on top of the CPU. Connect power to fan from power supply. Make sure the cooling kit's bottom surface makes proper contact with top surface of CPU.

!! Warning !!

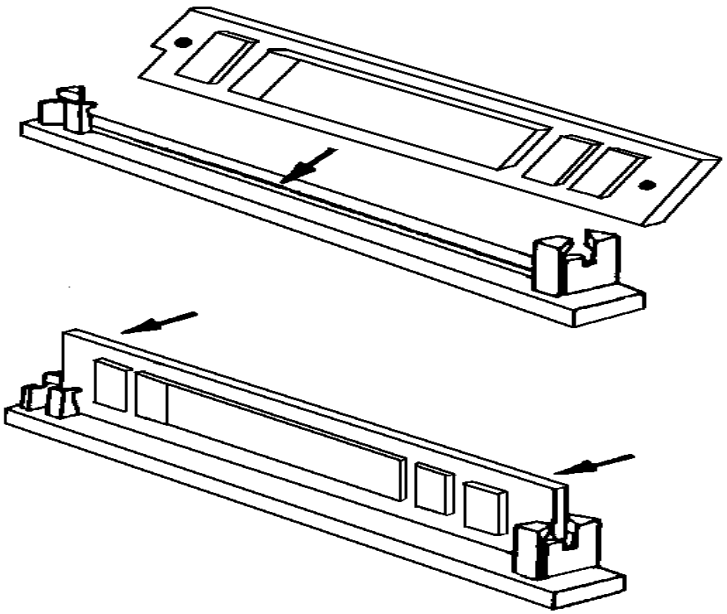
Manufacturer of the board or CPU is not responsible for damage to CPU because of improper handling during installation or cooling kit with fan is not used.

INSTALLING DRAM SIMMS

When working with DRAM SIMMs, it is extremely important that you avoid Electrical Static Discharge (ESD). Always ground yourself by wearing a grounded wristband or ankle strap.

1. Power must be off while installing SIMMs.
2. The SIMM module should face to the right with pin 72 next to the power supply connectors.
3. Insert the SIMM at a 45 degree angle, tilted towards ISA slots.
4. Gently push the SIMM to an upright position until it "snaps" into place.

Repeat above steps until the entire bank is filled.



The on-board DRAM memory sub-system has four module mounting sockets which are divided into "banks" of two sockets each. Sockets labeled SIM1 and SIM2 constitute bank 0. Sockets labeled SIM3 and SIM4 constitute bank 1. They support 1MB, 2MB, 4MB, 8MB, 16MB, and 32MB x32 or x36 DRAM SIMMs. DRAM speed must be 70ns or faster. Both EDO or Fast Page Mode DRAMs are supported.

Each Bank must be populated with the same size of memory. If SIM1 has a 2Mx36 module installed, SIM2 must also have a 2Mx36 module installed.

Memory Configuration

SIM1 & SIM2	SIM3 & SIM4	TOTAL
1Mx36	None	8 Mbyte
1Mx36	1Mx36	16 Mbyte
1Mx36	4Mx36	40 Mbyte
2Mx36	None	16 Mbyte
2Mx36	2Mx36	32 Mbyte
2Mx36	4Mx36	48 Mbyte
2Mx36	8Mx36	80 Mbyte
4Mx36	none	32 Mbytes
4Mx36	4Mx36	64 Mbyte
8Mx36	None	64 Mbyte
8Mx36	8Mx36	128 Mbyte

The 54CPI supports both PCI slots and ISA slots. You can install the corresponding add-on cards into any of these slots. Make sure these add-on cards' interrupts or DMA channels do not conflict with each other. The best way to remember is to write down the information of all the installed cards into the back of this manual for later reference.

. PCI Add-on cards are normally automatically configured by system BIOS during boot up. However, some PCI add-on cards do have jumper settings for INTA or INTB. Write down the information if it is available for later reference.

  ISA add-on cards can be installed in the provided ISA slots. Unless the ISA add-on card is plug-n-play compatible, there is no specific software that can automatically configure the ISA add-on cards, therefore special care should be taken when setting Interrupt and DMA channels of ISA cards.

Please refer to the manuals shipped with the add-on cards for more information. Care should be taken when inserting the cards into the slots to make sure the connector slots are not damaged.

CHAPTER 4: SYSTEM SETUP

SYSTEM CMOS

You need to setup the system CMOS every time:

- You start a new and un-configured system
- You receive a start-up error message indicating the configuration information stored in the non-volatile CMOS RAM has somehow become corrupted.
- You add, remove, or change peripherals from your system.

You add, remove, or change DRAM from your system.

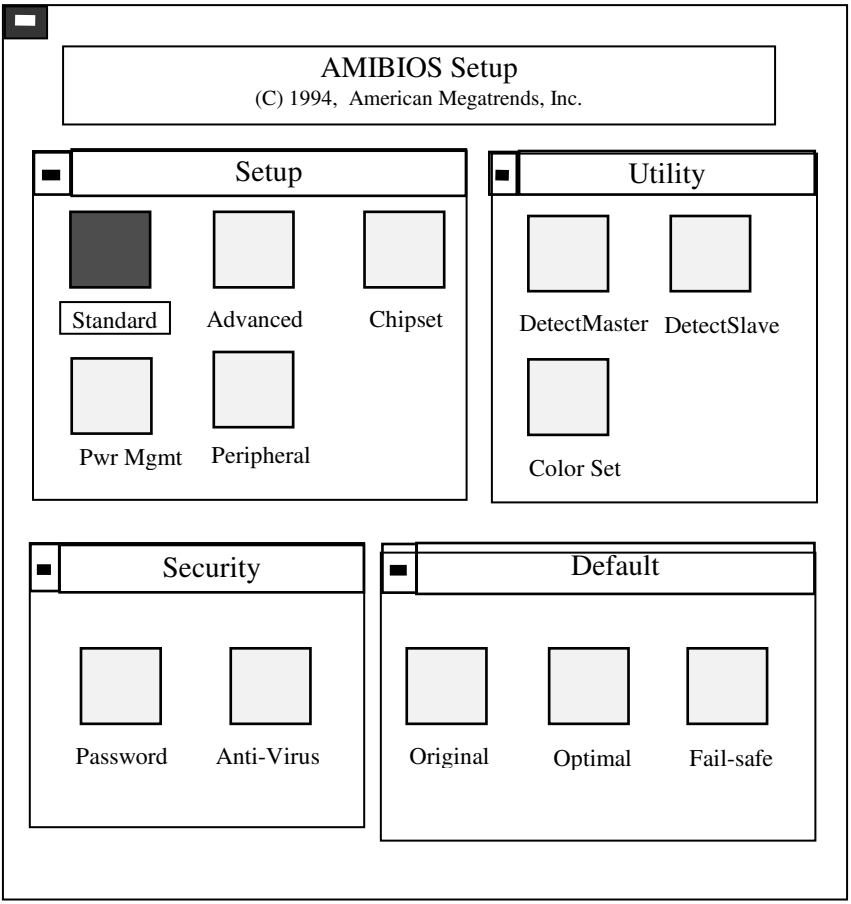
The first time you power up the system, the configuration information stored in the battery-backed CMOS RAM may not be correct. The BIOS detects this condition and prompts the user to go through the SETUP section. This chapter explains how to use the BIOS SETUP program and how to make the appropriate entries.

Some of the parameters are already factory preset and do not need to be changed. Please read the instructions carefully and only change the settings if necessary.

Entering CMOS Setup

The System BIOS provides a Built-in Setup Utility that can be accessed by pressing < Del > key at the appropriate time during system boot up. Setup configuration data is stored in system CMOS RAM.

The Following windows will appear in the AMIBIOS Setup main screen. Details of setup options in each window is given in the following sections.



Setup Window

Types of Setup	Description
Standard Setup	Sets time date, hard disk type, types of floppy drives, display type, and if Keyboard is installed.
Advanced Setup	Above 1 MB Memory Test, Parity Error check, System Boot Up Numlock, System Boot Up Sequence, Cache Memory, Adapter Shadow Cacheable, and many others.
Chipset Setup	Sets chipset-specific options and features.
Power Mgmt	Controls I/0 Controller-related options.

Standard Setup

Standard Setup is selected from the Setup window in the main screen. Standard setup options described in this section are selected by choosing the appropriate high-level icon from the Standard Setup screen. All displayed icons are described in this section, although the screen display is often all you need to understand how to set the option.

Date and Time Configuration

Select the Standard option. Select the Date and Time icon. The current values for each category are displayed. Enter new values through the keyboard.

Master Hard Disk:

Slave Hard Disk:

Select one of these hard disk drive icons to configure the drive named in the option. A scrollable screen that lists all valid disk drive types is displayed. Select the correct type and press < Enter >. Note that a hard drive will not work properly if you enter the incorrect drive parameter. If the hard disk drive is an IDE type, select *DetectMaster or DetectSalve* from the Utility section of the BIOS Setup main menu to automatically detect the IDE drive parameters and report them to this screen.

You can also manually enter the hard disk drive parameters. The drive parameters are:

Parameter	Description
Type	The number for a drive with certain identification parameters.
Cylinders	The number of cylinders in the disk drive.
Heads	The number of heads.

Parameter	Description
Write Precompensation	The size of a sector gets progressively smaller as the track diameter diminishes, yet each sector must still hold 512 bytes. Write precompensation circuitry on the hard disk compensates for the physical difference in sector size by boosting the write current for sectors on inner tracks. This parameter is the track number where write precompensation begins.
Landing Zone	This number is the cylinder location where the heads will normally park when the system is shut down.
Sectors	The number of sectors per track. MFM drives have 17 sectors per track. RLL drives have 26 sectors per track. ESDI drives have 34 sectors per track. SCSI and IDE drives may have even more sectors per track.
Capacity	The formatted capacity of the drive is (Number Of heads) x (Number of cylinders) x (Number of sectors per track) x (512 bytes per sector)

Floppy Drive A:

Floppy Drive B:

Move the cursor to these fields and press <Enter> then select the floppy type. The settings are 360 KB 5.25", 1.2 MB 5.25", 720 KB 3.5", 1.44 MB 3.5", or 2.88 MB 3.5".

Primary Display

Select the type of display monitor and Display controller card. The VGA/EGA, CGA 40x25, CGA 80x25, or Monochrome are supported. 'Absent' option could be used if the system does not have display card installed or for display cards that use TSR files instead of BIOS firmware. The Optimal and Fail-Safe setting are *VGA/EGA*.

Above 1 MB Memory Test

During system boot up, the system BIOS can either perform or not perform a thorough test of the system memory above the standard 1MB area. Since a thorough test takes a long time, disabling this option can speed up the power-on initialization process because the BIOS will only scan and quickly test the extended memory of every 32K locations to determine the on-board memory size. The Optimal and Fail-Safe settings are *Disabled.*

Parity Error Check

This option is to support Non-Parity bit SIMMs and Parity bit SIMMs. Enable this option only if you are sure that the SIMMs installed support parity bit. The Optimal and Fail-Safe setting are *Disabled*.

System Boot Up Num Lock

When the computer boots up, the BIOS can either select Numeric values or Cursor control functions for the numeric keypad of IBM compatible keyboards. Most extended compatible keyboards have separate cursor control keys. Therefore, the default setting should be "On" to select Numeric value function for the numeric keypad.

Floppy Drive Seek At boot

This option allows the system BIOS to look for the floppy diskette in the floppy drives during boot up process. This is often set to disabled for systems which do not have floppy drives. The default setting is *Disabled.*

Floppy Drive Swapping

This option allows the system to swap between two floppy drives, drive A to drive B or vice versa, without physically changing the cable setup. When “Enabled is selected, floppy drive A will become B, and floppy drive B will become A. The Optimal and Fail-Safe settings for this option are *Disabled.*

System Boot Up Sequence

System can either boot up from a floppy drive or from a hard disk drive. Selecting option A:, C: will force the BIOS to look for bootable operating system files from floppy drive A: first, before look for files from drive C:. Reverse this sequence by selecting C:, A:. The default setting is *C:, A:.*

Password Checking

If the "Always" option is chosen at Setup, each time the system is turned on, the prompt request for user password will appear.

If the "Setup" option is chosen at Setup, the Password prompt will not appear when the system is turned on, but will appear if the user attempts to enter the Setup program.

The board is shipped with the Password Checking option disabled. To enable this option, you have to select your password by selecting the Password icon in the Security window of the main menu screen.

If you want to ‘disable the Password Checking option, go to the Security Menu and select the Password icon to change to new password. You will be asked to enter the old password before you can enter the new password. However, do not enter any characters when you are asked to enter new password, simply

press the <Enter> key two times. The message to indicate that Password Checking is disabled will appear.

IDE Block Transfer

This option is for the hard drives that can support multiple sector data transfer providing faster performance. Set this option to Disabled only for debugging purposes, otherwise select Auto and let the system BIOS detect and set the option accordingly. Both Optimal and FailSafe are set to *Auto.*

IDE Primary 32-Bit Transfer

This option is used to support the first IDE controller that can support 32-bit data transfer by moving two consecutive words per cycle for better performance. Select *Enabled* if the controller can support this mode, Otherwise, set it to Disabled. Both Optimal and FailSafe are set to *Disabled.*

IDE Primary LBA Mode

Most earlier IDE hard drives' sizes are less than 528MB because of the limitation from PC/AT standard specification. In order to support IDE hard drive with sizes larger than 528MB, the Logical Block Address (LBA) mapping mode must be used. This option is used to support IDE drives connected to the Primary IDE controller that have a size larger than 528MB. Select Master, Slave, Both, or Disabled accordingly to the size of the drives installed. Master is for the first drive, Slave is for the Second drive, and Both if both drives are larger than 528MB. Both Optimal and FailSafe are set to *Disabled.*

IDE Primary Master PIO Mode

Many new IDE controllers and IDE drives can support faster data transfer mode, mode 0, mode 1, mode 2, mode 3, mode 4, respectively. Select the proper mode for the Master drive that connected to the first IDE controller. If you know specifically the mode it can support, you can enter the value, otherwise set it to Auto. The system BIOS will auto detect and set the mode accordingly. The Optimal and Fail-safe settings are *Auto*.

IDE Primary Slave PIO Mode

This option is the same as the one above, but for the second IDE hard drive that is connected to the first IDE Controller.

Drives on Secondary Controller

This group of options is for drives that are connected to the second IDE controller. The Optimal and Fail-safe settings are *Absent*.

Internal Cache

This option is used to control the internal Cache Memory (16KB inside the Pentium microprocessor). Three options are available: Disabled, Write Back (Wr-Back), and Write Through (Wr-Thru). Write Back will provide the best performance. *Disabled* and Write Through are provided only for debugging purposes. The Optimal setting is *Wr-Back*. The Fail-Safe setting is *Wr-Thru.*

External Cache

This option is to control the External Cache Memory (Outside of the microprocessor, also called Secondary Cache or Level 2 Cache). Three options are available: Disabled, Write Back (Wr-Back), and Write Through (Wr-Thru). Write Back will provide the best performance. *Disabled* and Write Through are provided only for debugging purposes. The default setting should be *Wr-Back*.

F000 Shadow Cacheable

The System BIOS ROM code is located at address space F000-FFFF, and can be cached into the CPUs Internal Cache Memory or to system board's External Memory to enhance the performance of the system. However, some software applications may not operate properly when system BIOS ROM is cached. The Optimal setting is *Enabled*. The FailSafe option is set to *Disabled.*

Video Shadow ROM C000:16K

Video Shadow ROM C400:16K

When this option is set to *Enabled*, the video ROM code, that is normally mapped into memory address space from C0000h - C7FFFh is copied (shadowed) from ROM to the system DRAM for faster execution. This will significantly improve the display performance of the system. The settings are *Absent, No Shadow,* or *Shadow*. The Optimal setting is *Enabled* and the Fail-safe setting is *Disabled*.

Shadow C800,16K
Shadow CC00,16K
Shadow D000,16K
Shadow D400,16K
Shadow D800,16K
.....

Shadow DC00,16K

These options are used to selectively shadow the ROM code on the add-on cards into the corresponding memory address space, in system DRAM for faster execution. However, since some add-on cards may not work properly if their ROM code is shadowed, care should be taken when selecting these options. The default setting is *Disabled*.

Advanced Chipset Setup

The BIOS Setup options described in this section are selected by choosing the option from the Chipset Setup screen. Chipset Setup is selected from the Setup section on the BIOS Setup main menu.

ATBUS Clock Selection

This option is used to set the ISA bus clock to the proper speed. Normally, the speed of ISA bus should be around 8Mhz. If the PCI bus clock is about 33Mhz (for 90 and 100Mhz Pentium CPU), the option should be set to PCICLK/4. If the PCI clock is about 25Mhz (for 75Mhz Pentium CPU), the option should be

set to PCICLK/3. The Optimal and FailSafe settings are set to PCICLK/4. Set to PCICLK/3 only when the Pentium speed is 75Mhz.

Base Memory Size

The base size of system DRAM memory is 640KB. The address space from 640KB to 1MB is reserved for I/O ROM and I/O RAM. Since this reserved area is normally occupied by Video RAM, Video ROM, and system BIOS ROM, there will be no 128KB of contiguous address space available. However, some add-on cards may need 128KB of contiguous address space. This option is provided so that the area from 512MB to 640KB of the system DRAM can be disabled to create a 128KB hole of address space for this purpose. The default setting is 640KB. The setting 512KB should be selected only when the type of add-on card described above is installed.

Non Cacheable Block-1

This option allows users to optionally assign a specific address space that is either located in system DRAM memory or I/O memory address space as Cacheable or Non-Cacheable. This is required to avoid memory coherency problems if the add-on card has a shared I/O memory. Three options are provided: Disabled, DRAM, or AT Bus. If DRAM or AT Bus is selected, the user can select the next two options for the size of this address space (Block Size) and its starting address (Block Base Address). The default setting should be *Disabled*.

PCI VGA Palette Snoop

This option should be *Enabled* when running with a Multimedia Video Processor Card. Once enabled, the address space of the

PCI VGA Palette can be snooped. The default Optimal and Fail-Safe default settings are *Disabled*.

PCI IDE Card Selection

This option allows users to manually assign the PCI IDE controller card to selectively PCI slots. This is only use for debug purpose. It should be set to Auto.

IRQ 9.....15 Available to

These options allow users to manually assign the system interrupts to be used either by PCI add-on cards or ISA add-on cards. Once these interrupts are assigned to PCI add-on cards, the system BIOS will automatically route the interrupt from PCI devices to these interrupts accordingly. Priority will be for whichever available. Note that care should be taken because if these interrupt levels are used by ISA add-on cards, they can not be shared by PCI add-on cards. The default setting is for *PCI* add-on cards.

16-Bit I/O Recovery Time

This option specifies the length of a delay inserted between comsecutive 16-bit I/O operations. The settings are 1(SYSCLK), 2(SYSCLKs), 3(SYSCLKs) or 4(SYSCLKs). The optimal and Fail-Safe default settings are 2.

Power Management Setup

The 54CPI supports Green or Energy saving features. With the Power saving option enabled, the system BIOS will

automatically disable or stop the operation of the system peripheral devices, as well as the system CPU, when the system is in idle mode for a certain period of time. This will save energy that is consumed by these devices. The Optimal setting is *Enabled*. The FailSafe setting is *Disabled*.

The following options are valid only when the option above is *Enabled*.

System Event Timer

This option determines the time delay before the system goes into the power saving mode from the idle states. The Optimal setting is 5 minutes.

IDE Power Down

Once this option is enabled, the IDE hard drive will stop spinning when the system goes into the power saving mode. The Optimal Setting is Disabled.

VGA Access

While the system is in an idle state, the video monitor will not go into the power saving mode when it detects that video images are being updated, for example, video screen saver. *Ignore* option enables the video monitor to ignore such video activities and go direct into power saving mode after the system is in an idle state for a certain period of time. The Optimal Setting is Disabled.

Programming Flash BIOS

To support FLASH BIOS, the component at location U19 must be a FLASH EPROM. Follow these steps to reprogram the FLASH BIOS:

1. Turn the system power OFF.
2. Open the system cover and check JS17 jumper block. If the jumper block is in the 2-3 position, change it to the 1-2 position.
3. Turn the system power ON.
4. Boot up the system and run AMIFLASH.COM Program from the Utility Diskette to load the new BIOS code into the FLASH EPROM.
5. After programming is completed, shut the system off.
6. Leave JS17 in the 1-2 position for normal operation.
7. Turn the system power ON.
8. Hit DEL key during boot up to go into the CMOS setup.
9. Use the TAB key to go to the Default Setup menu. Select Optimal icon and press YES to load the Optimal values.
10. Go to the Standard CMOS Setup to set Date, Time, Hard drive type, and Floppy drive type.
11. For manual setup, select Advanced CMOS Setup, Advanced Chipset Setup, and Power Management Setup menus to set each option indivdually.
12. After completing the setup process, press ESC and select YES to save the CMOS setup.
13. Reboot the system.

APPENDIX A: AMI BIOS HARD DISK TYPE

Type	Cylinder	Heads	Write Precomp	Landing Zone	Sectors	Size
1	306	4	128	305	17	10MB
2	615	4	300	615	17	20MB
3	615	6	300	615	17	31MB
4	940	8	512	940	17	62MB
5	940	6	512	940	17	47MB
6	615	4	65535	615	17	20MB
7	462	8	256	511	17	31MB
8	733	5	65535	733	17	30MB
9	900	15	65535	901	17	112MB
10	820	3	65535	820	17	20MB
11	855	5	65535	855	17	35MB
12	855	7	65535	855	17	50MB
13	306	8	128	319	17	20MB
14	733	7	65535	733	17	43MB
16	612	4	0	663	17	20MB
17	977	5	300	977	17	41MB
18	977	7	65535	977	17	57MB
19	1024	7	512	1023	17	60MB
20	733	5	300	732	17	30MB
21	733	7	300	732	17	43MB
22	733	5	300	733	17	30MB
23	306	4	0	336	17	10MB
24	925	7	0	925	17	54MB
25	925	9	65535	925	17	69MB
26	754	7	754	754	17	44MB
27	754	11	65535	754	17	69MB
28	699	7	256	699	17	41MB

Type	Cylinder	Heads	Write Precomp	Landing Zone	Sectors	Size
29	823	10	65535	823	17	68MB
30	918	7	918	918	17	53MB
31	1024	11	65535	1024	17	94MB
32	1024	15	65535	1024	17	128MB
33	1024	5	1024	1024	17	43MB
34	612	2	128	612	17	10MB
35	1024	9	65535	1024	17	77MB
36	1024	8	512	1024	17	68MB
37	615	8	128	615	17	41MB
38	987	3	987	987	17	25MB
39	987	7	987	987	17	57MB
40	820	6	820	820	17	41MB
41	977	5	977	977	17	41MB
42	981	5	981	981	17	41MB
43	830	7	512	830	17	48MB
44	830	10	65535	830	17	69MB
45	917	15	65535	918	17	114MB
46	1224	15	65535	1223	17	152MB
47	USER'S	TYPE				

APPENDIX B: ISA I/O ADDRESS MAP

I/O ADDRESS (HEX)	I/O DEVICE
000 - 01F	DMA Controller 1, 8237A-5
020 - 03F	Interrupt Controller 1, 8259A
040 - 05F	System Timer, 8254-2
060 - 06F	8742 Keyboard Controller
070 - 07F	Real-Time Clock/CMOS and NMI Mask
080 - 09F	DMA Page Register, 74LS612
0A0 - 0BF	Interrupt Controller 2, 8259A
0C0 - 0DF	DMA Controller 2, 8237A-5
0F0 - 0FF	i486 Math Coprocessor
1F0 - 1F8	Fixed Disk Drive Adapter
200 - 207	Game I/O
20C - 20D	Reserved
21F	Reserved
278 - 27F	Parallel Printer Port 2
2B0 - 2DF	Alternate Enhanced Graphic Adapter
2E1	GPIB Adapter 0
2E2 - 2E3	Data Acquisition Adapter 0
2F8 - 2FF	Serial Port 2 (RS-232-C)
300 - 31F	Prototype Card
360 - 363	PC Network (Low Address)
364 - 367	Reserved
368 - 36B	PC Network (High Address)
36C - 36F	Reserved
378 - 37F	Parallel Printer Port 1
380 - 38F	SDLC, Bisynchronous 2
390 - 393	Cluster
3A0 - 3AF	Bisynchronous 1
3B0 - 3BF	Monochrome Display and Printer Adapter

I/O ADDRESS (HEX)	I/O DEVICE
3C0 - 3CF	Enhanced Graphics Adapter
3D0 - 3DF	Color/Graphics Monitor Adapter
3F0 - 3F7	Diskette Drive Controller
3F8 - 3FF	Serial Port 1 (RS-232-C)
6E2 - 6E3	Data Acquisition Adapter 1
790 - 793	Cluster Adapter 1
AE2 - AE3	Data Acquisition Adapter 2
B90 - B93	Cluster Adapter 2
EE2 - EE3	Data Acquisition Adapter 3
1390 - 1393	Cluster Adapter 3
22E1	GPIB Adapter 1
2390 - 2393	Cluster Adapter 4
42E1	GPIB Adapter 2
62E1	GPIB Adapter 3
82E1	GPIB Adapter 4
A2E1	GPIB Adapter 5
C2E1	GPIB Adapter 6
E2E1	GPIB Adapter 7

APPENDIX C: MEMORY MAPPING

Address (hex)	Function	Comments
00000000-0007FFFF	512K System RAM	Cached
00080000-0009FFFF	128K System RAM	Cached
000A0000-000BFFFF	128K Video RAM	Not Cached
000C0000-000C7FFF	32K Video BIOS	Cached
000C8000-000CFFFF	32K I/O ROM	Not Cached
000D0000-000DFFFF	64K I/O ROM	Not Cached
000E0000-000EFFFF	64K Extended BIOS	Not Cached
000F0000-000FFFFF	64K On-Board BIOS ROM	Cached
00100000-00BFFFFF	System Memory (RAM)	Cached
00C00000-00FFFFFF	System Memory (RAM)	Cached
01000000-BFFFFFFF	System Memory (RAM)	Cached
C0000000-C1FFFFFF	System Memory (RAM)	Cached
C2000000-FFFDFFFF	System Memory	Cached
FFFE0000-FFFFFFFF	128K On-Board BIOS ROM	Not cached

APPENDIX D: INTERRUPT LEVEL ASSIGNMENTS

LEVEL on SYSTEM	LEVEL on IO BUS	TYPICAL INTERRUPT SOURCE
NMI	None	Parity, ISA/EISA Channel Check, Bus Time Out, Fail Safe Timer Timeout
IRQ0	None	Interval Timer 1, Counter 0 Out
IRQ1	None	Keyboard Controller
IRQ2	None	Cascade Interrupts from IRQ8 to IRQ15
IRQ3	IRQ3	Serial Port 2
IRQ4	IRQ4	Serial Port 1
IRQ5	IRQ5	Parallel Port 2
IRQ6	IRQ6	Diskette Controller
IRQ7	IRQ7	Parallel Port 1
IRQ8	None	Real Time Clock
IRQ9	IRQ2	Expansion Bus Pin
IRQ10	IRQ10	Expansion Bus Pin
IRQ11	IRQ11	Expansion Bus Pin
IRQ12	IRQ12	Expansion Bus Pin
IRQ13	None	Coprocessor Error, DMA Chaining
IRQ14	IRQ14	Fixed Disk Drive Controller Expansion Bus Pin
IRQ15	IRQ15	Expansion Bus Pin

PRODUCT INFORMATION RECORD

Record all the information as you receive the product and provide to your supplier in writing in the event that you should need technical support assistance. This will help to speed up the response and get your problem solved.

System Board

Date Purchased or Received: _____

Purchased From: _____

Product Name: _____PCB Ver:_____ Rev: ___

Serial Number: _____

CPU Processor Speed: _____Memory Size: _____

BIOS Version: _____ Software Driver Rel #: _____

PCI Add-on Cards:

Model #_____ Interrupt:_____ Slot #:_____

Model #_____ Interrupt:_____ Slot #:_____

Model #_____ Interrupt:_____ Slot #:_____

ISA Add-on Cards:

Model #_____Interrupt:____ DMA: ____ Slot #:_____

Model #_____Interrupt:____ DMA: ____ Slot #:_____

Model #_____Interrupt:____ DMA: ____ Slot #:_____

Model #_____Interrupt:____ DMA: ____ Slot #:_____