H I P P O - S X

REVISION: 1.0

RADIO FREQUENCY INTERFERENCE STATEMENT

This equipment generates and uses radio frequency energy and if not installed and used properly, that is, in strict accordance with the manufacturer's instructions, may cause interference with radio and television reception.

If this equipment does cause interference to radio or TV reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

* Reorient the receiving antenna.
* Relocate the computer away from the receiver.
* Move the computer away from the receiver.
* Plug the computer into a different outlet so that computer and receiver are on different branch circuits.
* Ensure that card slot covers are in place when no card is installed.
* Ensure that card mounting screws, attachment connector screws, and ground wires are tightly secured.
* If peripherals are used with this system, it is suggested to use shielded, grounded cables, with in-line filters if necessary.

If necessary, the user should consult the dealer service representative for additional suggestions.

The manufacturer is not responsible for any radio or TV interference caused by unauthorized modifications to this equipment. It is the responsibility of the user to correct such interference.

Note

1. Electronic components are sensitive to dust and dirt. Do inspect and clean the computer system regularly.

2. Turn off the power whenever you install or remove any connector, memory module and add-on card. Before turning on the power, make sure that all the connectors, memory modules and add-on cards are secured.

3. After power is on, wait for a minute. The system BIOS are going through a self-test during this period and nothing is shown on the screen. After the self-test, the system BIOS will initialize the display adaptor and show messages.

4. The SIMM sockets are fragile device. Do not force the SIMM modules into the sockets. It may break the locking latches.

Preface

This manual provides information about the installation and maintenance of OCTEK Hippo-SX motherboard. In-depth explanations of the functions of this motherboard are provided.

The content in this manual is only for reference and is intended to provide the basic information for the general users. There are also technical information for hardware and software engineers.

In this manual, there are 4 chapters. Chapter 1 contains a brief introduction. In Chapter 2, the specification and functions of OCTEK Hippo-SX motherboard are explained. It also outlines many advanced features of the CPU and the system architecture. Chapter 3 explains the installation of coprocessor, DRAM modules and jumpers. Technical information is provided in Chapter 4.

Memory expansion card is described in Appendix A. Appendix B contains the informa-tion about the Hippo Cache Card. Additional information is given in the Appendix C, D, E, F, and G for maintenance purpose.

Table of Content

Chapter 1
Introduction

OCTEK Hippo-SX provides excellent computing performance at low cost. The heart of Hippo-SX is the 80486SX which combines CPU and internal cache memory on a single chip. Incorporated with a highly integrated chipset, OCTEK Hippo-SX fully takes advantage of the power of 80486SX and provides high performance, reliability and compatibility to the user. OCTEK Hippo-SX is suitable for those users who need power for the daily computing applications and network operations.

The burst read mode is supported and thus the data is transferred to CPU at full speed. Furthermore, the chipset supports a optional secondary 128K bytes cache memory. Installation is very simple.

If you want more speed in numeric operation, WEITEK 4167 can be installed. 256KB, 1MB and 4MB SIMM RAM modules are supported. 32MB memory can be installed on board.

Fast A20 gate and fast reset generation are incorporated to improve the performance of advanced operation system and expanded memory managers.

Compatibility and reliability are important issues. I/O channel is compatible to standard AT bus. Therefore any peripheral may be used on OCTEK Hippo-SX. On board POWERGOOD generator is essential to ensure the reliability of the system and is well-designed to work with all power supplies.

Chapter 2
General Features

SPECIFICATION

Processor :

Intel 80486SX CPU
with optional WEITEK 4167 Co-processor

Speed :

Turbo/normal speed

I/O Slot :

Compatible to standard AT bus
Eight 16-bit slots

Optional Secondary Cache Memory :

128KB Direct mapped/Write through

Memory :

Shadow RAM and Memory remapping
Page/Interleaved mode
Flexible configuration
SIMM sockets for 256K, 1M and 4M modules
Maximum 32MB on board

GENERAL FEATURES

System support functions :

- 8-Channel DMA (Direct Memory Access)
- 16-level interrupt
- 3 programmable timers
- CMOS RAM for system configuration
- Real time clock with battery back-up
- Fast A20 gate and fast reset

Other Features :

- On board POWERGOOD generation
- External battery connector

PROCESSOR

80486SX is the powerful microprocessor which merges many innovative features on a single chip, suitable for commercial applications and advanced operation systems. 80486SX is a 32-bit microprocessor with 32-bit external data bus and 32-bit external address bus. It is fully binary compatible with existing Intel's CPU. All existing software for PC XT/AT can be used on OCTEK Hippo-SX.

Cache memory can improve the overall performance of a computer system. Nevertheless, if the cache memory is separated from CPU, CPU still needs to fetch code and data from external bus. That means the data transfer rate should not be too fast to allow the external devices to keep pace with the CPU. In 80486SX, the cache controller and cache memory are integrated into the chip. Most of the operations can be carried out inside the CPU, which reduces the bus operation on external data and address bus and thus speeds up the internal execution.

The cache memory is a 8K bytes, 16 bytes line size, four-way set associative configuration. The hit rate of this configuration is much better than 32K bytes two-way set associative external cache because a four-way set associative architecture provides better performance in a multitasking and multi-processor environment.

If a read miss occurs, the CPU will initiate a burst mode read operation. In burst mode read operation, CPU performs four successive read operations each of which takes only one cycle. Total 128 bits data are fetched into the CPU's internal cache. Since burst mode read operation is very fast, the traffic of the CPU bus is greatly reduced and the bus is available to other bus masters, such as DMA controller.

By eliminating the access to external bus, operations with the internal cache can be completed in a single cycle. 80386DX at least needs two cycles for an operation. To further increase the rate of data transfer inside the CPU, the internal bus of the cache memory is increased to 128 bits, which is four times of the external bus. Since, in most of the time, the CPU is using the internal cache, the large bus size substantially improves the overall performance.

When the CPU writes data to the main memory, the data is first stored in a write buffer. There are four write buffers. When the external bus is idle, data will be sent to the main memory. If all buffers are filled, it can start write operation in burst mode. Since the internal cache is updated immediately, the CPU need not suspend its operation and there is no need to wait for the external device to update the main memory.

Many often-used instructions are executed in a clock cycle and some instructions are modified to take fewer cycles than in 80386DX. On the contrary, 80386DX may take two to three more cycles for the same instruction. The CPU contains an advanced instruction pipeline structure and a 32-byte code queue to speed up the execution.

80486SX includes all the functions of 80386DX and is able to support sophisticated software and operation systems which are widely employed now. It is able to operate in real mode, protected mode and virtual 8086 mode. A new addressing mechanism allows switching between modes more efficiently. Hence

applications using EMS memory can run efficiently although they only use software drivers to emulate EMS memory.

Internal memory management unit provides a flexible addressing scheme for the next generation operation system. Multitasking, concurrent operation and manipulating huge data base can be accomplished with excellent performance. Paging mechanism is employed to allow powerful operating system to implement virtual memory. Each segment is divided into several pages which are 4K bytes per page. Page mechanism is transparent to software and allows software to address 64 terabytes. Furthermore, the 64KB segment boundary which is an barrier of 8088 and 80286 is removed and the segment length can be increased up to 4GB.

SECONDARY CACHE MEMORY

Although there is 8K bytes internal cache memory inside the CPU, a secondary cache memory is still necessary when the size of main memory is large.

In a single user system, when only DOS is used and few megabytes memory is installed, the internal cache memory is adequate and the performance is still very high.

In a multi-user or multitasking environment, CPU has to switch from one process to another, which involves a large mount of data transfer. The performance to a great extent depends on the data transfer rate. In a 80486SX system, a large portion of the internal cache memory has to be updated to the main memory and then the data for another process is retrieved into the cache memory. The low speed main memory will substantially slow down the system.

In order to shorten the time required for switching between processes, a secondary cache memory is needed as a buffer between the slow speed main memory and the internal cache memory of 80486SX. Wait state is thus eliminated when the CPU reads external data from the secondary cache memory. Furthermore, the secondary cache memory can support the burst mode of 80486SX. The CPU is able to run at full speed.

Since there is already a 8K bytes cache memory in 80486SX, a small cache memory, such as 32K bytes, can not substantially improved the performance. On the other hand, the secondary cache should be able to contain a copy of the internal cache memory or more, which means data of different processes can coexist in the secondary cache memory. So, an optimal size is 128K or 512K bytes and this size is adequate for over 8M bytes main memory.

In Hippo-SX, the secondary cache controller is incorporated in the chipset. There is no need to install an external cache controller. If the secondary cache memory is needed, just plug in the secondary cache memory card and enable secondary card in the BIOS setup. It reduces the cost for upgrading the system.

MEMORY SYSTEM

Four banks of DRAMs can be installed. Two banks are available on motherboard and others are on optional memory expansion board. The maximum memory size is 32MB when using 4MB DRAM.

The memory system provides a flexible memory configuration. 256KB and 1MB DRAM can be mixed together. Several combinations of DRAM types are allowed. So, a basic system is equipped with 1MB using 256KB DRAM and then memory size is increased to 5MB by putting another bank of 1MB DRAM.

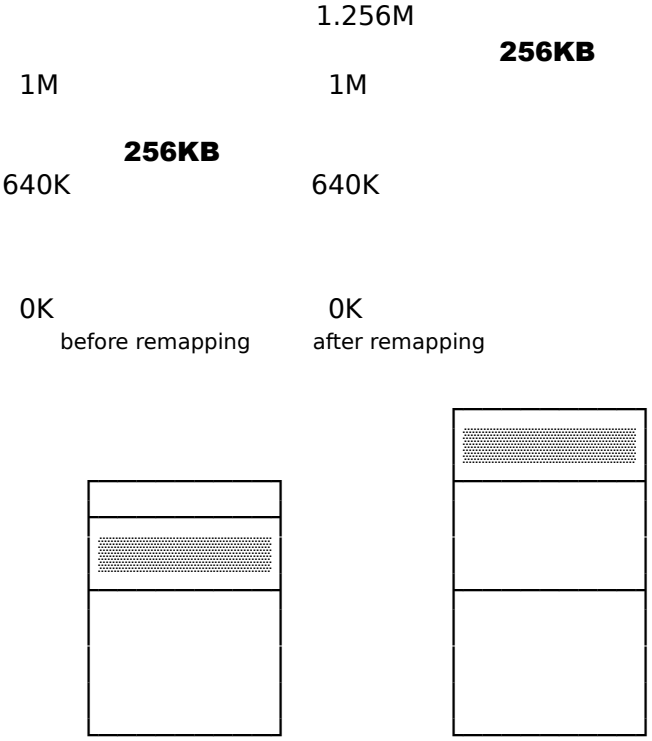
When using 4MB modules, you may install up to two banks. So the memory size is either 16MB or 32MB. 4MB module cannot work with other memory types.

The memory system supports page-inter-leaved mode. The memory is divided into pages. Successive memory accesses within the same page need not require wait state. When more than one bank of memory are installed, the page size is effectively increased because several banks of memory can be kept active. If four banks are filled, the page size is increased by a factor of four.

To enhance the system performance, shadow RAM mode is supported. In shadow RAM mode, system BIOS and video BIOS contained in low speed memory such as EPROM and ROM are copied into DRAM. Improvement is significant because access to DRAM is mush faster than ROM.

Another useful feature is memory remapping. 640KB is allocated as base memory. System BIOS and video BIOS occupy some locations between 640K and 1M. When 1M bytes or more are installed, there are some parts of DRAM overlapping with the BIOS and cannot be accessed. Memory remapping allows these parts of memory to be accessed at other locations and

thus is available to software.

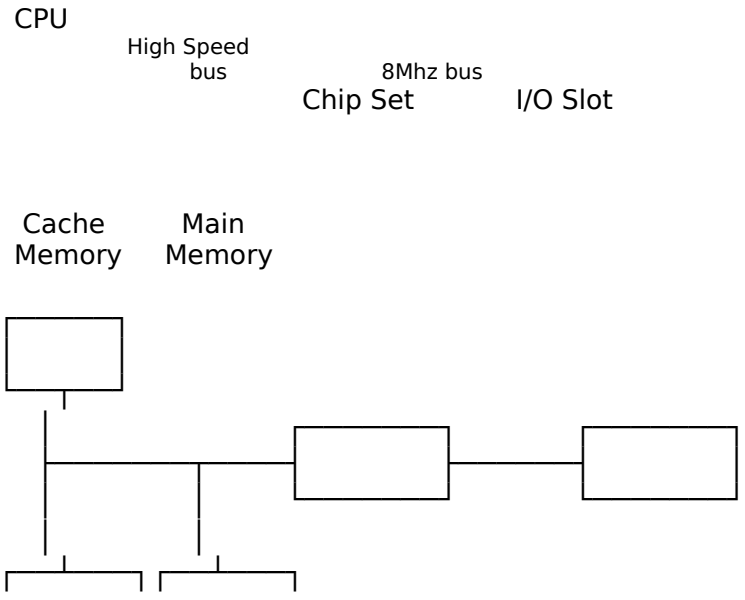


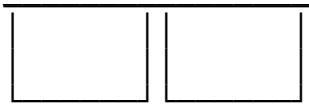
Memory remapping

DUAL BUS DESIGN

It is very important that a high speed system should be compatible with existing peripherals without lowering the performance. To be compatible, the I/O slot should run at 8MHz or slower. On the other hand, the rest of the system are running at full speed.

In Hippo-SX, a dual bus design is employed. A high speed bus links the CPU, coprocessor, cache memory and main memory. This bus is synchronous with clock of the CPU and the data transfer is 32 bits. Whenever there is a request for transferring data to or from I/O slot, the chipset is responsible for handling the conversion between the bus. The clock rate of the high speed bus will not be reduced, which eliminates many compatibility problem.





Chapter 3
Configuring The System

Important Note : Turn off the power before installing or replacing any component.

INSTALLING MATH COPROCESSOR

Math coprocessor WEITEK 4167 is a PGA devices. Beside the CPU, there is a 144-pin PGA socket. To install Math Coprocessor, be sure to line up pin 1 of the Math coprocessor with pin 1 of the socket as shown below.

Before installing the Math coprocessor, make sure that all the pins are straight. The pins are very fragile. Once these pins are bent, the coprocessor may be damaged.

The Math coprocessor is automatically detected by the system and the applications. No jumper is needed to be set.

INSTALLING RAM MODULES

OCTEK Hippo-SX has eight sockets for SIMM modules. Whenever you add memory to the motherboard, install four modules at the same time. Also make sure that the chips on the modules face towards CPU. The modules should be locked by the sockets. Please check carefully before turning on the power. Otherwise, the system will not work properly.

To install a module, the module edge is angled into the socket's contact and then the module is pivoted into position, where the locking latches will secure it. If the module edge is not completely inserted into the socket, it cannot be pivoted to be in vertical position and should be dragged out and re-inserted again. Do not force the module into the SIMM socket. It will damage the locking latches.

The modules should be locked by the locking latches of the sockets firmly. Please check carefully before turning on the power. Otherwise, the system will not work properly.

If the BIOS reports an memory error or parity error, drag out the modules and insert them again. If the locking latches are damaged, contact your dealer to replace the socket.

CONFIGURATION OF MEMORY

The configuration of the memory is very flexible. There are several combinations of DRAM types you may consider. Either 256KB or 1MB SIMM are acceptable.

There are totally four banks of DRAM. Two banks (bank 0 and 1) are on the motherboard and the others (bank 2 and 3) are on the memory expansion board. If bank 0 and 1 are filled, you have to use bank 2 and 3. If you use 4MB module, bank 2 and bank 3 are not used.

Page mode is always active. Interleaved mode is only enabled for those banks with similar pairs or quartet of DRAMs. The memory size is detected automatically by system BIOS and indicated during memory test after reset. No jumper is needed to be set for the memory size and DRAM type.

To determine what DRAM speed rating should be used depends on the system speed and wait state. The highest performance is accomplished by using zero wait state, but high speed DRAM has to be used. If zero wait state is selected, fast page mode DRAM is needed.

Select zero wait state for 100ns DRAM or faster. 120ns DRAM can be used for 1 wait state. The wait state setting is applied to four banks of memory. Therefore make sure to install DRAM with the same speed rating, or accom-modate the wait state setting to the new DRAM type.

Because of the shadow RAM and memory remapping feature, the memory size may not equal to the actual memory size. For example, there is 1MB on board. If memory remapping is disabled, the BIOS will show 640KB. After enabled, the memory size is increased to 896KB. The rest of the memory (128KB) is assigned for shadow RAM and can not be used by software.

The number of wait state is assigned in the BIOS setup. Improper setting may make the system malfunction. In this case, reset the CMOS setup using JP11. Then reset the system and go through the system setup again.

DRAM CONFIGURATION

	Bank 0	Bank 1	Bank 2	Bank 3	Total Memory	Inter-leaved
1	0	0	0	0	0	
2	256K	0	0	0	1M	2W
3	256K	256K	0	0	2M	2W
4	256K	256K	256K	0	3M	
5	256K	256K	256K	256K	4M	4W
6	1M	0	0	0	4M	
7	256K	1M	0	0	5M	
8	1M	256K	0	0	5M	
9	256K	256K	1M	0	6M	2W
10	256K	1M	256K	0	6M	
11	1M	256K	256K	0	6M	
12	256K	256K	1M	256K	7M	2W
13	256K	1M	256K	256K	7M	2W
14	1M	256K	256K	256K	7M	2W
15	1M	1M	0	0	8M	2W
16	256K	1M	1M	0	9M	
17	1M	1M	256K	0	9M	2W
18	1M	256K	1M	0	9M	
19	256K	256K	1M	1M	10M	2W
20	256K	1M	1M	256K	10M	
21	1M	1M	256K	256K	10M	2W
22	1M	256K	1M	256K	10M	
23	1M	1M	1M	0	12M	2W
24	256K	1M	1M	1M	13M	2W

25	1M	1M	1M	256K	13M	2W
26	1M	256K	1M	1M	13M	2W
27	1M	1M	1M	1M	16M	4W
28	4M				16M	
29	4M	4M			32M	2W

CONTROL OF SYSTEM SPEED

System speed can be controlled by keyboard. To change the speed by keyboard, use **`-'** and **`+'** of the numeric keypad. Press **`Ctrl' `Alt'** and **`-'** for slow speed and press **`Ctrl' `Alt'** and **`+'** for fast speed.

RESET CMOS SETUP INFORMATION

Sometimes, the improper setting of system setup may make the system malfunction. In this case, turn off the power and set JP1 to 1-2 for a while. The internal CMOS status register is reset. Then set the jumper to 2-3 and turn on the power. The BIOS finds the CMOS status register is reset and regards the setup information is invalid. So it will prompt you to correct the information.

If you just want the BIOS to discard the register settings, you select the XCMOS SETUP, press `INS' on the keyboard for a few seconds after power up. The BIOS will detect the key stroke and use the default setting for booting.

SYSTEM BOARD JUMPER SETTING

There are several options which allows user to select by hardware switches. JP3 and JP4 are reserved.

Display Selection

JP2	
ON	CGA, EGA, VGA
OFF	Monochrome display *

Secondary Cache Installation

	Secondary	Cache
JP5 & JP6	Installed	Not installed
	OFF	ON *

Note : * factory setting

SYSTEM BOARD CONNECTORS

Under typical conditions, these connectors should be connected to the indicators and switches of the system unit. The functions of connectors on the version 2.0 motherboard are listed below.

Connector	Function
SW1	Hardware reset connector
J26	Speaker connector
J27	Power LED & Ext-lock connector
J11, J12	Power supply connector
J1	External battery connector
J2	Keyboard connector
J25	NOT Used

Pin assignment of the connector are illustrated as follows:

SW 1 - Hardware Reset Connector

Pin	Assignment
1	Selection Pin
2	Ground

J 1 - External Battery Connector

Pin	Assignment
1	+ Vdc
2	not used
3	Ground
4	Ground

J 2 - Keyboard Connector

Pin	Assignment
1	Keyboard clock
2	Keyboard data
3	Spare
4	Ground
5	+5 Vdc

J 26 - Speaker Connector

Pin	Assignment
1	Data out
2	+5 Vdc
3	Ground
4	+5 Vdc

J 27 - Power LED & Ext-Lock Connector

Pin	Assignment
1	+5 Vdc
2	Key
3	Ground
4	Keyboard inhibit
5	Ground

J 11, J 12 - Power Supply Connector

Pin	Assignment
1	POWERGOOD
2	+5 Vdc
3	+12 Vdc
4	-12 Vdc
5	Ground
6	Ground

Pin	Assignment
1	Ground
2	Ground
3	-5 Vdc
4	+5 Vdc
5	+5 Vdc

6	+5 Vdc

Chapter 4
Technical Information

This section provides technical information about OCTEK Hippo-SX and is intended for advanced users interested in the basic design and operation of OCTEK Hippo-SX.

MEMORY MAPPING

Address	Range	Function
000000-7FFFFF	000K-512K	System Board Memory (512K)
080000-09FFFF	512K-640K	System Board Memory (128K)
0A0000-0BFFFF	640K-768K	Display Buffer (128K)
0C0000-0DFFFF	768K-896K	Adaptor ROM / Shadow RAM (128K)
0E0000-0EFFFF	896K-960K	System ROM / Shadow RAM (64K)
0F0000-0FFFFF	960K-1024K	System BIOS ROM / Shadow RAM (64K)
100000-7FFFFF	1024K-8192K	System Memory
800000-FFFFFF	8192K-16318K	System Memory

I/O ADDRESS MAP

I/O Address Map on System Board

I/O address hex 000 to 0FF are reserved for the system board I/O.

ADDRESS (HEX)	DEVICE
000-01F	DMA Controller 1, 8237
020-03F	Interrupt Controller 1, 8259, Master
040-05F	Timer, 8254
060-06F	Keyboard Controller
070-07F	Real Time Clock, NMI (non-maskable interrupt) mask
080-09F	DMA Page Register, 74LS612
0A0-0BF	Interrupt Controller 2, 8259
0C0-0DF	DMA Controller 2, 8237
0F0	Clear Math Coprocessor Busy
0F1	Reset Math Coprocessor
0F8-0FF	Math Coprocessor Port

I/O address hex 100 to 3FF are available on the I/O channel.

ADDRESS (HEX)	DEVICE
1F0-1F8	Fixed Disk
200-207	Game I/O
278-27F	Parallel Printer Port 2
2F8-2FF	Serial Port 2
300-31F	Prototype Card
360-36F	Reserved
378-37F	Parallel Printer Port 1
380-38F	SDLC, bisynchronous 2
3A0-3AF	Bisynchronous 1
3B0-3BF	Monochrome Display and Printer Adapter
3C0-3CF	Reserved
3D0-3DF	Color Graphics Monitor Adapter
3F0-3F7	Diskette Controller
3F8-3FF	Serial Port 1

SYSTEM TIMERS

OCTEK Hippo-SX has three programmable timer/counters controlled by 82C206 and they are defined as channels 0 through 2:

Channel 0	System Timer
Gate 0	Tied on
Clk in 0	1.190 Mhz OSC
Clk out 0	8259 IRQ 0

Channel 1	Refresh Request Generator
Gate 1	Tied on
Clk in 1	1.190 Mhz OSC
Clk out 1	Request Refresh Cycle

Channel 2	Tone Generation of Speaker
Gate 2	Controlled by bit 0 of port hex 61 PPI bit
Clk in 2	1.190 Mhz OSC
Clk out 2	Used to drive the speaker

Note : Channel 1 is programmed to generate a 15-micro-second period signal.

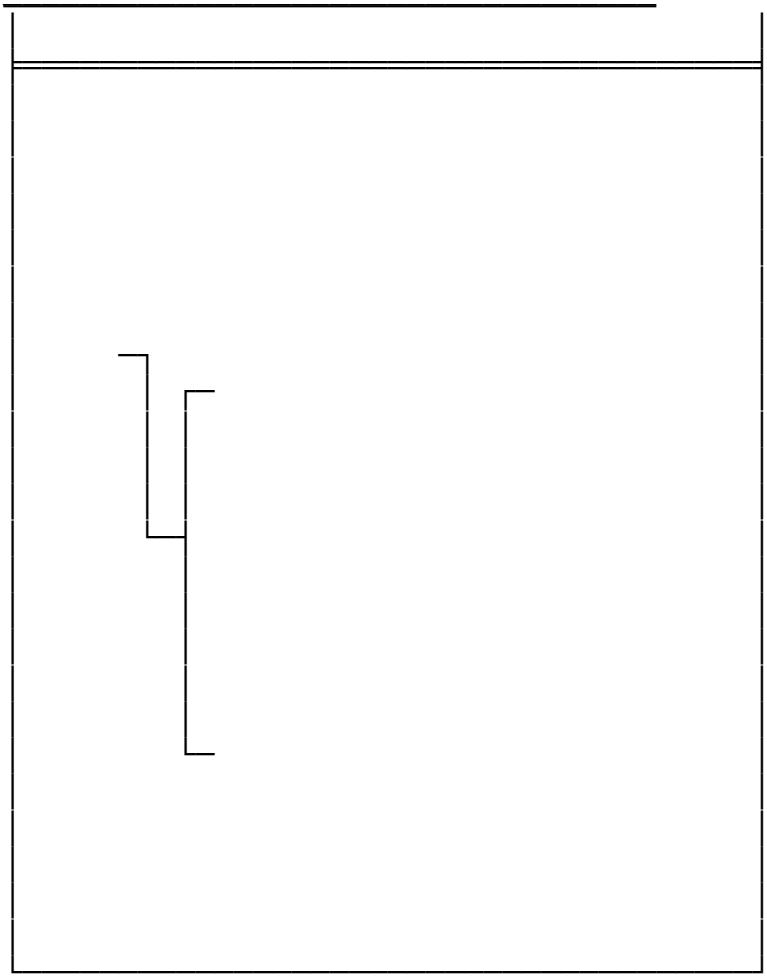
The 8254 Timer/Counters are treated by system programs as an arrangement of four programmable external I/O ports. Three are treated as counters and the fourth is a control register for mode programming.

SYSTEM INTERRUPTS

Sixteen levels of system interrupts are provided on OCTEK Hippo-SX. The following shows the interrupt-level assignments in decreasing priority.

Level		Function
Microprocessor NMI		Parity or I/O Channel Check
Interrupt Controllers		
CTLR 1	CTLR 2	
IRQ0		Timer Output 0
IRQ1		Keyboard (Output Buffer Full)
IRQ2		Interrupt from CTLR 2
	IRQ8	Real-time Clock Interrupt
	IRQ9	Software Redirected to INT 0AH (IRQ2)
	IRQ10	Reserved
	IRQ11	Reserved
	IRQ12	Reserved
	IRQ13	Coprocessor
	IRQ14	Fixed Disk Controller
	IRQ15	Reserved
IRQ3		Serial Port 2
IRQ4		Serial Port 1
IRQ5		Parallel Port 2
IRQ6		Diskette Controller
IRQ7		Parallel Port 1

TECHNICAL INFORMATION



DIRECT MEMORY ACCESS (DMA)

OCTEK Hippo-SX supports seven DMA channels.

Channel	Function
0	Spare (8 bit transfer)
1	SDLC (8 bit transfer)
2	Floppy Disk (8 bit transfer)
3	Spare (8 bit transfer)
4	Cascade for DMA Controller 1
5	Spare (16 bit transfer)
6	Spare (16 bit transfer)
7	Spare (16 bit transfer)

The following shows the addresses for the page register.

Page Register	I/O Address (HEX)
DMA Channel 0	0087
DMA Channel 1	0083
DMA Channel 2	0081
DMA Channel 3	0082
DMA Channel 5	008B
DMA Channel 6	0089
DMA Channel 7	008A
Refresh	008F

REAL TIME CLOCK AND CMOS RAM

Real time clock and CMOS RAM are contained on board. Real time clock provides the system date and time. CMOS RAM stores system information. Both are backed up by battery and will not lose information after power off. The following page shows the CMOS RAM Address Map.

CMOS RAM ADDRESS MAP

Addresses	Description
00-0D	* Real-time clock information
0E	* Diagnostic status byte
0F	* Shutdown status byte
10	Diskette drive type byte - drives A and B
11	Reserved
12	Fixed disk type byte - drives C and D
13	Reserved
14	Equipment byte
15	Low base memory byte
16	High base memory byte
17	Low expansion memory byte
18	High expansion memory byte
19-2D	Reserved
2E-2F	2-byte CMOS checksum
30	* Low expansion memory byte
31	* High expansion memory byte
32	* Date century byte
33	* Information flags (set during power on)
34-3F	Reserved

REAL TIME CLOCK INFORMATION

The following table describes real-time clock bytes and specifies their addresses.

Byte	Function	Address
0	Seconds	00
1	Second alarm	01
2	Minutes	02
3	Minute alarm	03
4	Hours	04
5	Hour alarm	05
6	Day of week	06
7	Date of month	07
8	Month	08
9	Year	09
10	Status Register A	0A
11	Status Register B	0B
12	Status Register C	0C
13	Status Register D	0D

SYSTEM EXPANSION BUS

OCTEK Hippo-SX provides eight 16-bit slots.

The I/O channel supports:

* I/O address space from hex 100 to hex 3FF
* Selection of data access (either 8 or 16 bit)
* 24 bit memory addresses (16MB)
* Interrupts
* DMA channels
* Memory refresh signal

The following figure shows the pin numbering for I/O channel connectors (side A and B).

The following figure shows the pin numbering for I/O channel connectors (side C and D).

The following tables summarize pin assignments for the I/O channel connectors.

I/O Channel (A-Side)

I/O Pin	Signal Name	I/O
A1	-I/O CH CK	I
A2	SD7	I/O
A3	SD6	I/O
A4	SD5	I/O
A5	SD4	I/O
A6	SD3	I/O
A7	SD2	I/O
A8	SD1	I/O
A9	SD0	I/O
A10	-I/O CH RDY	I
A11	AEN	O
A12	SA19	I/O
A13	SA18	I/O
A14	SA17	I/O
A15	SA16	I/O
A16	SA15	I/O
A17	SA14	I/O
A18	SA13	I/O
A19	SA12	I/O
A20	SA11	I/O
A21	SA10	I/O
A22	SA9	I/O

A23	SA8	I/O
A24	SA7	I/O
A25	SA6	I/O
A26	SA5	I/O
A27	SA4	I/O
A28	SA3	I/O
A29	SA2	I/O
A30	SA1	I/O
A31	SA0	I/O

I/O Channel (B-Side)

I/O Pin	Signal Name	I/O
B1	GND	Ground
B2	RESET DRV	I
B3	+5 Vdc	Power
B4	IRQ9	I
B5	-5 Vdc	Power
B6	DRQ2	I
B7	-12 Vdc	Power
B8	0WS	I
B9	+12 Vdc	Power
B10	GND	Ground
B11	-SMEMW	O
B12	-SMEMR	O
B13	-IOW	I/O
B14	-IOR	I/O
B15	-DACK3	I
B16	DRQ3	O
B17	-DACK1	I
B18	DRQ1	O
B19	-Refresh	I/O
B20	CLK	O
B21	IRQ7	I
B22	IRQ6	I
B23	IRQ5	I
B24	IRQ4	I
B25	IRQ3	I

B26	-DACK2	O
B27	T/C	O
B28	BALE	O
B29	+5 Vdc	Power
B30	OSC	O
B31	GND	Ground

I/O Channel (C-Side)

I/O Pin	Signal Name	I/O
C1	SBHE	I/O
C2	LA23	I/O
C3	LA22	I/O
C4	LA21	I/O
C5	LA20	I/O
C6	LA19	I/O
C7	LA18	I/O
C8	LA17	I/O
C9	-MEMR	I/O
C10	-MEMW	I/O
C11	SD8	I/O
C12	SD9	I/O
C13	SD10	I/O
C14	SD11	I/O
C15	SD12	I/O
C16	SD13	I/O
C17	SD14	I/O
C18	SD15	I/O

I/O Channel (D-Side)

I/O Pin	Signal Name	I/O
D1	-MEM CS16	I
D2	-I/O CS16	I
D3	IRQ10	I
D4	IRQ11	I
D5	IRQ12	I
D6	IRQ15	I
D7	IRQ14	I
D8	-DACK0	O
D9	DRQ0	I
D10	-DACK5	O
D11	DRQ5	I
D12	-DACK6	O
D13	DRQ6	I
D14	-DACK7	O
D15	DRQ7	I
D16	+5 Vdc	Power
D17	-MASTER	I
D18	GND	Ground

Appendix A
Memory Expansion Card

Memory expansion card contains bank 2 and bank 3 of memory. There are 8 SIMM modules on the card and total memory on this card is 8MB. Please refer to Chapter 3 for the configuration of the memory.

After installing the memory card, the system BIOS will determine the type of DRAM and the amount of total memory. There is no need to set any jumper. The system BIOS will prompt you to setup the memory size after re-boot.

However, you should make sure that the memory on the memory expansion board can be used reliably with the current setting of wait state. If there is any problem, increase the number of wait state.

There is a mounting plate on rear of the card. This mounting plate is used to keep the card on the slot firmly. Use a screw to fasten the card to the case.

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Appendix B
Hippo Cache Card

There are 128K bytes cache memory on the Hippo cache card. The expansion slot beside the CPU is dedicated to this card.

To setup the cache controller, follow the steps described below.

1. Turn off the power and plug in the card;
2. Turn on the power and enter CMOS SETUP;
3. Enable the cache memory;
4. Turn off the power again and then remove the mini jumper on JP5 and JP6;
5. Turn on the power and the cache card can be used.

If you want to remove the cache memory card, disable the cache memory in CMOS SETUP. Then you should turn off the power and place mini jumpers on JP5 and JP6 before removing the cache memory card.

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Appendix C
Operation and Maintenance

STATIC ELECTRICITY

When installing or removing any add-on card, DRAM module or coprocessor, you should discharge the static electricity on your body. Static electricity is dangerous to electronic device and can build-up on your body. When you touch the add-on card or motherboard, it is likely to damage the device. To discharge the static electricity, touch the metal of your computer. When handling the add-on card, don't contact the components on the cards or their "golden finger". Hold the cards by their edges.

KEEPING THE SYSTEM COOL

The motherboard contains many high-speed components and they will generate heat during operation. Other add-on cards and hard disk drive can also produce a lot of heat. The temperature inside the computer system may be very high. In order to keep the system running stably, the temperature must be kept at a low level. A easy way to do this is to keep the cool air circulating inside the case. The power supply contains a fan to blow air out of the case. If you find that the temperature is still very high, it would be better to install another fan inside the case. Using a larger case is recommended if there are a number of add-on cards and disk drives in the system.

CLEANING THE "GOLDEN FINGER"

Whenever inserting an add-on card to the motherboard, make sure that there is no dirt on the "golden finger" of the add-on card. If not, the contact between the "golden finger" and the slot may be poor and thus the add-on card may not work properly. Use a pencil eraser to clean the "golden finger" if dirt is found.

CLEANING THE MOTHERBOARD

The computer system should be kept clean. Dust and dirt are harmful to electronic devices. To prevent dust from accumulating on the mother-board, installing all mounting plates on the rear of the case. Regularly examine your system, and if necessary, vacuum the interior of the system with a miniature vacuum.

Appendix D
Troubleshooting

MAIN MEMORY ERROR

After power up, the monitor remains blank, and there are beep sounds indicating a main memory failure. In this case, turn off the power and remove all SIMM modules. Carefully place the modules back to the sockets and make sure that all the modules are locked by the locking latches firmly.

In some other cases, the total memory found by the BIOS is different from the actual amount of memory on board. (Note that 128K bytes memory is reserved for the shadow RAM function and will not be counted by the BIOS). It is also a memory failure and you can follow the instruction above.

CACHE MEMORY FAILURE

If the system hangs after memory test, it is likely that the cache memory has some problems when the secondary cache memory card is installed. Maybe some of the SRAMs are damaged or the contact of the IC pins is poor. Try to press the SRAM to make sure that the SRAMs are inserted in the sockets, or examine the SRAM to see whether any pins are bent under or out. If the bent pins are found, remove the SRAM, straighten the pin and place the SRAM again. You may also check the BIOS setup of the cache configuration. If the cache controller is enabled, you should select chipset's cache controller. Otherwise, the system will fail.

IMPROPER SETTING OF WAIT STATE

If the system hangs after memory test, another possible cause is the improper setting of the wait state for memory operation. The number of wait state must match the speed of the DRAM. Reset the CMOS RAM and set up the wait state. Try to increase the number of wait state.

Appendix E
System Board Layout

Appendix F
Memory Expansion Card Layout

Appendix G
Hippo Cache Card Layout