VL Slot Configuration

JP39	
Close	VL slot clock greater than 33.333MHz
Open	VL slot clock less than or equal to 33.333MHz

JP40	
Close	1 WS VL-write cycle
Open	0 WS VL-write cycle

CPU Voltage

TYPE	CPUVCC	JP41	JP42	JP43	JP44	JP45	JP46
AUTO	5V/3.45V	OPEN	OPEN	OPEN	OPEN	1-2	OPEN
FIXED	5V	OPEN	OPEN	OPEN	OPEN	OPEN	1-2
FIXED	4V	OPEN	OPEN	OPEN	1-2	OPEN	OPEN
FIXED	3.8V	OPEN	OPEN	1-2	OPEN	OPEN	OPEN
FIXED	3.6V	OPEN	1-2	OPEN	OPEN	OPEN	OPEN
FIXED	3.45V	OPEN	OPEN	OPEN	OPEN	OPEN	OPEN
FIXED	3.3V	1-2	OPEN	OPEN	OPEN	OPEN	OPEN

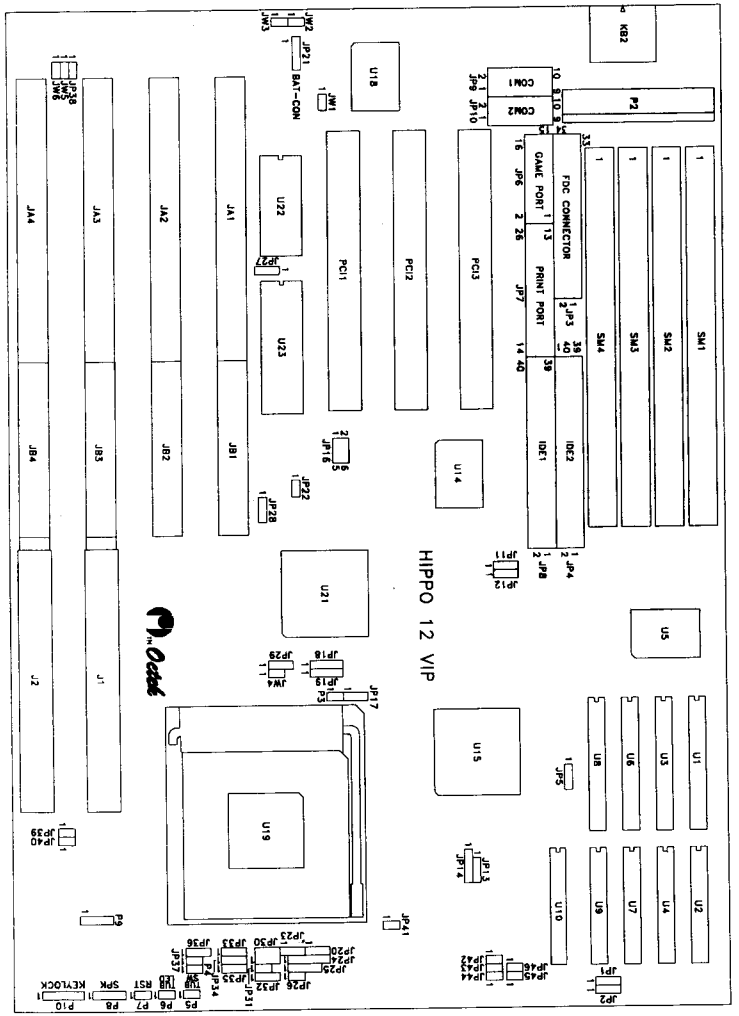
CPU Clock Multiple

JP33	Intel 486DX4 / AMD Enhance 486DX4
Open	CLK 3x
1-2	CLK 2.5x
2-3	CLK 2x

CPU Type

	JP1	JP2	JP18	JP19	JP20	JP24	JP25	JP26	JP30	JP31	JP32	JP34	JP35	JP36	JP37
Intel 486DX/DX2	1-2	1-2	1-2 3-4	3-4	Open	Open	Open	Open	1-2	Open	Open	Open	Open	Open	Open
Intel 486SX	1-2	1-2	2-3	Open	Open	Open	Open	Open	1-2	Open	Open	Open	Open	Open	Open
Intel Pentium Overdrive P24T	1-2	1-2	1-2 3-4	2-3	Open	2-3 4-5	1-2	Open	3-4 5-6	Open	2-3	2-3	1-2	2-3	Open
Cyrix CX486S	2-3	1-2	2-3	Open	Open	1-2 3-4	2-3	Open	3-4	Open	2-3	1-2	2-3	1-2	Open
Cyrix CX486D	2-3	1-2	1-2 3-4	3-4	Open	1-2 3-4	2-3	Open	3-4	Open	2-3	1-2	2-3	1-2	Open
UMC-U5S	1-2	2-3	2-3	1-2 3-4	Open	Open	3-4	Open	1-2	Open	1-2	Open	Open	Open	Open
Intel SL 486SX	1-2	1-2	2-3	Open	Open	2-3 4-5	Open	Open	3-4	Open	2-3	2-3	Open	Open	Open
Intel SL DX / DX2 / DX4	1-2	1-2	1-2 3-4	3-4	Open	2-3 4-5	Open	Open	3-4	Open	2-3	2-3	Open	Open	Open
AM486DXL AM486DX4 UMC-U5DS	1-2	2-3	1-2 3-4	1-2 3-4	Open	Open	3-4	Open	1-2	Open	1-2	Open	Open	Open	Open
AMD Enhance AM486DX2 AM486DX4	1-2	1-2	1-2 3-4	3-4	Open	2-3 4-5	Open	Open	3-4	Open	2-3	2-3	Open	Open	Open
Intel P24D	1-2	1-2	1-2 3-4	3-4	2-3	2-3 4-5	Open	1-2	3-4	1-2	2-3	2-3	Open	Open	1-2
AM486DX2	1-2	2-3	1-2 3-4	1-2 3-4	1-2	Open	3-4	Open	1-2	Open	1-2	Open	Open	Open	Open

Board Layout



System Board Connectors

	Description
P2	Power Connectors
P5	Turbo Switch
P6	Turbo LED Connector
P7	Hardware Reset Switch
P8	Speaker Connector
P9	Hard Disk LED Connector
P10	Power LED and Keylock Connector
JP3	Floppy Drive Connector
JP4	IDE Hard Disk Connector (secondary)
JP6	Game Port Connector
JP7	Parallel Port Connector
JP8	IDE Hard Disk Connector (primary)
JP9	COM 1/3 Serial Port Connectors
JP10	COM 2/4 Serial Port Connector
JP21	External Battery Connector
KB2	Keyboard Connector

Power Saving Features

Whenever the system is not in used (e.g. No key has been hit in the keyboard for a certain period of time), the clock chip of the main board will be signaled to slow down the CPU clock. The system subsequently enters a "sleep" mode. When an external request for system usage is detected (as the pressing of a key or the movement of a mouse), the clock is stepped up to full operating frequency. The time limit for entry to "sleep" mode is selectable in CMOS setup.

IDE drive spin-down is also controllable. The fixed disk will stop spinning after a pre-selected time interval of inactivity.

Reset CMOS Setup Information

Sometimes it may be desirable to clear the existing content of the CMOS RAM. This may be accomplished by allowing the shunt connector to join pin 3 and pin 4 of the header at JP21 for a while. When the system is re-booted, CMOS RAM content is regarded as invalid and the user is prompted to setup the CMOS again. In normal operation, JP21 place (2-3).

P7 Hardware Reset Switch

Pin	Assignment
1	GND
2	Signal pin

P8 Speaker Connector

Pin	Assignment
1	Data out
2	NC
3	Ground
4	+5V

P9 Hard Disk LED Connector

Pin	Assignment
1	+5V
2	Signal pin
3	Signal pin
4	+5V

The External Cache System

An external cache is available to boost the system performance. The external cache is direct-mapped and employs a write-back scheme. The cache sizes are 128K, 256K, 512K.

VESA Local Bus

The Video Electronics Standards Association (VESA) VL Bus is a widely accepted 32-bit local bus standard. It allows devices to be connected CPU local running at CPU clock speed.

Maximum Number of VL-Bus Devices And Slots

The following guidelines are recommended by VESA:

Speed	Max. no. of VL adapter cards installed
33MHz	2
40MHz	2
50MHz	1

PCI Local Bus

The PCI Local Bus is a high performance 32-bit bus with multiplexed address and data line. It is intended for use as interconnect machanism between highly integrated peripheral controller, add-on card and memory system.

Chapter Four
Technical Information

This section provides technical information about Hippo 12 and is particularly useful to advanced users.

Memory Map

Address	Range	Function
0-9FFFFh	0K-640K	Base Memory
A0000-BFFFFh	640K-768K	Video Display Buffer
C0000-DFFFFh	768K-896K	Adapter ROM
E0000-EFFFFh	896K-960K	System ROM (optional)
F0000-FFFFFh	960K-1024K	System ROM
100000-1FFFFFh	1024K-2048K	Extended Memory

The DRAM System

The memory controller supports fast page mode DRAM accesses. This feature is instrumental in sustaining a high memory bandwidth between the DRAM array and the 486 operating in burst mode.

Both normal and hidden refresh are supported. Normal refresh refers to the classical refresh scheme in which the CPU is held while refresh cycles take place in the local DRAM and the ISA bus memory. Hidden refresh scheme allows the CPU to continue executing instructions during DRAM refresh period as long as the CPU does NOT access DRAM or the ISA bus. Refresh overhead is therefore minimized.

Shadow RAM is available as an option. System BIOS and video BIOS residing in slow EPROM can be copied to local DRAM to speed up accesses to BIOS code. Shadow RAM addresses range from C0000h to FFFFFh. 16K granularity is provided for address range C0000h to EFFFFh, while the area F0000h - FFFFFh can only be shadowed as a whole. Video BIOS at C0000h - C7FFFh can be cached in the external cache after shadowing.

System Interrupts

Level	Function
Microprocessor NMI	Parity or I/O Channel Check
Interrupt Controllers	
CTLR 1	CTLR 2
IRQ0	Timer Output 0
IRQ1	Keyboard
IRQ2	
IRQ8	Real-time Clock Interrupt
IRQ9	Software Redirected to INT 0AH (IRQ2)
IRQ10	Reserved
IRQ11	Reserved
IRQ12	Reserved
IRQ13	Coprocessor
IRQ14	Fixed Disk Controller
IRQ15	Reserved
IRQ3	Serial Port 2
IRQ4	Serial Port 1
IRQ5	Parallel Port 2
IRQ6	Diskette Controller
IRQ7	Parallel Port 1

DRAM Configuration: 72 pin SIMM sockets for 1M x 32, 2M x 32, 4M x 32, 8M x32, 16Mx32, or x 36

Cache : 8 KB internal cache in CPU
128K, 256K, 512K secondary cache

On-board I/O Facility:
Floppy controller
2 serial ports
1 parallel port
1 game port

Power Saving Feature: Support SMM for power management
CPU with programmable SMM region

Expansion Slot

VL-slot (side A)

I/O Pin	Signal Name	I/O Pin	Signal Name
A1	D1	A29	A18
A2	D3	A30	A16
A3	GROUND	A31	A14
A4	D5	A32	A12
A5	D7	A33	A10
A6	D9	A34	A8
A7	D11	A35	GROUND
A8	D13	A36	A6
A9	D15	A37	A4
A10	GROUND	A38	WBACK#
A11	D17	A39	BEO#
A12	VCC	A40	VCC
A13	D19	A41	BE1#
A14	D21	A42	BE2#
A15	D23	A43	GROUND
A16	D25	A44	BE3#
A17	GROUND	A45	ADS#
A18	D27	A48	LRDY#
A19	D29	A49	LDEV#
A20	D31	A50	LREQ#
A21	A30	A51	GROUND
A22	A28	A52	LGNT#
A23	A26	A53	VCC
A24	GROUND	A54	ID2
A25	A24	A55	ID3
A26	A22	A56	ID4
A27	VCC	A57	LKEN#
A28	A20	A58	LEADS#

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ISA slot (side A and side B)

I/O Pin	Signal Name	I/O Pin	Signal Name
A1	-I/O CH CK	B1	GND
A2	SD7	B2	RESET DRV
A3	SD6	B3	+5 Vdc
A4	SD5	B4	IRQ9
A5	SD4	B5	-5 Vdc
A6	SD3	B6	DRQ2
A7	SD2	B7	-12 Vdc
A8	SD1	B8	0WS
A9	SD0	B9	+12 Vdc
A10	-I/O CH RDY	B10	GND
A11	AEN	B11	-SMEMW
A12	SA19	B12	-SMEMR
A13	SA18	B13	-IOW
A14	SA17	B14	-IOR
A15	SA16	B15	-DACK3
A16	SA15	B16	DRQ3
A17	SA14	B17	-DACK1
A18	SA13	B18	DRQ1
A19	SA12	B19	-Refresh
A20	SA11	B20	CLK
A21	SA10	B21	IRQ7
A22	SA9	B22	IRQ6
A23	SA8	B23	IRQ5
A24	SA7	B24	IRQ4
A25	SA6	B25	IRQ3
A26	SA5	B26	-DACK2
A27	SA4	B27	T/C
A28	SA3	B28	BALE
A29	SA2	B29	+5 Vdc
A30	SA1	B30	OSC
A31	SA0	B31	GND

The following table summarizes the pin assignments for PCI local bus connector.

PCI Bus Pinout (side A)

I/O Pin	Signal Name	I/O Pin	Signal Name
A1	TRST#	A31	AD[18]
A2	+12V	A32	AD[16]
A3	Reserved	A33	Reserved
A4	Reserved	A34	FRAME#
A5	+5V	A35	Ground
A6	INTA#	A36	TRDY#
A7	INTC#	A37	Ground
A8	+5V	A38	STOP#
A9	Reserved	A39	Reserved
A10	+5V	A40	SDONE
A11	Reserved	A41	SBO#
A12	Ground	A42	Ground
A13	Ground	A43	PAR
A14	Reserved	A44	AD[15]
A15	RST#	A45	Reserved
A16	+5V	A46	AD[13]
A17	GNT#	A47	AD[11]
A18	Ground	A48	Ground
A19	Reserved	A49	AD[09]
A20	AD[30]	A50	C/BE[0]#
A21	Reserved	A51	Reserved
A22	AD[28]	A52	AD[06]
A23	AD[26]	A53	AD[04]
A24	Ground	A54	Ground
A25	AD[24]	A55	AD[02]
A26	IDSEL	A56	AD[00]
A27	Reserved	A57	+5V
A28	AD[22]	A58	REQ64#
A29	AD[20]	A59	+5V
A30	Ground	A60	+5V

RADIO FREQUENCY INTERFERENCE STATEMENT

This equipment generates and uses radio frequency energy and if not installed and used properly, that is, in strict accordance with the manufacturer's instructions, may cause interference with radio and television reception.

If this equipment does cause interference to radio or TV reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

* Reorient the receiving antenna.
* Relocate the computer away from the receiver.
* Move the computer away from the receiver.
* Plug the computer into a different outlet so that computer and receiver are on different branch circuits.
* Ensure that card slot covers are in place when no card is installed.
* Ensure that card mounting screws, attachment connector screws, and ground wires are tightly secured.
* If peripherals are used with this system, it is suggested to use shielded, grounded cables, with in-line filters if necessary.

If necessary, the user should consult the dealer service representative for additional suggestions.

The manufacturer is not responsible for any radio or TV interference caused by unauthorized modifications to this equipment. It is the responsibility of the user to correct such interference.

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PCI Bus Pinout (side B)

I/O Pin	Signal Name	I/O Pin	Signal Name
B1	-12V	B31	Reserved
B2	TCK	B32	AD[17]
B3	Ground	B33	C/BE[2]#
B4	Reserved	B34	Ground
B5	+5V	B35	IRDY#
B6	+5V	B36	Reserved
B7	INTB#	B37	DEVSEL#
B8	INTD#	B38	Ground
B9	PRSNT1#	B39	LOCK#
B10	Reserved	B40	PERR#
B11	PRSNT2#	B41	Reserved
B12	Ground	B42	SERR#
B13	Ground	B43	Reserved
B14	Reserved	B44	C/BE[1]#
B15	Ground	B45	AD[14]
B16	CLK	B46	Ground
B17	Ground	B47	AD[12]
B18	REQ#	B48	AD[10]
B19	+5V	B49	Ground
B20	AD[31]	B50	AD[08]
B21	AD[29]	B51	AD[07]
B22	Ground	B52	Reserved
B23	AD[27]	B53	AD[05]
B24	AD[25]	B54	AD[03]
B25	Reserved	B55	Ground
B26	C/BE[3]#	B56	AD[01]
B27	AD[23]	B57	Reserved
B28	Ground	B58	ACK64#
B29	AD[21]	B59	+5V
B30	AD[19]	B60	+5V

TABLE OF CONTENT

ISA slot (side C and side D)

I/O Pin	Signal Name	I/O Pin	Signal Name
C1	SBHE	D1	-MEM CS16
C2	LA23	D2	-I/O CS16
C3	LA22	D3	IRQ10
C4	LA21	D4	IRQ11
C5	LA20	D5	IRQ12
C6	LA19	D6	IRQ15
C7	LA18	D7	IRQ14
C8	LA17	D8	-DACK0
C9	-MEMR	D9	DRQ0
C10	-MEMW	D10	-DACK5
C11	SD8	D11	DRQ5
C12	SD9	D12	-DACK6
C13	SD10	D13	DRQ6
C14	SD11	D14	-DACK7
C15	SD12	D15	DRQ7
C16	SD13	D16	+5 Vdc
C17	SD14	D17	-MASTER
C18	SD15	D18	GND

Chapter One
Introduction

HIPPO 12 supports advanced local bus architectures : VL-Bus and PCI-Bus, providing flexibility to set up various system configuration for optional performance. Both buses are industrial standards, with support from major PC manufacturers. So there are wide range of choice of peripherals.

OCTEK HIPPO 12 brings the new technology of power saving to desktop computing. Compliance with the EPA requirement, high throughput VESA Local Bus, advanced chipset with power user-programmable features and integrated on-board I/O are some of the real benefits of HIPPO 12.

The key components of the advanced power-saving capabilities are HIPPO 12's built-in support of DPMS functions (Display Power Management Standard) of VESA (Video Electronics Standard Association), support for Windows APM and CPU clock step-down hardware. The energy saving feature of HIPPO 12 is compatible with MS-DOS 5.0 (or later versions) and Windows 3.1.

VL-slot (side B)

I/O Pin	Signal Name	I/O Pin	Signal Name
B1	D0	B29	GROUND
B2	D2	B30	A17
B3	D4	B31	A15
B4	D6	B32	VCC
B5	D8	B33	A13
B6	GROUND	B34	A11
B7	D10	B35	A9
B8	D12	B36	A7
B9	VCC	B37	A5
B10	D14	B38	GROUND
B11	D16	B39	A3
B12	D18	B40	A2
B13	D20	B41	N/C
B14	GROUND	B42	RESET#
B15	D22	B43	D/C#
B16	D24	B44	M/IO#
B17	D26	B45	W/R#
B18	D28	B48	RDYRTN#
B19	D30	B49	GROUND
B20	VCC	B50	IRQ9
B21	A31	B51	BRDY#
B22	GROUND	B52	BLAST#
B23	A29	B53	ID0
B24	A27	B54	ID1
B25	A25	B55	GROUND
B26	A23	B56	VLCLK
B27	A21	B57	VCC
B28	A19	B58	LBS16#

Chapter Two
General Features

Specifications

Processor: 80486DX, 80486DX2, 80486DX4, 486 SL-enhance, UMC P5, CX 486DX, CX 486DX2, 80486SX or 80487SX

Processor Clock: 25 / 33 / 40 / 50 MHz clock selectable

Speed: Turbo/normal speed

Expansion Bus: Three PCI slots
Six 16-bit ISA slots
Two VESA Local Bus slots (supporting Two VL master)

On-board PCI Local Bus Device: PCI-IDE controller

DRAM Upgrade Capacity: 4 MB (min. config.)
256 MB (max. config.)

Direct Memory Access (DMA)

Channel	Function
0	Spare (8 bit transfer)
1	SDLC (8 bit transfer)
2	Floppy Disk (8 bit transfer)
3	Spare (8 bit transfer)
4	Cascade for DMA Controller 1
5	Spare (16 bit transfer)
6	Spare (16 bit transfer)
7	Spare (16 bit transfer)

The 80486 CPU

In simple terms, an 80486 is a combination of a microprocessor (80386), a floating point math coprocessor (80387), a cache controller and 8KB of cache RAM, all in one chip.

The 80486 CPU is binary-compatible with the 8086, 8088 , 80186, 80286, 80386DX and 80386SX CPUs. Software developed for older members of the 80x86 family (such as the 8086 and the 80286) can be run without modification on the 80486. Frequently used instructions can be executed in one clock cycle owing to architectural enhancement:

1. an 8 KB on-chip cache
2. pipelined instruction execution
3. most 486s contain on-chip floating point units

The burst bus interface of the 80486 enables it to attain a transfer rate of 106 MB/sec at 33 MHz CPU clock. Burst cycles are done at the continuous rate of one 32-bit transfer per clock. Another advanced feature is the implementation of the write-buffers. If the bus is currently busy, memory writes are directed to one of the four write-buffers. This write buffering allows the 80486 to continue the next instruction. In summary, the 80486 CPU provides a high performance level and retains compatibility with a large base of existing software.

I/O Address Map

ADDRESS (HEX)	DEVICE
000-01Fh	DMA Controller 1
020-03Fh	Interrupt Controller 1
040-05Fh	Timer
060-06Fh	Keyboard Controller
070-07Fh	Real Time Clock
080-09Fh	DMA Page Register
0A0-0BFh	Interrupt Controller
0C0-0DFh	DMA Controller 2
0F0	Clear Math Coprocessor Busy Flag
0F1	Reset Math Coprocessor
0F8-0FFh	Math Coprocessor Port
170-177h	Fixed Disk (secondary)
1F0-1F7h	Fixed Disk (primary)
200-207h	Game Port
278-27Fh	Parallel Port 2
2E8-2EFh	Serial Port 4
2F8-2FFh	Serial Port 2
300-31Fh	Prototype Card
360-36Fh	Reserved
370-377h	Floppy Disk Controller (secondary)
378-37Fh	Parallel Port 1
380-38Fh	SDLC, bisync 2
3A0-3AFh	Bisync 1
3B0-3BFh	Monochrome Display and Printer Adapter
3C0-3CFh	Reserved
3D0-3DFh	Color Graphics Adapter
3E8-3EFh	Serial Port 3
3F0-3F7h	Floppy Disk Controller (primary)
3F8-3FFh	Serial Port 1

DRAM Configuration

SM1	SM 2	SM 3	SM4	Total
1Mx32				4M
1Mx32	1Mx32			8M
2Mx32				8M
1Mx32	1Mx32	1Mx32		12M
1Mx32	2Mx32			12M
1Mx32	1Mx32	1Mx32	1Mx32	16M
1Mx32	1Mx32	2Mx32		16M
2Mx32	2Mx32			16M
4Mx32				16M
1Mx32	4Mx32			20M
1Mx32	2Mx32	2Mx32		20M
1Mx32	1Mx32	4Mx32		24M
2Mx32	4Mx32			24M
2Mx32	2Mx32	2Mx32		24M
1Mx32	2Mx32	4Mx32		28M
4Mx32	4Mx32			32M
2Mx32	2Mx32	2Mx32	2Mx32	32M
1Mx32	4Mx32	4Mx32		36M
4Mx32	4Mx32	2Mx32		40M
1Mx32	1Mx32	4Mx32	4Mx32	40M
1Mx32	2Mx32	4Mx32	4Mx32	44M
4Mx32	4Mx32	4Mx32		48M
8Mx32	8Mx32			48M
1Mx32	4Mx32	4Mx32	4Mx32	52M
1Mx32	4Mx32	8Mx32		52M
4Mx32	4Mx32	4Mx32	4Mx32	64M
4Mx32	4Mx32	8Mx32		64M
8Mx32	8Mx32			64M
4Mx32	8Mx32	8Mx32		80M
4Mx32	4Mx32	16Mx32		96M
8Mx32	16Mx32			96M
4Mx32	8Mx32	16Mx32		112M
8Mx32	8Mx32	8Mx32	8Mx32	128M
8Mx32	16Mx32	16Mx32		160M
16Mx32	16Mx32	16Mx32	16Mx32	256M

70ns DRAM can be used in all operating frequencies. System BIOS will enable the parity check when 36-bit SIMM modules is inserted.

P10 Power LED & Keylock Connector

Pin	Assignment
1	+5V
2	Key
3	Ground
4	Keyboard inhibit
5	Ground

JP21 External Battery Connector

Pin	Assignment
1	External Battery Input
2	On-board Battery +3.6V
3	On-board Battery Input
4	Ground

The On-board PCI IDE

The PCI Local Bus IDE controller supports enhanced IDE mode 3 features. The IDE controller is fully compatible with ANSI ATA rev 3.x - 4.0 specification for IDE hard disk operations.

The On-board I/O Controller

The on-board I/O controller offers

1. support for two floppy drives (360K 5-¼", 1.2M 5-¼", 720K 3-½ ", 1.44M 3-½ ")
2. one parallel port (SPP)
3. two serial ports
4. game port
5. optional ECP,EPP high performance parallel port

Control Of System Speed

System speed can be controlled by the keyboard and the turbo switch. When the keys "Ctrl", "Alt", "-" are pressed simultaneously, the system switches to low speed. When the keys "Ctrl", "Alt", "+" are pressed at the same time, the system returns to high speed mode (turbo mode).

The header P5 should be connected to the turbo switch of the cabinet. Whenever the system speed is set low by the turbo switch, the key strobes "Ctrl", "Alt", "+" and "Ctrl", "Alt", "-" will have NO impact on the system speed.

P2 Power Connectors

Pin	Assignment
1	**Power Good**
2	+5V
3	+12V
4	-12V
5	Ground
6	Ground

Pin	Assignment
1	Ground
2	Ground
3	-5V
4	+5V
5	+5V
6	+5V

P5 Turbo Switch

Pin	Assignment
1	Signal pin
2	Ground

P6 Turbo LED Connector

Pin	Assignment
1	LED Signal
2	+5V

Chapter Three Installation

Installing DRAM Modules

Follow the steps below to install DRAM SIMMs :

(a) Turn off the PC.
(b) The SIMM RAM is inserted in SIMM socket 1 first. The memory modules should be carefully installed into the SIMM sockets in such a way that the modules are properly oriented and aligned.
(c) Allow the two metal latches at each end of the socket to lock onto the memory module.
(d) Further memory capacity upgrade should be directed to SIMM 2.

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PCI Bus Pinout (side B)

I/O Pin	Signal Name	I/O Pin	Signal Name
B1	-12V	B31	Reserved
B2	TCK	B32	AD[17]
B3	Ground	B33	C/BE[2]#
B4	Reserved	B34	Ground
B5	+5V	B35	IRDY#
B6	+5V	B36	Reserved
B7	INTB#	B37	DEVSEL#
B8	INTD#	B38	Ground
B9	PRSNT1#	B39	LOCK#
B10	Reserved	B40	PERR#
B11	PRSNT2#	B41	Reserved
B12	Ground	B42	SERR#
B13	Ground	B43	Reserved
B14	Reserved	B44	C/BE[1]#
B15	Ground	B45	AD[14]
B16	CLK	B46	Ground
B17	Ground	B47	AD[12]
B18	REQ#	B48	AD[10]
B19	+5V	B49	Ground
B20	AD[31]	B50	AD[08]
B21	AD[29]	B51	AD[07]
B22	Ground	B52	Reserved
B23	AD[27]	B53	AD[05]
B24	AD[25]	B54	AD[03]
B25	Reserved	B55	Ground
B26	C/BE[3]#	B56	AD[01]
B27	AD[23]	B57	Reserved
B28	Ground	B58	ACK64#
B29	AD[21]	B59	+5V
B30	AD[19]	B60	+5V

TABLE OF CONTENT

ISA slot (side C and side D)

I/O Pin	Signal Name	I/O Pin	Signal Name
C1	SBHE	D1	-MEM CS16
C2	LA23	D2	-I/O CS16
C3	LA22	D3	IRQ10
C4	LA21	D4	IRQ11
C5	LA20	D5	IRQ12
C6	LA19	D6	IRQ15
C7	LA18	D7	IRQ14
C8	LA17	D8	-DACK0
C9	-MEMR	D9	DRQ0
C10	-MEMW	D10	-DACK5
C11	SD8	D11	DRQ5
C12	SD9	D12	-DACK6
C13	SD10	D13	DRQ6
C14	SD11	D14	-DACK7
C15	SD12	D15	DRQ7
C16	SD13	D16	+5 Vdc
C17	SD14	D17	-MASTER
C18	SD15	D18	GND

Chapter One
Introduction

HIPPO 12 supports advanced local bus architectures : VL-Bus and PCI-Bus, providing flexibility to set up various system configuration for optional performance. Both buses are industrial standards, with support from major PC manufacturers. So there are wide range of choice of peripherals.

OCTEK HIPPO 12 brings the new technology of power saving to desktop computing. Compliance with the EPA requirement, high throughput VESA Local Bus, advanced chipset with power user-programmable features and integrated on-board I/O are some of the real benefits of HIPPO 12.

The key components of the advanced power-saving capabilities are HIPPO 12's built-in support of DPMS functions (Display Power Management Standard) of VESA (Video Electronics Standard Association), support for Windows APM and CPU clock step-down hardware. The energy saving feature of HIPPO 12 is compatible with MS-DOS 5.0 (or later versions) and Windows 3.1.

VL-slot (side B)

I/O Pin	Signal Name	I/O Pin	Signal Name
B1	D0	B29	GROUND
B2	D2	B30	A17
B3	D4	B31	A15
B4	D6	B32	VCC
B5	D8	B33	A13
B6	GROUND	B34	A11
B7	D10	B35	A9
B8	D12	B36	A7
B9	VCC	B37	A5
B10	D14	B38	GROUND
B11	D16	B39	A3
B12	D18	B40	A2
B13	D20	B41	N/C
B14	GROUND	B42	RESET#
B15	D22	B43	D/C#
B16	D24	B44	M/IO#
B17	D26	B45	W/R#
B18	D28	B48	RDYRTN#
B19	D30	B49	GROUND
B20	VCC	B50	IRQ9
B21	A31	B51	BRDY#
B22	GROUND	B52	BLAST#
B23	A29	B53	ID0
B24	A27	B54	ID1
B25	A25	B55	GROUND
B26	A23	B56	VLCLK
B27	A21	B57	VCC
B28	A19	B58	LBS16#

Chapter Two
General Features

Specifications

Processor: 80486DX, 80486DX2, 80486DX4, 486 SL-enhance, UMC P5, CX 486DX, CX 486DX2, 80486SX or 80487SX

Processor Clock: 25 / 33 / 40 / 50 MHz clock selectable

Speed: Turbo/normal speed

Expansion Bus: Three PCI slots
Six 16-bit ISA slots
Two VESA Local Bus slots (supporting Two VL master)

On-board PCI Local Bus Device: PCI-IDE controller

DRAM Upgrade Capacity: 4 MB (min. config.)
256 MB (max. config.)

Direct Memory Access (DMA)

Channel	Function
0	Spare (8 bit transfer)
1	SDLC (8 bit transfer)
2	Floppy Disk (8 bit transfer)
3	Spare (8 bit transfer)
4	Cascade for DMA Controller 1
5	Spare (16 bit transfer)
6	Spare (16 bit transfer)
7	Spare (16 bit transfer)

The 80486 CPU

In simple terms, an 80486 is a combination of a microprocessor (80386), a floating point math coprocessor (80387), a cache controller and 8KB of cache RAM, all in one chip.

The 80486 CPU is binary-compatible with the 8086, 8088 , 80186, 80286, 80386DX and 80386SX CPUs. Software developed for older members of the 80x86 family (such as the 8086 and the 80286) can be run without modification on the 80486. Frequently used instructions can be executed in one clock cycle owing to architectural enhancement:

1. an 8 KB on-chip cache
2. pipelined instruction execution
3. most 486s contain on-chip floating point units

The burst bus interface of the 80486 enables it to attain a transfer rate of 106 MB/sec at 33 MHz CPU clock. Burst cycles are done at the continuous rate of one 32-bit transfer per clock. Another advanced feature is the implementation of the write-buffers. If the bus is currently busy, memory writes are directed to one of the four write-buffers. This write buffering allows the 80486 to continue the next instruction. In summary, the 80486 CPU provides a high performance level and retains compatibility with a large base of existing software.

I/O Address Map

ADDRESS (HEX)	DEVICE
000-01Fh	DMA Controller 1
020-03Fh	Interrupt Controller 1
040-05Fh	Timer
060-06Fh	Keyboard Controller
070-07Fh	Real Time Clock
080-09Fh	DMA Page Register
0A0-0BFh	Interrupt Controller
0C0-0DFh	DMA Controller 2
0F0	Clear Math Coprocessor Busy Flag
0F1	Reset Math Coprocessor
0F8-0FFh	Math Coprocessor Port
170-177h	Fixed Disk (secondary)
1F0-1F7h	Fixed Disk (primary)
200-207h	Game Port
278-27Fh	Parallel Port 2
2E8-2EFh	Serial Port 4
2F8-2FFh	Serial Port 2
300-31Fh	Prototype Card
360-36Fh	Reserved
370-377h	Floppy Disk Controller (secondary)
378-37Fh	Parallel Port 1
380-38Fh	SDLC, bisync 2
3A0-3AFh	Bisync 1
3B0-3BFh	Monochrome Display and Printer Adapter
3C0-3CFh	Reserved
3D0-3DFh	Color Graphics Adapter
3E8-3EFh	Serial Port 3
3F0-3F7h	Floppy Disk Controller (primary)
3F8-3FFh	Serial Port 1

DRAM Configuration

SM1	SM 2	SM 3	SM4	Total
1Mx32				4M
1Mx32	1Mx32			8M
2Mx32				8M
1Mx32	1Mx32	1Mx32		12M
1Mx32	2Mx32			12M
1Mx32	1Mx32	1Mx32	1Mx32	16M
1Mx32	1Mx32	2Mx32		16M
2Mx32	2Mx32			16M
4Mx32				16M
1Mx32	4Mx32			20M
1Mx32	2Mx32	2Mx32		20M
1Mx32	1Mx32	4Mx32		24M
2Mx32	4Mx32			24M
2Mx32	2Mx32	2Mx32		24M
1Mx32	2Mx32	4Mx32		28M
4Mx32	4Mx32			32M
2Mx32	2Mx32	2Mx32	2Mx32	32M
1Mx32	4Mx32	4Mx32		36M
4Mx32	4Mx32	2Mx32		40M
1Mx32	1Mx32	4Mx32	4Mx32	40M
1Mx32	2Mx32	4Mx32	4Mx32	44M
4Mx32	4Mx32	4Mx32		48M
8Mx32	8Mx32			48M
1Mx32	4Mx32	4Mx32	4Mx32	52M
1Mx32	4Mx32	8Mx32		52M
4Mx32	4Mx32	4Mx32	4Mx32	64M
4Mx32	4Mx32	8Mx32		64M
8Mx32	8Mx32			64M
4Mx32	8Mx32	8Mx32		80M
4Mx32	4Mx32	16Mx32		96M
8Mx32	16Mx32			96M
4Mx32	8Mx32	16Mx32		112M
8Mx32	8Mx32	8Mx32	8Mx32	128M
8Mx32	16Mx32	16Mx32		160M
16Mx32	16Mx32	16Mx32	16Mx32	256M

70ns DRAM can be used in all operating frequencies. System BIOS will enable the parity check when 36-bit SIMM modules is inserted.

P10 Power LED & Keylock Connector

Pin	Assignment
1	+5V
2	Key
3	Ground
4	Keyboard inhibit
5	Ground

JP21 External Battery Connector

Pin	Assignment
1	External Battery Input
2	On-board Battery +3.6V
3	On-board Battery Input
4	Ground

The On-board PCI IDE

The PCI Local Bus IDE controller supports enhanced IDE mode 3 features. The IDE controller is fully compatible with ANSI ATA rev 3.x - 4.0 specification for IDE hard disk operations.

The On-board I/O Controller

The on-board I/O controller offers

1. support for two floppy drives (360K 5-¼", 1.2M 5-¼", 720K 3-½ ", 1.44M 3-½ ")
2. one parallel port (SPP)
3. two serial ports
4. game port
5. optional ECP,EPP high performance parallel port

Control Of System Speed

System speed can be controlled by the keyboard and the turbo switch. When the keys "Ctrl", "Alt", "-" are pressed simultaneously, the system switches to low speed. When the keys "Ctrl", "Alt", "+" are pressed at the same time, the system returns to high speed mode (turbo mode).

The header P5 should be connected to the turbo switch of the cabinet. Whenever the system speed is set low by the turbo switch, the key strobes "Ctrl", "Alt", "+" and "Ctrl", "Alt", "-" will have NO impact on the system speed.

P2 Power Connectors

Pin	Assignment
1	**Power Good**
2	+5V
3	+12V
4	-12V
5	Ground
6	Ground

Pin	Assignment
1	Ground
2	Ground
3	-5V
4	+5V
5	+5V
6	+5V

P5 Turbo Switch

Pin	Assignment
1	Signal pin
2	Ground

P6 Turbo LED Connector

Pin	Assignment
1	LED Signal
2	+5V

Chapter Three Installation

Installing DRAM Modules

Follow the steps below to install DRAM SIMMs :

(a) Turn off the PC.
(b) The SIMM RAM is inserted in SIMM socket 1 first. The memory modules should be carefully installed into the SIMM sockets in such a way that the modules are properly oriented and aligned.
(c) Allow the two metal latches at each end of the socket to lock onto the memory module.
(d) Further memory capacity upgrade should be directed to SIMM 2.

Reserved Jumpers

JP12	2-3
JP13	1-2
JP17	1-2
JP22	1-2
JP23	2-3
JP27	2-3
JP28	Open
JP29	Open
JP38	2-3
JW1	1-2
JW2	Open
JW3	Open
JW4	1-2
JW5	1-2
JW6	1-2
P3	Open

Jumper Setting

Cache Configuration

For 33MHz clock, the tag RAM 32Kx8 is used 20ns and 40MHz or 50MHz system, 15ns RAM is used (U10).

	512K (128Kx8) U1, U3, U6, U8	256K (32Kx8) U1-U4, U6-U9	256K (64Kx8) U1, U3, U6, U8	128K (32Kx8) U1, U3, U6, U8
JP5	2-3	1-2	2-3	2-3
JP14	1-2, 3-4	1-2	1-2	OPEN

Clock Selection

JP16	Clock Rate	CPU Speed
1-2	50MHz	DX50
1-2, 3-4, 5-6	33MHz	DX33, DX2-66,DX4-100
3-4, 5-6	40MHz	DX40, DX2-80
5-6	25MHz	DX25, DX2-50

On-board IDE

JP11	IDE
1-2	enabled
2-3	disabled

Reserved Jumpers

JP12	2-3
JP13	1-2
JP17	1-2
JP22	1-2
JP23	2-3
JP27	2-3
JP28	Open
JP29	Open
JP38	2-3
JW1	1-2
JW2	Open
JW3	Open
JW4	1-2
JW5	1-2
JW6	1-2
P3	Open

Jumper Setting

Cache Configuration

For 33MHz clock, the tag RAM 32Kx8 is used 20ns and 40MHz or 50MHz system, 15ns RAM is used (U10).

	512K (128Kx8) U1, U3, U6, U8	256K (32Kx8) U1-U4, U6-U9	256K (64Kx8) U1, U3, U6, U8	128K (32Kx8) U1, U3, U6, U8
JP5	2-3	1-2	2-3	2-3
JP14	1-2, 3-4	1-2	1-2	OPEN

Clock Selection

JP16	Clock Rate	CPU Speed
1-2	50MHz	DX50
1-2, 3-4, 5-6	33MHz	DX33, DX2-66,DX4-100
3-4, 5-6	40MHz	DX40, DX2-80
5-6	25MHz	DX25, DX2-50

On-board IDE

JP11	IDE
1-2	enabled
2-3	disabled