GMB-386SOP

80386SX Mainboard

User's Guide

ABOUT THIS GUIDE

This guide contains instructions for configuring and installing the GMB-386SOP mainboard.

- Chapter 1, **Introduction**, acquaints user with the special features of the GMB-386SOP mainboard.
- Chapter 2, **Hardware Configuration**, gives information on configuring memory and setting the mainboard's jumpers. Brief sections on installing memory and a math coprocessor are also included.
- Chapter 3, **Mainboard Installation**, is an overview of how to install the mainboard in a system.
- Chapter 4, **Technical Reference**, offers technical information of the mainboard.
- Finally, a **Quick Reference Table**.

TRADEMARKS USED IN THIS MANUAL

MS-DOS, XENIX, Microsoft, WINDOWS are trademarks of Microsoft Corp.

NOVELL, Netware are trademarks of Novell, Inc.

Wordstar is a trademark of MicroPro International.

Lotus 1-2-3 is a trademark of Lotus Development Corp.

AT is a trademark of International Business Machines Corp.

OS/2 is a trademark of Microsoft Corp. and International Business Machines Corp.

UNIX is the trademark of AT&T.

Weitek is a trademark of Weitek Corp.

The information presented in this publication has been carefully checked for reliability; however, no responsibility is assumed for inaccuracies, whereas, specification is subjected to change without notice.

UNPACKING THE MAINBOARD

The GMB-386SOP Mainboard comes packed in a sturdy cardboard shipping carton. The carton contains:

- The GMB-386SOP Mainboard
- This User's Guide
- BIOS User's Guide

Note: Do not remove the mainboard from its original packing until ready to install.

The GMB-386SOP mainboard is easily damaged by static electricity. Observe the following precautions while unpacking and installing the mainboard.

1. Touch an unpainted area of the system chassis before handling the mainboard or any component. Doing so, discharges the static charge the user's body may have built.

2. Remove the mainboard from its anti-static wrapping and place it on a grounded surface, component side up.

3. Inspect the mainboard for damage. Shipping may have loosened integrated circuits from their sockets. If any integrated circuit appears loose, press carefully to seat it firmly in this socket.

Do not apply power if the mainboard appears damaged. If there is damage to the board, or items are missing, contact dealer immediately.

STATIC ELECTRICITY PRECAUTIONS

Static electricity can easily damage the GMB-386SOP mainboard. Observing a few basic precautions can help safeguard against damage that could result in experience repairs. Follow the measures below to protect the equipment from static discharge:

- Keep the mainboard and other system components in their anti-static packaging until ready to install.
- Touch a grounded surface before removing any system component from its protective anti-static packaging. A grounded surface within easy reach is the expansion slot covers at the rear of the system case, or any other unpainted portion of the system chassis.
- During configuration and installation, touch a grounded surface frequently to discharge any static electric charge that may build up in the body. Another option is to wear a grounding wrist strap.
- When handling a mainboard or an adapter card, avoid touching its components. Handle the mainboard and adapter cards either by the edges or by the mounting bracket that attaches to the slot opening in the case.

CONTENTS

CHAPTER 1 INTRODUCTION

The GMB-386SOP mainboard is a 1/2 body AT size high-performance mainboard that provides with the basic elements on which to build an advanced computer. This mainboard is fully IBM AT compatible, but has the added enhancement of a powerful 32-bit microprocessor.

The GMB-386SOP mainboard is configured with one of two microprocessors:

- AMD 386SX CPU running at 33, or 40MHz.
- Cyrix CX486SLC CPU running at 25, or 33MHz.

The GMB-386SOP mainboard features on-board cache capability. Cache memory accelerates system performance by storing the most recently used instructions and data in a small amount of high-speed memory. The GMB-386SOP mainboard's cache significantly accelerate the speed of the user's programs.

The GMB-386SOP mainboard was developed around a microprocessor with 32-bit internal access to data, and a high performance single chip core logic with Internal Cache Controller.

1.1 KEY FEATURES

The advanced features of the GMB-386SOP mainboard include:

- 100% IBM PC-AT Compatible SX Chipset.
- Support AMD 386SX and Cyrix CX486SLC microprocessors.
- Two chip PC/AT solution: one 160 pin CMOS Plastic Flat Package (PFP) and one 100-pin PQFP.
- Supports systems running from 25-40 MHz.

- Write-back direct-mapped cache with programmable size selections: 16K, 32K, 64K, 128K.
- Supports two banks of 256K, 1M, and 4M page-mode local DRAMs for configurations up to 16MB.
- 640KB - 1MB non cacheable regions.
- All memory access non cacheable.
- Programmable cache and DRAM read/write cycles.
- Shadow RAM option for system and channel ROM BIOS.
- Turbo/slow speed selection.
- Synchronous AT Bus Clock with programmable clock division options: CLK2/4,6,8,10.
- 0 or 1 wait state options for 16-bit AT bus cycles.
- Transparent 8042 emulation for fast CPU reset and GATEA20 generation.
- Supports the 80387SL Numerics Coprocessor.
- Option for write protected, cacheable video BIOS.
- Flash ROM support.
- Support 7 Direct Memory Access channels.
- Support 16 Interrupt levels.
- Battery-backed CMOS memory for real time clock and system configuration.
- User Defined Password to inhibit illegal access.

1.2 MAINBOARD COMPONENTS

This section gives a brief description of key components on the mainboard. Refer to Fig 1 for component locations.

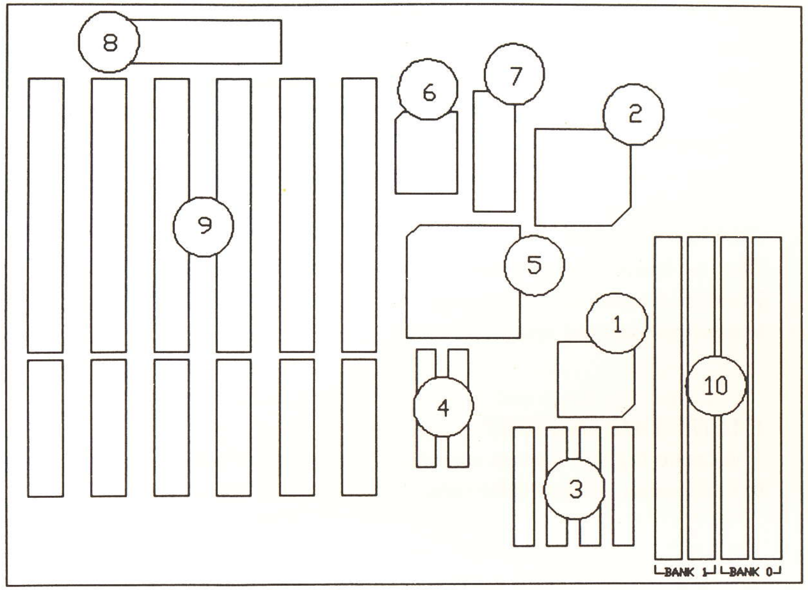


Fig 1 Key Components of the GMB-386SOP Mainboard

(1). *SYSTEM MICROPROCESSOR*
The system microprocessor is a high-performance 32-bit microprocessor. The microprocessor on the mainboard is available in the clock speed of 25, 33, or 40MHz.

(2). *MATH COPROCESSOR SOCKET*
This socket will let the user add an optional 80387SL math coprocessor. Adding a numeric coprocessor to the mainboard significantly increases the speed of calculation intensive applications such as spreadsheet, databases, and graphics programs.

(3). *CACHE MEMORY*
The on-board cache memory consists of four pieces of SRAM (Static Random Access Memory) chips (either 4Kx4, 8Kx4, 16Kx4, or 32Xx4) that contain the cached code and data.

(4). *CACHE TAG MEMORY*
The cache tag sub-system consists of one piece of SRAM chips that register the addresses of the cache data.

(5). *SINGLE CHIP CORE LOGIC*
This is a highly integrated single chip core logic for the system, which includes:

- **Integrated cache controller supports:**
  Direct-mapped caching scheme.
  Built-in internal comparator.
  Optional write-back or write-through cache update algorithm.
  Either one or two banks of SRAM.
  16KB, 32KB, 64KB, 128KB cache size.
  Programmable zero or one wait state for read cycle.
  Programmable zero, one or two wait state for write cycle.
  Two cacheable blocks ranging from 128K to 1MB.
  Optional caching of shadowed video BIOS.

- **Integrated DRAM controller supports:**
  Page mode 256KB, 1MB, 4MB DRAM.
  System memory size ranging from 1MB up to 16MB.
  Parity generation and detection.
  C/D/E/F block shadow RAM.
  Programmable zero, one or two wait state for read/write cycles.
  Hidden DRAM refresh.
  CAS before RAS refresh that reduces power consumption.

- **Integrated AT bus controller supports:**
  Arbitration between CPU, refresh, and DMA.
  Data bus conversion between local bus, memory bus, and system bus.
  Hidden AT refresh.
  Optional one level deep AT buffer write.
  Additional wait state option for AT bus cycle.
  Optional one or two AT bus clocks for back-to-back I/O cycle recovery time.
  Synchronous/Asynchronous AT bus clock generation.

(6). *OPTI 82C206 INTEGRATED PERIPHERALS CONTROLLER (IPC)*
The 82C206 integrated peripherals controller provide all of the standard peripherals required for system board implementation except the keyboard interface controller. The 82C206 offers 7 DMA channels, 13 interrupt request channels, 2 timer/counter channels, and a real-time clock.

(7). *SYSTEM BIOS*
The BIOS lets the user control the mainboard's microprocessor speed, shadow RAM and cache functions from the keyboard.

(8). *KEYBOARD CONTROLLER*
The 8042 is a single chip keyboard interface controller.

(9). *EXPANSION SLOTS*
Six 16-bit expansion slots are provided on the mainboard.

(10). *MAIN MEMORY*
Four SIMM (Single In-line Memory Module) sockets are provided for 256K, 1MB, and 4MB SIMM modules. Memory can be configured for 1MB, 2MB, 4MB, 8MB, 10MB, and 16MB.

1.3 CACHE OVERVIEW

The special feature of the GMB-386SOP mainboard is a built-in direct-mapped cache controller with write-back operation which supports 16KB, 32KB, 64KB, or 128KB cache memory.

The cache capabilities for the GMB-386SOP mainboard significantly improve the performance of the software applications. Cache works by copying most recently accessed data and placing it in an area of high speed memory called SRAM. Cache SRAM is positioned between main memory DRAM and the CPU. Data is transferred from DRAM to SRAM and then from SRAM to the CPU. The CPU then accesses data in and out of the SRAM at a very high speed, allowing the application to run much faster.

Since most program executions are sequential and repetitive, it is highly possible that the CPU will find data already stored in cache. If the data is already in cache, a cache hit results. If the CPU must go to main memory DRAM or hard disk to access the data, then a cache miss occurs.

The GMB-386SOP mainboard's built-in cache controller offers several features that increase system performance during cache hit and cache miss cycle. A Page DRAM memory enhances performance during read miss cycles. It also allows Refresh and cache hit cycles to occur together without holding the CPU during Refresh cycles.

CHAPTER 2 HARDWARE CONFIGURATION

Before installing the GMB-386SOP mainboard into the system chassis, user may find it convenient to first configure the mainboard's hardware. This chapter describes how to set the mainboard jumpers for cache memory and display type, and how to install Math Coprocessor, memory modules.

2.1 POWER PRECAUTIONS

Before beginning the configuration, user must be sure to work with an unplugged mainboard. Many components are powered by low-voltage current, but there still may be a dangerous electric current coming from the leads and power supply. User should take the following precautions:

- Turn off the power supply, and unplug the power cord before begin.
- Unplug all cables that connect the mainboard to any external devices.

2.2 JUMPER SETTINGS

Configure the hardware options by setting jumper switches on the mainboard. Jumper switches are rows of small pins on the mainboard that can be set by using a jumper cap.

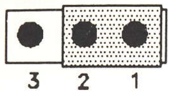
Set a jumper switch as follows:

- Short a jumper by placing the plastic jumper cap over two pins of the jumper switch.
- Open a jumper switch by removing the jumper cap.

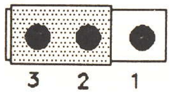
Note: *When opening a jumper, attach the plastic jumper cap to one of the pins so it will not be lost.*

Symbols:

For setting Multi-pin jumpers, the symbols below are used:

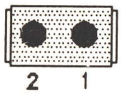


Pins 1 and 2 are Shorted with a jumper cap.

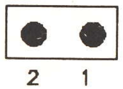


Pins 2 and 3 are Shorted with a jumper cap.

For setting 2-pin jumpers, the following symbols are used:



The jumper is Shorted when the jumper cap is placed over the two pins of the jumper.



The jumper is Open when the jumper cap is removed from the jumper.

2.3 JUMPER AND MEMORY BANK LOCATIONS

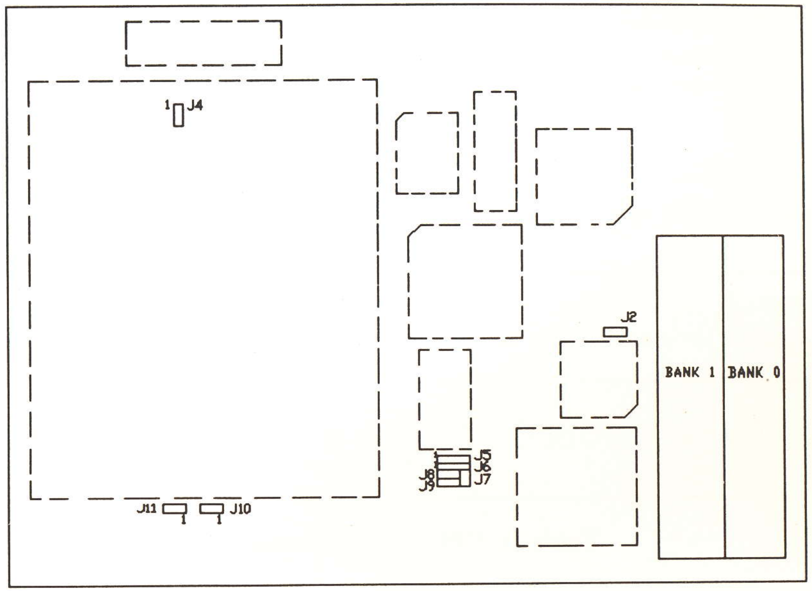


Fig 2 Jumper and Memory Bank Locations

2.4 CPU JUMPER SETTING

The GMB-386SOP mainboard can support the microprocessor at 25, 33 or 40MHz. Jumpers J2 and J11 are required to setup for installing various CPU. Refer to Fig 2 for the location of J2 and J11. Set the jumpers according to the following table:

J2, J11 -- CPU Jumper

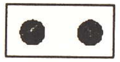
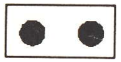
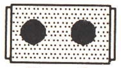
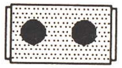
CPU	J2	J11
AMD 386SX	 2 1	 2 1
Cyrix 486SLC	 2 1	 2 1

Table 1: CPU Jumper Setting

2.5 MATH COPROCESSOR INSTALLATION

The GMB-386SOP mainboard has a 68-pin PLCC socket that supports an 80387SL math coprocessor. See Fig 1 in Chapter 1 for the socket's location.

2.5.1 INSTALLING AN 80387SL MATH COPROCESSOR

Install an 80387SL math coprocessor as follows:
Caution: *Static electricity can damage a math coprocessor.*

1. Make sure that power to the mainboard is off and review the section on static electricity precautions at the beginning of this manual.

2. Align the coprocessor so that the notched corner of the chip matches the notched corner of the socket. The notched corner of the chip is marked by a round dot.

3. Align the pins with the second row of socket holes. The 80387SL coprocessor is correctly aligned if an empty row of socket holes appears around the chip.

4. Carefully press the chip into the socket.

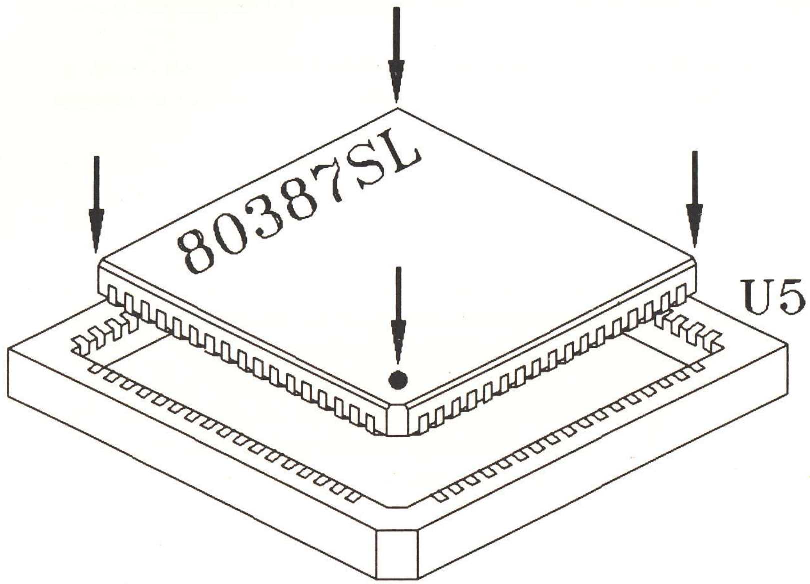


Fig 3 Installing an 80387SL Coprocessor

2.6 CACHE CONFIGURATION

The GMB-386SOP mainboard has a built-in cache controller. It requires external SRAM as tag and cache memory. The caching Scheme is direct mapping with write-back operation. The mainboard allows 16KB, 32KB, 64KB, and 128KB cache configurations. Memory size is selected by the hardware jumpers and the BIOS setup program.

2.6.1 UPGRADING CACHE

The GMB-386SOP mainboard is available with an optional 16KB, 32KB, 64KB, or 128KB cache memory on-board. User can upgrade cache memory by installing additional SRAM (Static Random Access Memory) chips in sockets U19, U20, U21, and U23.

The speed of the SRAM chips needed depends on the clock speed of the microprocessor:

25MHz CPU requires **20ns (tag)** and **35ns (data)** SRAM chips for SRAM interleaved.
33MHz CPU requires **15ns (tag)** and **25ns (data)** SRAM chips for SRAM interleaved.
40MHz CPU requires **15ns (tag)** and **20ns (data)** SRAM chips for SRAM interleaved.

2.6.2 CACHE SIZE AND MEMORY LOCATIONS

The table below describes the chip capacity and socket location required for each cache size configuration. User can use 8K x 8-bit or 32K x 8-bit SRAM chips in banks 0 and 1, and in the Tag RAM sockets. Please note that, do not combine different chip capacities in banks 0 and 1.

	Cache RAM				**Tag RAM**	
Cache Size	U19	U20	U21	U23	U26	U27
16K	8Kx8	Empty	8Kx8	Empty	8Kx8	Empty
32K	8Kx8	8Kx8	8Kx8	8Kx8	8Kx8	Empty
64K	32Kx8	Empty	32Kx8	Empty	8Kx8	Empty
128K	32Kx8	32Kx8	32Kx8	32Kx8	8Kx8	8Kx8

Table 2: Cache Size Configuration

2.6.3 CACHE CHIP SOCKETS AND JUMPER LOCATIONS

The diagram below describes the location of the cache chip sockets and cache jumpers.

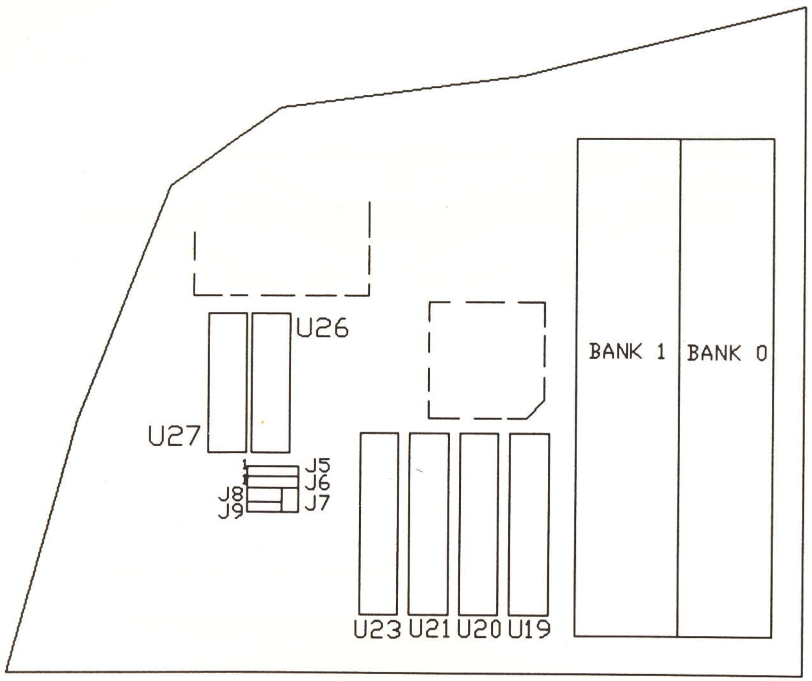


Fig 4 Cache Jumper and Socket Locations

2.6.4 CACHE JUMPER SETTING

Cache memory is configured using jumpers, J5 - J10. The following table summarize the possible configuration.

	Cache Size			
Jumper	16K	32K	64K	128K
J5	2-3	2-3	1-2	1-2
J6	2-3	2-3	2-3	1-2
J7	OPEN	OPEN	OPEN	CLOSE
J8	OPEN	OPEN	CLOSE	CLOSE
J9	OPEN	CLOSE	CLOSE	CLOSE
J10	OPEN	OPEN	OPEN	CLOSE

Table 3: Cache Jumper Setting

2.6.5 INSTALLING CACHE CHIPS

Install cache chips on the mainboard as follows:

Caution: *Static electricity can damage a cache chip.*

1. Review the section on static electricity precautions at the beginning of this manual, and make sure that power to the mainboard is off.
2. Align the chip so that the notched corner of the chip matches the notched corner of the socket.

3. Align the pins with the socket holes.
4. Carefully press the chip into the socket.

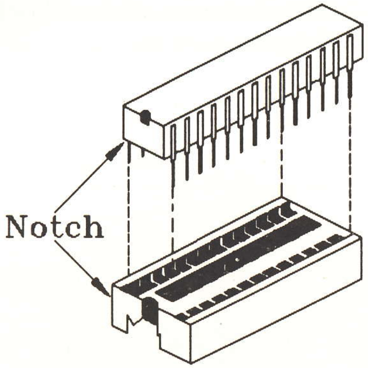


Fig 5 Installing a Cache Chip

2.7 DISPLAY ADAPTER SETUP

Set the jumper, J4, to configure the mainboard for either a color display card or a monochrome display card. Short the jumper for a color display adapter. Open the jumper for a monochrome display adapter. Refer to Fig 2 for the location of J4. Set the jumper as below.

J4 -- Display Adapter Type

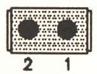
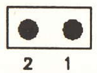
Display Adapter	J4
Color Display (Default)	
Mono Display	

Table 4: Dispaly Adapter Type

2.8 MEMORY INSTALLATION

The GMB-386SOP lets user add system memory via SIMM sockets on the mainboard. On-board memory is located in two banks: Bank 0 and Bank 1. See Fig 2.

Two SIMM sockets are provided in each bank. User can install either a 256K, 1M, or 4M SIMM in each socket. Note that all SIMM modules in a bank must be the same capacity.

SIMM speed required for best performance depends on the CPU speed, which requires 70ns SIMM.

The mainboard supports the following configurations:

Bank 0	Bank 1	Memory Size
256K	256K	1MB
1M	NONE	2MB
1M	1M	4MB
4M	NONE	8MB
1M	4M	10MB
4M	4M	16MB

Table 5: On-board Memory Configuration

2.11.1 INSTALLING SIMM

Install a SIMM in a memory socket as follows:

Caution: *Static electricity can seriously damage SIMM modules.*

1. Review the section on static electricity precautions at the beginning of this manual.

2. Align the SIMM module so that the pin-1 marking on the module corresponds to the socket pin-1 marking.

3. Hold the module at a 70-degree angle to the socket, and insert the module's connectors into the socket.

4. Snap the module to a vertical position in the socket. The module is fully inserted when retaining pegs snap into holes at each end of the module.

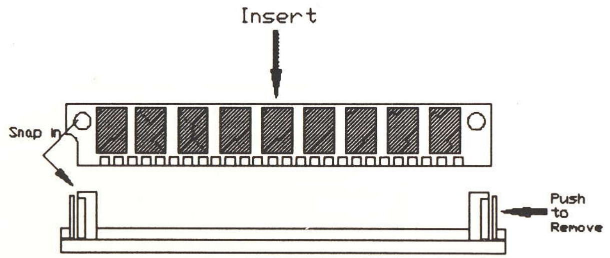


Fig 6 Installing a SIMM

5. To fill a bank, repeat steps 1 through 4 until the sockets in each bank contain SIMMs.

6. After installing memory, run BIOS Setup to indicate to the system for how much memory the user has installed.

CHAPTER 3 MAINBOARD INSTALLATION

Once the GMB-386SOP mainboard's hardware has been configured, the user is now ready to install the mainboard into the system chassis. This chapter describes what are needed to assemble an advanced computer system based on the GMB-386SOP mainboard.

3.1 WHAT ARE NEEDED

The following components and tools are the minimum required to build a working computer system.

3.1.1 COMPONENTS

The following components are recommended:

- Case with standard chassis and hardware. The GMB-386SOP fits most AT compatible cases.
- Standard AT power supply.
- 8 ohm speaker.
- Floppy disk drive(s) (360KB, 1.2MB, or 1.44MB).
- Hard disk drive (optional).
- Hard disk and floppy disk drive controller card.
- Flat ribbon cables to connect the disk drive controller and the disk drive(s).
- Serial/parallel interface card.
- AT-compatible keyboard.
- Video card and Display (monochrome, CGA, EGA, or VGA).

3.1.2 TOOLS

Installing the GMB-386SOP mainboard requires the following tools:

- 1/4" Nutdriver
- 3/16" Nutdriver

User can also use a Philips screwdriver with a 6" shaft and a flat blade screwdriver instead of the nutdrivers.

3.2 POWER SUPPLY REQUIREMENTS

Need a clean, steady power source to get the best performance from the system. For reliable performance, make sure the power supply provides a voltage range of 5.25 volts maximum to 4.75 volts minimum. If the area has noisy power transmission, use a line noise filter between the power source and the computer.

User must make sure the power supply can supply the total power required by all the devices in the system. Check the power requirements of the floppy disk drives, hard disk drives, and any additional boards that will use. In a system that includes a hard disk drive and installed adapter cards, use a power supply of at least 200 watts.

3.3 INSTALLING THE MAINBOARD

Before starting, check the location of the mounting holes in the case and on the mainboard.

Caution: *Static electricity can damage the mainboard.*

Install the GMB-386SOP mainboard as follows:

1. Review the section on static electricity precautions at the beginning of this manual.

2. Place the case on an anti-static mat and remove the cover. Remove the nylon stand-offs and screws for mounting the mainboard.
3. Put the front of the case to the right and the rear to the left. The mainboard occupies the section of the case nearest the user; the power supply goes on the far side.
4. Align the mounting holes on the case to the mounting holes on the mainboard. Make sure to access the keyboard connector (J1) once the board is installed.
5. From the bottom of the mainboard, insert stand-offs into the proper holes on the board, and attach the mounting screws to the bottom of the case.

Note: *Some cases do not use stand-offs and mounting screws; in this case user can fasten the mainboard into the case with regular screws.*

6. Place the mainboard into the case and fasten the board securely with regular screws.

3.4 CONNECTION THE MAINBOARD

Once the mainboard has been fastened into the system case, the next step is to connect the internal cables. The internal cables are wire leads with plastic female connectors that attach to the connectors. The mainboard connectors have varying numbers of pins and are the points of contact between the mainboard and other parts of the computer.

A description of each connector and its connector pins follows. See Fig 7 for the location of the connectors on the mainboard.

Note: *Before making connectors on the board, make sure that power to the system is turned off.*

3.4.1 CONNECTION LOCATIONS

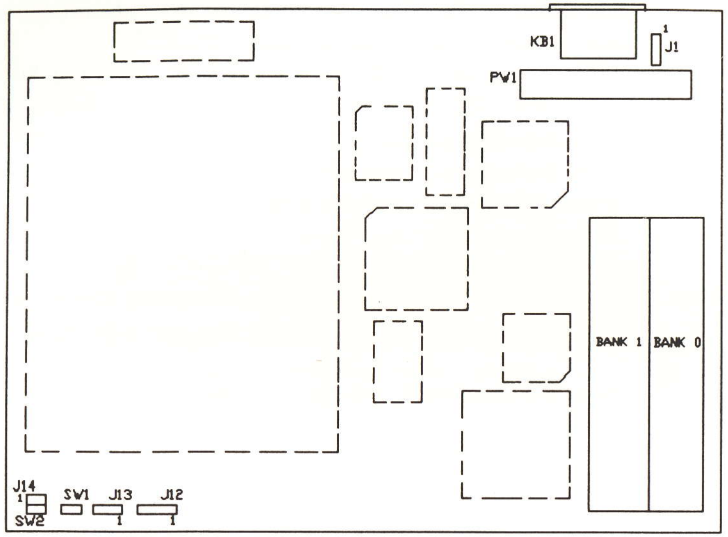


Fig 7 Connector Locations

3.5 CONNECTORS

3.5.1 PW1-POWER SUPPLY CONNECTOR

The power supply connector has twelve-pin male header connectors. Plug the dual connectors from the power directly onto the board connector.

PW1			
Pin	Description	Pin	Description
1	Power Good	7	Ground
2	+5V DC	8	Ground
3	+12V DC	9	-5V DC
4	-12V DC	10	+5V DC
5	Ground	11	+5V DC
6	Ground	12	+5V DC

Table 6

3.5.2 J12-KEYLOCK & POWER LED CONNECTOR

J12 is a keylock connector that enables and disables the keyboard and the Power-LED on the case.

Pin	Description
1	LED power
2	Not Used
3	Ground
4	Keyboard Inhibiter
5	Ground

Table 7

3.5.3 SW2-TURBO SWITCH CONNECTOR

SW2 connects to the Turbo switch, which is used to select the mainboard's clock speed.

Setting	Description
Short	Normal Mode
Open (default)	Turbo Mode

Table 8

3.5.4 J14-TURBO LED CONNECTOR

J14 is usually connected to a Turbo LED on front of the system case. If the system board select is in Turbo mode, the indicator will light during high-speed operation.

Pin	Description
1	+Anode
2	-Cathode

Table 9

3.5.5 J13-SPEAKER CONNECTOR

Attach the system speaker to connector J13.

Pin	Description
1	Data Out
2	Not Used
3	Ground
4	+5V

Table 10

3.5.6 SW1-RESET SWITCH CONNECTOR

Attach the Reset switch cable to this connector. The Reset switch restarts the system.

Setting	Description
Short	Reset
Open	Not Reset

Table 11

3.5.7 J1-EXTERNAL BATTERY

The GMB-386SOP mainboard has a battery on-board; however, user can also attach an external battery to connector J1. Using an external battery helps to conserve the on-board battery.

Pin	Description
1	VDD (6V)
2	INT. BATT.
3	INT. BATT. IN
4	Ground

Table 12

When using internal Battery short Pin 2, 3 by a micro jumper. When using external Battery, remove the micro jumper from Pin 2, 3 and connect the external battery connector onto J1.

3.5.8 KB1-KEYBOARD CONNECTOR

A standard five-pin female DIM keyboard connector is located at the rear of the keyboard. Plug the jack on the keyboard cable into this connector.

Pin	Description
1	Keyboard Clock
2	Keyboard Data
3	Spare
4	Ground
5	+5V DC

Table 13

3.6 SYSTEM ASSEMBLY OVERVIEW

After installing and connecting the mainboard, assemble components in the following order:

1. **Power Supply:** Place the power supply so that it fits the raised tongues on the chassis floor. Insert and fasten the two screws on the back panel of the chassis. Connect the power supply to the power supply connector, PW1.

2. **Disk Drives:** Slide disk drives into the chassis. Connect a wide 34-wire ribbon cable to each disk drive; this cable will attach to an adapter card. The power supply has four cables, each with four wires. Connect these cables to the disk drives.

3. **Adapter Cards:** Insert each adapter card -- Disk Controller cards, Video card, Serial/Parallel Interface card, etc. -- into an expansion slot. Refer to the installation and configuration instructions that comes with the card. Connect the disk drives to the Floppy Disk and Hard Disk Controller cards.

4. **Keyboard:** Connect the keyboard to its connector, KB1.

5. **Display:** Connect the display cable to the Video Card, and the display's power cord into a power outlet.

6. **Case:** Slide on the case cover and fasten its screws.

Connect the power cord to the power supply and plug it into a wall outlet. Put the boot disk into drive A: and turn on the power. User will then need to run the BIOS setup program.

CHAPTER 4 TECHNICAL REFERENCE

This chapter offers technical information relevant to the GMB-386SOP mainboard.

4.1 MEMORY MAP

The ROM code are address range 0C0000H - 0FFFFFH can be copied to RAM and executed from RAM. The code will run faster in RAM than in ROM. The shadow RAM can be enabled in 16K pages (C0000H-DFFFH).

Address	Name	Function
000000 to 07FFFF	512KB system board	System board memory
080000 to 09FFFF	128KB	I/O channel memory-IBM PC/AT 128KB Memory Expansion Option
0A0000 to 0BFFFF	128KB video RAM	Reserved for graphics display buffer
0C0000 to 0DFFFF	128KB I/O expansion ROM	Reserved for ROM on I/O adapters
0E0000 to 0EFFFF	64KB Reserved on system board	Duplicated code assignment at address FE0000
0F0000 to 0FFFFF	64KB ROM on the system board	Duplicated code assignment at address FF0000
100000 to FDFFFF	Maximum memory 15MB	I/O channel memory-IBM PC/AT 512KB Memory Expansion Option
FE0000 to FEFFFF	64KB Reserved on system board	Duplicated code assignment at address 0E0000
FF0000 to FFFFFF	64KB ROM on the system board	Duplicated code assignment at address 0F0000

Table 14

4.2 I/O MAP

The following I/O ports are used by the indicated devices on the system board.

HEX RANGE	DEVICE
000-01F	DMA controller 1 (8237A equivalent)
020-03F	Master interrupt controller 1 (8259A equivalent)
040-05F	Timer control registers (8254 equivalent)
060-06F	Keyboard controller command registers
070-07F	RTC registers, NMI mask
080-09F	DMA page register (74LS612 equivalent)
0A0-0BF	Interrupt controller 2 (8259A equivalent)
0C0-0DF	DMA controller 2 (8237A equivalent)
0F0-0F1	Clear and reset coprocessor
0F8-0FF	Coprocessor interface

Table 15

HEX RANGE	SYSTEM FUNCTION
100-1EF	Available for system expansion
1F0-1F8	Fixed Disk
1F9-1FF	Undefined
200-207	Game I/O port
208-277	Available for system expansion
278-27F	Parallel printer port 2
280-2F7	Available for system expansion
2F8-2FF	COM2 control and data registers
300-31F	Prototype card
320-35F	Available for system expansion
360-36F	Reserved
370-377	Available for system expansion
378-37F	Parallel printer port 1
380-38F	SDLC, bisynchronous communications port 2
390-39F	Available for system expansion
3A0-3AF	Bisynchronous communications port 1
3B0-3BF	Monochrome display and printer port
3C0-3CF	Reserved
3D0-3DF	Graphics controller registers
3E0-3EF	Undefined
3F0-3F7	Diskette controller registers
3F8-3FF	COM1 control and data registers
400-FFF	Available for system expansion

Table 16

4.3 SYSTEM INTERRUPTS

Level		Function
Microprocessor NMI		Parity or I/O Channel Check
Interrupt Controllers		
CTLR 1	CTLR 2	
IRQ 0		Timer Output 0
IRQ 1		Keyboard (Output Buffer Full)
IRQ 2		Cascade Interrupt Control
	IRQ 8	Realtime Clock Interrupt
	IRQ 9	INT 0AH
	IRQ 10	Reserved
	IRQ 11	Reserved
	IRQ 12	Reserved
	IRQ 13	Coprocessor
	IRQ 14	Fixed Disk
	IRQ 15	Reserved
IRQ 3		Serial alternate
IRQ 4		Serial primary
IRQ 5		Parallel 2
IRQ 6		Diskette
IRQ 7		Parallel 1

Table 17

4.4 DMA I/O ADDRESS MAP

HEX RANGE	COMMAND CODE
0C0	CH0 base and current address
0C2	CH0 base and current word count
0C4	CH1 base and current address
0C6	CH1 base and current word count
0C8	CH2 base and current address
0CA	CH2 base and current word count
0CC	CH3 base and current address
0CE	CH3 base and current word count
0D0	Read status register/Write command register
0D2	Write request register
0D4	Write single mask register
0D6	Write model register
0D8	Clear byte pointer flip flop
0DA	Read temporary register/Write master clear
0DC	Clear mask register
0DE	Write all mask register bits

Table 18

4.5 SYSTEM TIMER

The Counter/Timer (CTC) is located in the 82C291 IPC. It is used to create accurate time delays under software control. The CTC has three 16-bit counters, Counters 0-2, that can be programmed to count in binary or binary coded decimal (BCD). Each counter operates independently and can be programmed to operate as a timer or a counter.

There are six modes. Counter 0 and Counter 1 can be programmed for all six modes, however, mode 1 and mode 5 use is limited due to no external hardware trigger signal. Counter 2 can operate in any of the six modes.

Mode 0:	Interrupt of terminal count.
Mode 1:	Hardware retriggerable one-slot.
Mode 2:	Rate generator.
Mode 3:	Square wave generator.
Mode 4:	Software triggered strobe.
Mode 5:	Hardware retriggerable strobe.

4.6 SLOT SIGNALS

This section lists the pin assignments of the 16-bit I/O channels and describes the I/O channel signals.

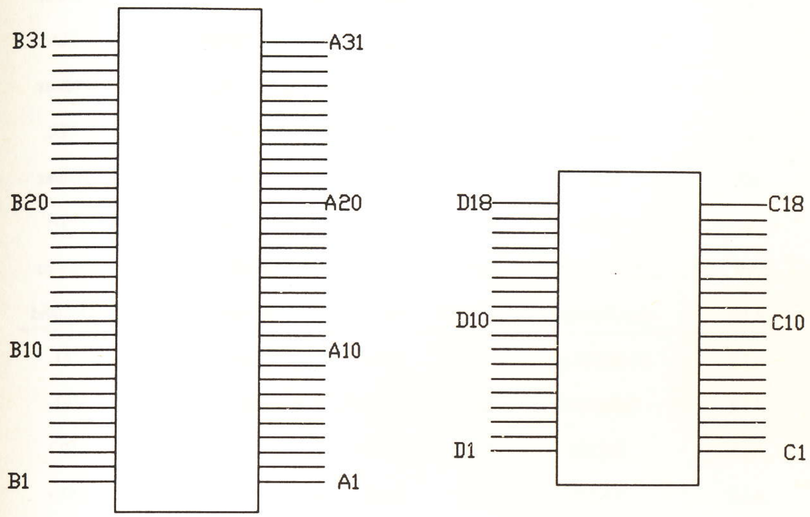


Fig 8 16-bit Channel Pin Assignments

PIN SIGNAL			PIN SIGNAL		
I/O Pin	Signal Name	I/O	I/O Pin	Signal Name	I/O
A1	-I/OCHCK	I	B1	GND	Ground
A2	SD7	I/O	B2	RESET DRV	O
A3	SD6	I/O	B3	+5VDC	Power
A4	SD5	I/O	B4	IRQ9	I
A5	SD4	I/O	B5	-5VDC	Power
A6	SD3	I/O	B6	DRQ2	I
A7	SD2	I/O	B7	-12VDC	Power
A8	SD1	I/O	B8	0WS	I
A9	SD0	I/O	B9	+12VDC	Power
A10	-IOCHRDY	I	B10	GND	Ground
A11	AEN	O	B11	-SMEMW	O
A12	SA19	I/O	B12	-SMEMR	O
A13	SA18	I/O	B13	-IOW	I/O
A14	SA17	I/O	B14	-IOR	I/O
A15	SA16	I/O	B15	-DACK3	O
A16	SA15	I/O	B16	DRQ3	I
A17	SA14	I/O	B17	-DACK1	O
A18	SA13	I/O	B18	DRQ1	I
A19	SA12	I/O	B19	-REFRESH	I/O
A20	SA11	I/O	B20	CLK	O
A21	SA10	I/O	B21	IRQ7	I
A22	SA9	I/O	B22	IRQ6	I
A23	SA8	I/O	B23	IRQ5	I

(TO BE CONTINUED)

PIN SIGNAL			PIN SIGNAL		
I/O Pin	Signal Name	I/O	I/O Pin	Signal Name	I/O
A24	SA7	I/O	B24	IRQ4	I
A25	SA6	I/O	B25	IRQ3	I
A26	SA5	I/O	B26	-DACK2	O
A27	SA4	I/O	B27	T/C	O
A28	SA3	I/O	B28	BALE	Buffer
A29	SA2	I/O	B29	+5VDC	Power
A30	SA1	I/O	B30	OSC	O
A31	SA0	I/O	B31	GND	Ground

PIN SIGNAL			PIN SIGNAL		
I/O Pin	Signal Name	I/O	I/O Pin	Signal Name	I/O
C1	SBHE	I/O	D1	-MEMCS16	I
C2	LA23	I/O	D2	-IOCS16	I
C3	LA22	I/O	D3	IRQ10	I
C4	LA21	I/O	D4	IRQ11	I
C5	LA20	I/O	D5	IRQ12	I
C6	LA19	I/O	D6	IRQ15	I
C7	LA18	I/O	D7	IRQ14	I
C8	LA17	I/O	D8	-DACK0	O
C9	-MEMR	I/O	D9	DRQ0	I
C10	-MEMW	I/O	D10	-DACK5	O
C11	SD8	I/O	D11	DRQ5	I
C12	SD9	I/O	D12	-DACK6	O

(TO BE CONTINUED)

	PIN SIGNAL			PIN SIGNAL	
I/O Pin	Signal Name	I/O	I/O Pin	Signal Name	I/O
C13	SD10	I/O	D13	DRQ6	I
C14	SD11	I/O	D14	-DACK7	O
C15	SD12	I/O	D15	DRQ7	I
C16	SD13	I/O	D16	+5VDC	Power
C17	SD14	I/O	D17	-MASTER	I
C18	SD15	I/O	D18	GND3	Ground

Table 19

4.6.1 I/O CHANNEL SIGNALS

Descriptions of the mainboard's I/O channel signals follow. Signal lines are all TTL compatible with a maximum loading of two low-power (LS) devices.

CLK (O)
The system clock is a synchronous microprocessor cycle clock.
RESET DRV (O)
This signal goes high at power-up, hardware reset, or when low line-voltage occurs.
SA0-SA19 (I/O)
The system address lines run from bit 0 through 19. They are latched onto the falling edge of BALE.
LA17 through LA23 (I/O)
The Unlatched Address Lines run from bit 17 to 23.
SD0-SD15 (I/O)
System Data bits 0 to 15.
BALE (buffered)
The Buffered Address Latch Enable is used in Latch SA0-Sa19 on the falling edge of BALE. During DMA cycles, BALE is forced high.

-I/O CH CK (I)
-I/O channel check is an active (low) signal which indicates that a parity error exists in the I/O board.
I/O CH RDY (I)
This signal lengthens I/O or memory cycles and should be held low with valid addresses. It can be held low for a maximum of 2.5 microseconds.
IRQ3-7, 9-12, 14-15 (I)
These Interrupt Request signals indicate I/O service request attention. They are prioritized in the following sequences: highest IRQ9, 10, 11, 12, 14, 15; and lowest IRQ3, 4, 5, 6, 7, 8.
-IOR (I/O)
The I/O Read signal is active low. It instructs an I/O device to drive its data onto the data bus.
-IOW (I/O)
The I/O Write signal is active low. It instructs an I/O device to read the data off the data bus.
-SMEMR (O)
The system Memory Read signal is low 1 megabyte memory is being used.
-MEMR (I/O)
The Memory Read signal is low while any of the memory locations are being read.
-SMEMW (O)
The System Memory write signal is low while the low 1 megabyte memory is being written.
-MEMW (I/O)
The Memory Write signal is low while any of the memory locations is being written.
DRQ0-3, 5-7 (I)
DMA Request channel 0 to 3 are for 8-bit data transfers. DRQ4 is used on the system board. Hold a DRQ line high until its DMA Request Acknowledge (DACK) goes active. Their priority is in the following sequences: highest DRQ0, 1, 2, 3; and lowest DRQ5, 6, 7.
-DACK 1-3, 5-7 (O)
These signals are used to are the corresponding signals for DRQ 0 to 3 and 5 to 7.
AEN (O)
The Address Enable is high when the DMA controller drives the address bus and is low when the CPU drives the address bus.

-REFRESH (I/O)
This signal indicates a refresh cycle is in progress. It is active low.
T/C (O)
This signal indicates the memory refresh cycle is in progress.
SBHE (I/O)
The System Bus High Enable signal indicates high byte SD8-15 is in the data bus.
-MASTER (I)
The Master signal gains control of the system. If this signal is held low for over 15 microseconds, system memory may be lost due to lack of refresh.
-MEM CS16 (I)
The I/O 16-bit Chip Select signal indicates the present data transfer is a 1 wait-state, 16-bit, I/O operation.
OSC (O)
The Oscillator 14.31818 MHz signal used for the color graphic card.
0WS (I)
The 0-Wait State indicates to the microprocessor that the present bus cycle can be completed without inserting any additional wait cycles.

QUICK REFERENCE TABLE

This table can help user to find information on specific jumpers and connectors m ore efficiently.

Jumper/Connector	Setting/Description	Page
J1	EXT Battery Connector	26
J2, J11	CPU Type Select	10
J4	Display Adapter Type	16
J5-J10	Cache Size Jumper Setting	15
J12	Keylock & Power LED Connector	24
J13	Speaker Connector	25
J14	Turbo LED Connector	25
KB1	Keyboard Connector	27
PW1	Power Supply Connector	23
SW1	Reset Switch Connector	26
SW2	Turbo Switch Connector	24

Table 20