G2 12MHz Zero-Wait '286 Turbo Mainboard User's Manual

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I. SPECIFICATION

* Intel or Compatible (AMD, HARRIS) 80286-10, 12 Microprocessor

* System Support Function:
  - 7-Channel Direct Memory Access (DMA)
  - 16-Level interrupt
  - System clock
  - Three programmable timer

* 32KB, 64KB selectable Read-Only Memory (ROM) subsystem, expandable to 128KB, fully compatible with IBM AT BIOS.

* Support on board 512K/640K/1M/2M/4M Random-Access Memory (RAM) subsystem, and expandable to 16MB RAM by added memory card on slot.

* 12MHz/0 wait state with 100ns DRAM.

* Complementary metal oxide semiconductor (CMOS) memory RAM to maintain system configuration.

* Real - Time Clock (RTC).

* Battery backup for CMOS configuration table and Real-Time Clock.

* Keyboard attachment.

* Speaker attachment.

* Support Hardware reset.

* Support Hardware speed change, and Turbo LED attachment.

* 5 Input/Output (I/O) slots with a 36-pin and a 62-pin card edge socket.

SYSTEM MEMORY MAP

Address	Name	Function
000000 to 07FFFF	512kb system board	System board memory
080000 to 09FFFF	128kb	I/O channel memory - IBM Personal Computer AT 128kb Memory Expansion Option
0A0000 to 0BFFFF	128kb video RAM	Reserved for graphics display fuffer
0C0000 to 0DFFFFF	128kb I/O expansion ROM	Reserved for ROM on I/O adapters
0E0000 to 0EFFFFF	64kb Reserved on system board	Duplicated cods assignment at address FE0000
0F0000 to 0FFFFFF	64kb ROM on system board	Duplicated cods assignment at address FF0000
100000 to FDFFFF	Maximum memory 15Mb	I/O channel memory - IBM Personal Computer AT 512kB Memory Expansion Option
FE0000 to FEFFFF	64kb Reserved on system board	Duplicated code assignment at address 0E0000
FF0000 to FFFFFF	64kb ROM on the system board	Duplicated code assignment at address 0F0000

I/O ADDRESS MAP

HEX RANGE	DEVICES	USAGE
000-01F	DMA controller 1	System
020-03F	Interrupt controller 1	System
040-05F	Timer	System
060-06F	8042 (Keyboard)	System
070-07F	Real time clock, NMI mask	System
080-09F	DMA page register	System
0A0-0BF	Interrupt controller 2	System
0C0-0DF	DMA controller 2	System
0F0	Clear Math Coprocessor busy	System
0F1	Reset Math Coprocessor	System
0F8-0FF	Math Coprocessor	System
1F0-1F8	Fixed disk	I/O
200-207	Game I/O	I/O
278-27F	Parallel printer port 2	I/O
2F8-2FF	Serial port 2	I/O
300-31F	Prototype card	I/O
360-36F	Reserved	I/O
378-37F	Parallel printer port 1	I/O
380-38F	SDLE, bisynchronous 2	I/O
3A0-3AF	Bisynchronous 1	I/O
3B0-3BF	Monochrome display and printer adapter	I/O
3C0-3CF	Reserved	I/O
3D0-3DF	Color/graphic monitor adapter	I/O
3F0-3F7	Floppy diskette controller	I/O
3F8-3FF	Serial port 1	I/O

II. G2 AT CHIPSet introduction

This mother board use G2 chipset, include a GC101A and two GC102, to instead most of LSI, MSI and SSI logic in standard IBM PC-AT, and implement a fully IBM PC-AT compatible system.

The GC101A is a peripheral controller. One of two GC102S is a data buffer, the other is an address buffer. Following is the introduction of this chipset:

GC101 Peripheral Controller Functional Description

The GC101 Peripheral Controller chip, the heart of a three-chip system, forms most of the control circuits and "glue" logic of the AT architecture into a single CMOS VLSI chip. Circuits embedded in this device include: an 82284, 74612, 8284, 8254, two 8237s, and two 8259s. The 82284 generates PROCCLK, /READY and /RESET for system use. It also provides all the CPU I/O command signals for memory, peripherals, and add-on boards. A 9-bit refresh counter produces the row address of memory during refreshes. The 74612 supplies memory mapping addresses. An 8284 uses the 14.318MHz input clock to generate OSC and a base clock for the 8254 timer/counter. This timer is programmed by the CPU and provides signals for system timing, refresh, and speaker tone generation.

The 8237s support Direct Memory Access, transferring 8-bit and 16-bit data between memory and I/O devices. Two 8259s are configured as master/slave; they receive interrupt requests from a timer, keyboard controller, a real time clock, the numeric processor and up to 11 other sources. They issue a signal to the CPU to initiate interrupt routines. The GC101 converts 16-bit buses for peripherals having only 8-bit wide buses; thus maintaining compatibility with the 8088 PC> The GC101A can access both 1M and 256k DRAMs, because it has two extra pins (ADRSEL and MA9); while the GC101 can access only 256Kx1 or 256Kx4 DRAMs. NOTE: references to the GC101 are generic, meaning either the GC101A or GC101. Except for the two extra pins in the GC101A, there is no difference between the two versions.

The GC101 design encompasses one wait state for memory operations and four wait states for I/O. The GC101 is internally programmed to insert, command delay based on the cycle type as shown in the table on the following page. To improve performance, use faster RAM and CPU, or reduce the memory wait states to zero by adding external synchronization logic. Memory is configurable from 256k to 4 MB by using RSEL0-RSEL2. Two inputs, HISPEED and IOSPEED, establish chip and system speeds. The chip operates up to 16MHz in the full commercial temperature range. (0-70°C)

GC102 Data Buffer Functional Description

The GC102 Data Buffer chip buffers data for the CPU (D0-15), the system expansion data bus (SD0-15), and the memory data bus (MD0-15). Two signals select data flow direction; DT/R controls flow between the D and SD buses, MBDIR controls flow between the MD and SD buses. For each signal, a high dictates flow to the SD bus, a low means flow from the SD bus. In addition, data latches between the D and SD buses are latched when CNTLOFF is high. The GC102 Data Buffer includes parity checking logic, for board implementations that can use it.

During memory read cycles, 16 RAM chips on the system board output MD to the GC102. Two additional RAM output MDPOUT0 (lower byte) and MDPOUT1 (upper byte). These 8 inputs are used in two 9-bit-wide parity-error detection circuits. During memory writes, the GC102 supplies MDPIN0, MDPIN1 and the MD bus to those 18 RAM chips.

Parity-error checking is enabled when MDPCKE input is high. If an error is detected on either byte of the memory data bus, and checking is enabled, /MDPCKN output goes low. Strap pin 73 HIGH to select Data Buffer mode. (LOW selects Address Buffer functions.)

GC102 Address Buffer Functional Description

The GC102 Address Buffer chip provides address buffers for the System expansion bus (SA0-15), the local I/O bus (XA1-16), and the system board DRAMs (MA0-8). ALE is included to latch addresses from the CPU.

Two signals select direction flow of the addresses; /DMAAEN controls the XA and SA buses, and CPUHLDA controls the MA and SA address buses. A low on either signal sends addresses to the SA bus, a high indicates the SA address bus is driving one of the other buses.

ADRSEL is input to the GC101A, and it controls RAS and CAS timing of bit MA9. A 10-bit address, needed for accessing 1 Mbit DRAMs, is produced by adding MA0-8 from this chip with MA9 from the GC101A. Strap pin 73 LOW to select Address Buffer mode. (HIGH selects Data Buffer functions.)

III. SYSTEM SUPPORT FUNCTION

SYSTEM TIMERS

The system has three programmable timer/ counters controlled by an Intel 82542 timer/ counter chip. These are channels 0 through 2, defined as follows:

Channel 0	System Timer
GATE 0	Tied on
CLK IN 0	1.190 MHz OSC
CLK OUT 0	8259A IRQ
Channel 1	Refresh Request Generator
GATE 1	Tied on
CLK IN 1	1.190MHz OSC
CLK OUT 1	Rqeust Refresh Cycle

Note: Channel 1 is programmed to generate a 15 micro-second period signal.

Channel 2	Tone Generation for Speaker
GATE 2	Controlled by bit 0 of port hex 61 PPI bit
CLK IN 2	1.190 MHz SOC
CLK OUT 2	Used to drive the speaker

SYSTEM INTERRUPTS

Sixteen levels of system interrupts are provided by the 80286 NMI and two 8259A Interrupt Controller chips. The following shows the interrupt-level assignments in decreasing priority:

LEVEL		FUNCTION
Microprocessor NMI		Parity or I/O channel check
Interrupt controllers		
CTRL 1	CTRL 2	
IRQ0		Timer output 0
IRQ1		Keyboard (Output buffer full)
IRQ2		Interrupt from CTRL 2
	IRQ8	Realtime clock interrupt
	IRQ9	Software redirected to INT 0AH (IRQ2)
	IRQ10	Reserved
	IRQ11	Reserved
	IRQ12	Reserved
	IRQ13	Coprocessor
	IRQ14	Fixed disk controller
	IRQ15	Reserved
IRQ3		Serial port 2
IRQ4		Serial port 1
IRQ5		Parallel port 2
IRQ6		Diskette controller
IRQ7		Parallel port 1

DIRECT MEMORY ACCESS

Eight DMA channels are supported by the system. TWo Intel 8237-5 DMA controller chips (four channels in each chip) are used. DMA channels are assigned as follows:

CTRL 1	CTRL 2
Ch0-Spare	Ch4-Cascade for CTRL 1
Ch1-SDLC	Ch5-Spare
Ch2-Diskette	Ch6-Spare
Ch3-Spare	Ch7-Spare

Channels 0 through 3 are contained in DMA controller 1. Transfers of 8-bit data, 8-bit I/O adapters and 8-bit or 16-bit system memory are supported by these channels. Each of these channels will transfer data in 64KB blicks throughout the 16-megabyte system address space.

Channel 4 through 7 are contained in DMA controller 2. To cascade channels 0 through 3 to the microprocessor, use channel 4. Transfers of 16-bit data between 16-bit adapters and 16-bit system memory are supported by channels 5, 6, 7. DMA channels 5 through 7 will transfer data in 128KB blocks throughout the 16-megabyte system address space. These channels will not transfer data on odd-byte boundaries.

The addresses for the page register are as follows:

PAGE RESIGER	I/O HEX ADDRESS
DMA Channel 0	0087
DMA Channel 1	0083
DMA Channel 2	0081
DMA Channel 3	0082
DMA Channel 5	008B
DMA Channel 6	0089
DMA Channel 7	008A
Refresh	008F

Address generation for the DMA channels is as follows:

* For DMA channels 3 through 0

SOURCE	DMA PAGE REGISTERS	8237A-5
Address	A23 - A16	A15 - A0

Note: To generate the addressing signal "byte high enable" (BHE) invert address line A0.

* For DMA channels 7 through 5

SOURCE	DMA PAGE REGISTERS	8237A-5
Address	A23 - A17	A16 - A1

Note: The BHE and A0 addressing signals are forced to a logic 0. DMA channel addresses do not increase or decrease through page boundaries (64KB for channels 0 through 3 and 128KB for channels 5 through 7).

REAL TIME CLOCK AND NONVOLATILE RAM

The real time clock MC146818 and its 64 bytes of RAM information are backed up by 6V DC battery. The internal clock circuitry uses 14 bytes while the rest is allocated to system configuration.

ADDRESS	DESCRIPTION
00	Seconds
01	Second alarm
02	Minutes
03	Minute alarm
04	Hours
05	Hour alarm
06	Day of week
07	Date of month
08	Month
09	Year
0A	Status register A
0B	Status register B
0C	Status register C
0D	Status register D
0E	Diagnostic status byte
0F	Shutdown
10	Diskette drive type byte - driver A and B
11	Reserved
12	Fixed disk type byte - driver C and D
13	Reserved
14	Equipment byte
15	Low base memory
16	High base memory
17	Low expansion memory byte
18	High expansion memory byte
19-2D	Reserved
2E-2F	2 byte CMOS checksum
30	Low expansion memory byte
31	High expansion memory byte
32	Data century byte
33	Information flags (set during power on)
34-3F	Reserved

IV I/O CHANNEL INTRODUCTION

The I/O channel supports:

* I/O address space hex 100 to hex 3FF

* 24 - bit memory address (16MB)

* Refresh of system memory from channel microprocessor

* Selection of data accesses (either 8 bit or 16 bit)

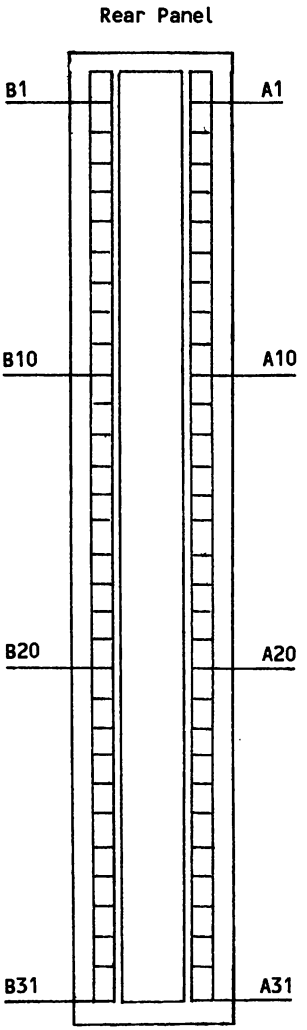
* Interrupt

* DMA channels

* I/O wait - state generation

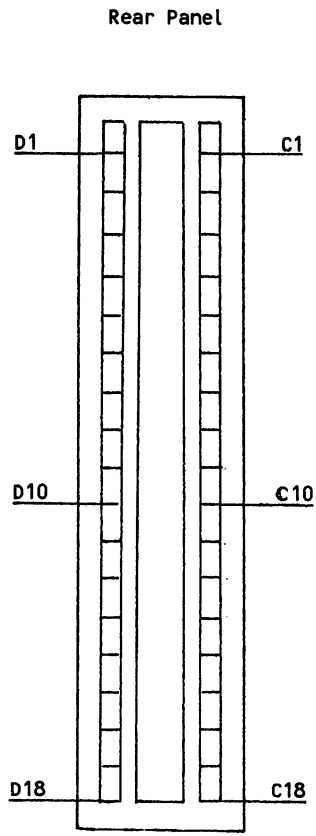
* Open-bus structure (allowing multiple microprocessors to share the system's resources, including memory)

The following figure shows the pin numbering for I/O channel connectors JP15, JP16, JP17, JP18, JP31.



I/O Channel Pin Numbering

The following figure shows the pin numbering for I/O channel connectors JP6, JP7, JP8, JP9, JP14.



I/O Channel Pin Numbering

The following figures summarize pin assignments for the I/O channel connectors.

I/O Pin	Signal Name	I/O
A1	-I/O CH CK	I
A2	SD7	I/O
A3	SD6	I/O
A4	SD5	I/O
A5	SD4	I/O
A6	SD3	I/O
A7	SD2	I/O
A8	SD1	I/O
A9	SD0	I/O
A10	-I/- CH RDY	I
A11	AEN	O
A12	SA19	I/O
A13	SA18	I/O
A14	SA17	I/O
A15	SA16	I/O
A16	SA15	I/O
A17	SA14	I/O
A18	SA13	I/O
A19	SA12	I/O
A20	SA11	I/O
A21	SA10	I/O
A22	SA9	I/O
A23	SA8	I/O
A24	SA7	I/O
A25	SA6	I/O
A26	SA5	I/O
A27	SA4	I/O
A28	SA3	I/O
A29	SA2	I/O
A30	SA1	I/O
A31	SA0	I/O

I/O Channel (A-Side,JP15,JP16,JP17,JP18,JP31)

I/O Pin	Signal Name	I/O
B1	GND	Ground
B2	RESET DRV	O
B3	+5 Vdc	Power
B4	IRQ9	I
B5	-5 Vdc	Power
B6	DRQ2	I
B7	-12 Vdc	Power
B8	OWS	I
B9	+12 Vdc	Power
B10	GND	Ground
B11	-SMEMW	O
B12	-SMEMR	O
B13	-IOW	I/O
B14	-IOR	I/O
B15	-DACK3	O
B16	DRQ3	I
B17	-DACK1	O
B18	DRQ1	I
B19	-Refresh	I/O
B20	CLK1	O
B21	IRQ7	I
B22	IRQ6	I
B23	IRQ5	I
B24	IRQ4	I
B25	IRQ3	I
B26	-DACK2	O
B27	T/C	O
B28	BALE	O
B29	+5 Vdc	Power
B30	OSC	O
B31	GND	Ground

I/O Channel (B-Side,JP15,JP16,JP17,JP18,JP31)

I/O Pin	Signal Name	I/O
C1	SBHE	I/O
C2	LA23	I/O
C3	LA22	I/O
C4	LA21	I/O
C5	LA20	I/O
C6	LA19	I/O
C7	LA18	I/O
C8	LA17	I/O
C9	-MEMR	I/O
C10	-MEMW	I/O
C11	SD08	I/O
C12	SD09	I/O
C13	SA10	I/O
C14	SA11	I/O
C15	SA12	I/O
C16	SA13	I/O
C17	SA14	I/O
C18	SA15	I/O

I/O Channel (C-Side,JP6,JP7,JP8,JP9,JP14)

I/O Pin	Signal Name	I/O
D1	-MEM CS16	I
D2	-I/O CS16	I
D3	IRQ10	I
D4	IRQ11	I
D5	IRQ12	I
D6	IRQ15	I
D7	IRQ14	I
D8	-DACK0	O
D9	DRQ0	I
D10	-DACK5	O
D11	DRQ5	I
D12	-DACK6	O
D13	DRQ6	I
D14	-DACK7	O
D15	DRQ7	I
D16	+5 Vdc	Power
D17	-MASTER	I
D18	GND	Ground

I/O Channel (D-Side,JP6,JP7,JP8,JP9,JP14)

I/O Channel Signal Description

The following is a description of the system board's I/O channel signals. All signal lines are TTL-compatible. I/O adapters should be designed with a maximum of two low-power shottky (LS) loads per line.

SA0 through SA19 (I/O)

Address bits 0 through 19 are used to address memory and I/O devices within the system. Three 20 address lines, in addition to LA17 through LA23, allow access of up to 16MB of memory. SA0 through SA19 are gated on the system bus when 'BALE'. is high and are

latched on the falling edge of 'BALE'. These signals are generated by the microprocessor or DMA controller. They also may be driven by other microprocessor or DMA controllers that reside on the I/O channel.

LA17 through LA23 (I/O)

Theses signals (unlatched) are used to address memory and I/O devices within the system. These signals are valid when "BALE" is high. LA17 through LA23 are not latched during microprocessor cycles and therefore do not stay valid for the whole cycle. Their purpose is to generate memory decodes for 1 wait-state memory cycles. These decodes should be latched by I/O adapters on the falling edge of 'BALE.' These signals also may be driven by other microprocessors or DMA controllers that reside on the I/O channel.

CLK (O)

This is the 6-MHz system clock. It is a synchronous microprocessor cycle clock with a cycle time of 167 nanoseconds. The clock has a 50% duty cycle. This signal should only be used for synchronization. It is not intended for uses requiring a fixed frequency.

RESET DRV (O)

'Reset drive' is used to reset or initialize system logic at power-up time or during a low line-voltage outage. This signal is active high.

SD0 through SD15 (I/O)

These signals provide bus bits 0 through 15 for the microprocessor, memory, and I/O devices. D0 is the least-significant bit and D15 is the most-significant bit. All 8-bit devices on the I/O channel should use D0 through D7 for communications to the microprocessor. The 16-bit devices will use D0 through D15. To support 8-bit devices, the data on D8 through D15 will be gated to D0 through D7 during 8-bit transfers to these devices; 16-bit microprocessor transfers to 8-bit devices will be converted to two 8-bit transfers.

BALE (0) (buffered)

'Address latch enable' is provided by the 82288 bus controller and is used on the system board to latch valid addresses and memory decodes from the microprocessor. It is a available to the I/O channel as an indicator of a valid microprocessor or address SA0 through SA19 are latched with the falling edge of 'BALE'. 'BALE' is forced high during DMA cycles.

-I/O CH CK (I)

'-I/O channel check' provides the system board with parity (error) information about memory or devices on the I/O channel. When this signal is active, it indicates an uncorrectable system error.

I/O CH RDY (I)

'I/O channel ready' is pulled low (not ready) by a memory or I/O device to lengthen I/O or memory cycles. Any slow device using this line should drive it low immediately upon detecting its valid address and a Read or Write command. Machine cycles are extended by an integral number of clock cycles (167 nanoseconds). This signal should be held low for no more than 2.5 microseconds.

IRQ3-IRQ7, IRQ9-IRQ12 and IRQ 14 through 15 (I)

Interrupt Requests 3 through 7, 9 through 12, and 14 through 15 are used to signal the microprocessor that an I/O device needs attention. The interrupt requests are prioritized, with IRQ9 through IRQ12 and IRQ14 through IRQ15 having the highest priority (IRQ9 is the highest) and IRQ3 through IRQ 7 having the lowest priority (IRQ7 is the lowest). An interrupt request is generated when an IRQ line is raised from low to high. The line must be held high until the microprocessor acknowledges the interrupt request (Interrupt Service routine). Interrupt 13 is used on the system board and is not available on the I/O channel. Interrupt 8 is used for the read-time clock.

-IOR (I/O)

'-I/O Read' instructs an I/O device to drive its data onto the data bus. It may be driven by the system microprocessor or DMA controller, or by a microprocessor or DMA controller resident on the I/O channel. This signal is active low.

-IOW (I/O)

'-I/O Write' instructs an I/O device to read the data on the data bus. It may be driven by any microprocessor or DMA controller in the system. This signal is active low.

-SMEMR (O) -MEMR (I/O)

These signals instruct the memory devices to drive data onto the data bus. '-SMEMR' is active only when the memory decode is within the low 1Mb of memory space. '-MEMR' is active on all memory read cycles. '-MEMR' may be driven by any microprocessor or DMA controller in the system. '-SMEMR' is derived from '-MEMR', it must have the address lines valid on the bus for one system clock period before driving '-MEMR' active. Both signals are active LOW.

-SMEMW (O) -MEMW (I/O)

These signals instruct the memory devices to store the data present on the data bus. '-SMEMW' is active only when the memory decode is within the low 1Mb of the memory space. '-MEMw' is active on all memory read cycles. '-MEMW' may be driven by any microprocessor or DMA controller in the system. '-SMEMW' is

derived from '-MEMW' and the decode of the low 1Mb of memory. When a microprocessor on the I/O channel wishes to drive '-MEMW', it must have the address lines valid on the bus for one system clock period before driving '-MEMW' active. Both signals are active low.

DRQ0-DRQ3 and DRQ5-DRQ7 (I)

DMA Requests 0 through 3 and 5 through 7 are asynchronous channel requests used by peripheral devices and the I/O channel microprocessors to gain DMA service (or control of the system). They are prioritized, with 'DRQ0' having the highest priority and 'DRQ7' having the lowest. A request is generated by bringing a DRQ line to an active level. A DRQ line must be held high until the corresponding 'DMA Request Acknowledge' (DACK) line goes active. 'DRQ0" through 'DRQ3' will perform 8-bit DMA transfers; 'DRQ5' through 'DRQ7' will perform 16-bit transfers. 'DRQ4' is used on the system board and is not available on the I/O channel.

-DACK0 to -DACK3 and -DACK5 to -DACK7 (O)

-DMA Acknowledge 0 to 3 and 5 to 7 are used to acknowledge DMA requests (DRQ0 through DRQ7). They are active low.

AEN (O)

'Address Enable' is used to degate the microprocessor and other devices from the I/O channel to allow DMA transfers to take place. When this line is active, the DMA controller has control of the address bus, the data-bus

Read command lines (memory and I/O), and the Write command lines (memory and I/O).

-REFRESH (I/O)

This signal is used to indicate a refresh cycle and can be driven by a microprocessor on the I/O channel.

T/C (O)

'Terminal Count' provides a pulse when the terminal count for any DMA channel is reached.

SBHE (I/O)

'Bus High Enable' (system) indicates a transfer of data on the upper byte of the data bus, SD8 through SD15. Sixteen-bit devices use 'SBHE' to condition data bus buffers tied to SD8 through SD15.

-MASTER (I)

This signal is used with a DRQ line to gain control of the system. A processor or DMA controller on the I/O channel may issue a DRQ to a DMA channel in cascade mode and receive a '-DACK'. Upon receiving the '-DACK', an I/O microprocessor may pull '-MASTER' low, which will allow it to control the system address, data, and control lines (a condition known as tri-state). After '-MASTER' is low, the I/O microprocessor must wait one system clock period before driving the address and data lines, and two clock periods before issuing a Read and Write command. If this signal is held low for more than 15 microsec-

onds, system memory may be lost because of a lack of refresh.

'MEM CS16 (I)

'-MEM 16 Chip Select' signals the system board if the present data transfer is a 1 wait-state, 16-bit, memory cycle. It must be derived from the decode of LA17 through LA23. '-MEM CS16 should be driven with an open collector or tri-state driver capable of sinking 20 mA.

'I/O CS16 (I)

'-I/O 16 bit Chip Select' signals the system board that the present data transfer is a 16-bit, 1 wait-state, I/O cycle. It is derived from an address decode. '-I/O CS16' is active low and should be driven with an open collector or tri-state driver capable of sinking 20 mA.

OSC (O)

'Oscillator' (OSC) is a high-speed clock with a 70-nanosecond period (14.31818 MHz). This signal is not synchronous with the system clock. It has a 50% duty cycle.

0WS (I)

The 'Zero Wait State' (0WS) signal tells the microprocessor that it can complete the present bus cycle without inserting any additional wait cycles. In order to run a memory cycle to a 16-bit device without wait cycles, '0WS' is derived from an address decode gated with a Read or Write command. In order to

run a memory cycle to an 8-bit device with a minimum of two wait states, '0WS' should be driven active one system clock after the Read or Write command is active gated with the address decode for the device. Memory Read and Write commands to an 8-bit device are active on the falling edge of the system clock. '0WS' is active low and should be driven with an open collector or tri-state driver capable of sinking 20 mA.

V JUMPER SETTING AND CONNECTOR PIN ASSIGNMENT

The system board has the following connectors and jumpers. Configure your system according to the table below:

JUMPER	FUNCTION
J 20	Battery power ON/OFF
J 25	EPROM size selection
J 26	Display selection
J 27,J 28,J 29	DRAM size setting
J 34	RTC chip selection
J 35	Parity enable/disable

CONNECTOR	FUNCTION
J 1	Keylock and Power on LED connector
J 2	Turbo mode LED indicator
J 3	Speaker connector
J 4	Hardware reset connector
J 5	Turbo switch for select high or low speed
J 19	External battery connector
J 32	Power supply connector
J 33	Keyboard connector

1. Description of Jumper Setting

Placing a jumper cap over some jumper means "ON"; Removing it away means "OFF"

J 20: Battery power
ON: Connect battery to the RTC circuit.
OFF: Disconnect battery to the RTC circuit.

If the system board would be shipped for a long time, this jumper cap could be removed for saving power consumption. But on normal operation, this jumper cap must be placed over.

J 25: EPROM SIZE
1-2 ON: 27128 ROM inserted
2-3 ON: 27256 ROM inserted

J 26: Display selection
ON: Color graphic
OFF: Monochrome

J 27,J 28,J 29 :DRAM Size setting when using 256K DRAM, J 28 must be "ON", and J 27, J 29 perform as follows:

J 27	J 29	Select
ON	ON	TEST MODE
ON	OFF	0-512K
OFF	ON	0-640K
OFF	OFF	0-640K, 1M-1.384M

When using 1M DRAM, J 28 must be "OFF",and J 27, J 29 perform as follows:

J 27	J 29	Select
ON	ON	0-512K
ON	OFF	0-640K
OFF	ON	0-640K, 1M-2.384M
OFF	OFF	0-640K, 1M-4.384M

J 34: RTC chip selection
1-2 ON: RTC chip using DS1287
2-3 ON: RTC chip using 146818

J 35: Parity enable/disable
ON : Parity enable
OFF: Parity disable

2. Description Of Connector Pin Assignment

J 1: Keylock and Power on LED connector

PIN	ASSIGNMENT
1	Power LED
2	Not used
3	GND
4	Keyboard inhibit
5	GND usually connected with Black wire

J 2: Turbo LED Indicator

J2 is connected with external Turbo LED indicator. LED turns on when the system is in 12 MHz.

J 3: Speaker Connector

PIN	ASSIGNMENT
1	Data out
2	Not used
3	GND
4	+5V usually connected with red wire

J 4: Hardware reset

J 4 is connected with External Hardware Reset Button to enable Hardware Reset

J 5: Turbo switch for select high or low speed

J 5 is connected with external hardware speed change button to change processor frequency.

J 19: External battery connector

If J 19 is used to take place of rechargeable battery, the four "AA" batteries will sustain about 4 months

PIN	ASSIGNMENT	WIRE COLOR
1	6V	Red
2	Not used	Don't care
3	GND	Black
4	GND	Black

J 32: Power Supply Connector

J32 is used to connect to the power supply cable

PIN	ASSIGNMENT	WIRE COLOR
1	Power good	Orange
2	+5V	Red
3	+12V	Yellow
4	-12V	Blue
5	GND	Black
6	GND	Black
7	GND	Black
8	GND	Black
9	-5V	White
10	+5V	Red
11	+5V	Red
12	+5V	Red

J 33: Keyboard Connector

J 33 is a 5-pin, 90-degree printed circuit board mounting, DIN connector.

PIN	ASSIGNMENT
1	Keyboard clock
2	Keyboard Data
3	Not used
4	GND
5	+5V

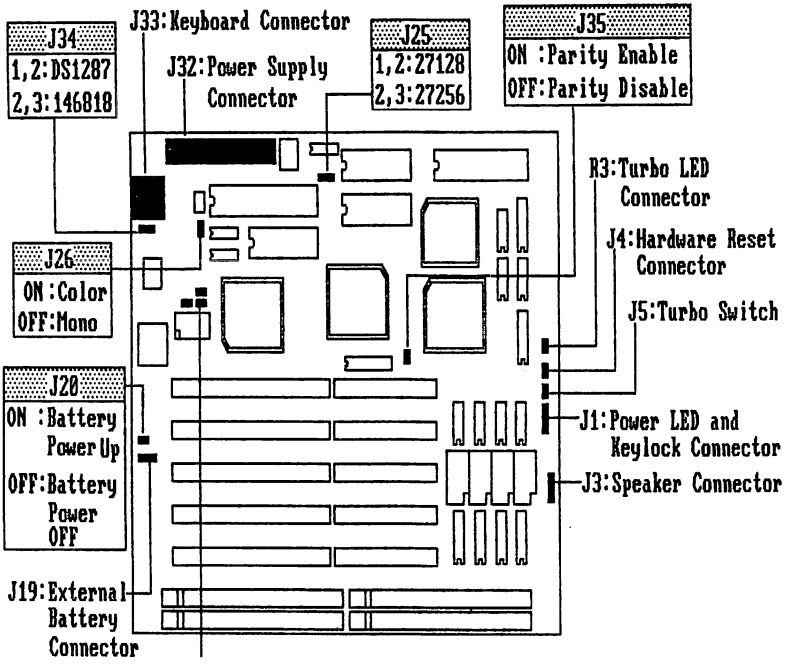
VI. HOW TO CONTROL THE SYSTEM SPEED BY SOFTWARE

1. Press "Ctrl","Alt" and "-" to change speed or press "Ctrl", "Alt" and "+" to change speed.
   A: <Alt>
   C: <Ctrl>
   S: <Shift>
   -: <->
   +: <+>
   \: <\> slash

2. When equipment of mainboard used AWARD BIOS and PTC 8042 Controller.
   A: <Alt>
   B: <Ctrl>
   -: <->
   +: <+>
   \: <\> slash

3. When equipment of mainboard used AMI BIOS.
   A: <Alt>
   B: <Ctrl>
   C: <\> slash

G2 MAIN BOARD OUTLINE DIAGRAM



J27	J28	J29	RAM Size
ON	ON	ON	Test Mode
ON	ON	OFF	0-512K
OFF	ON	ON	0-640K
OFF	ON	OFF	0-640K, 1M-1.384M
ON	OFF	ON	0-512K
ON	OFF	OFF	0-640K
OFF	OFF	ON	0-640K, 1M-2.384M
OFF	OFF	OFF	0-640K, 1M-4.384M

* If J28 "ON" must insert 256K DRAM, i.e.41256,44256 or 256K RAM Module into DIP socket or RAM Module socket. But they can't be installed simultaneous.
* If J28 "OFF" can install 1M RAM Module only.