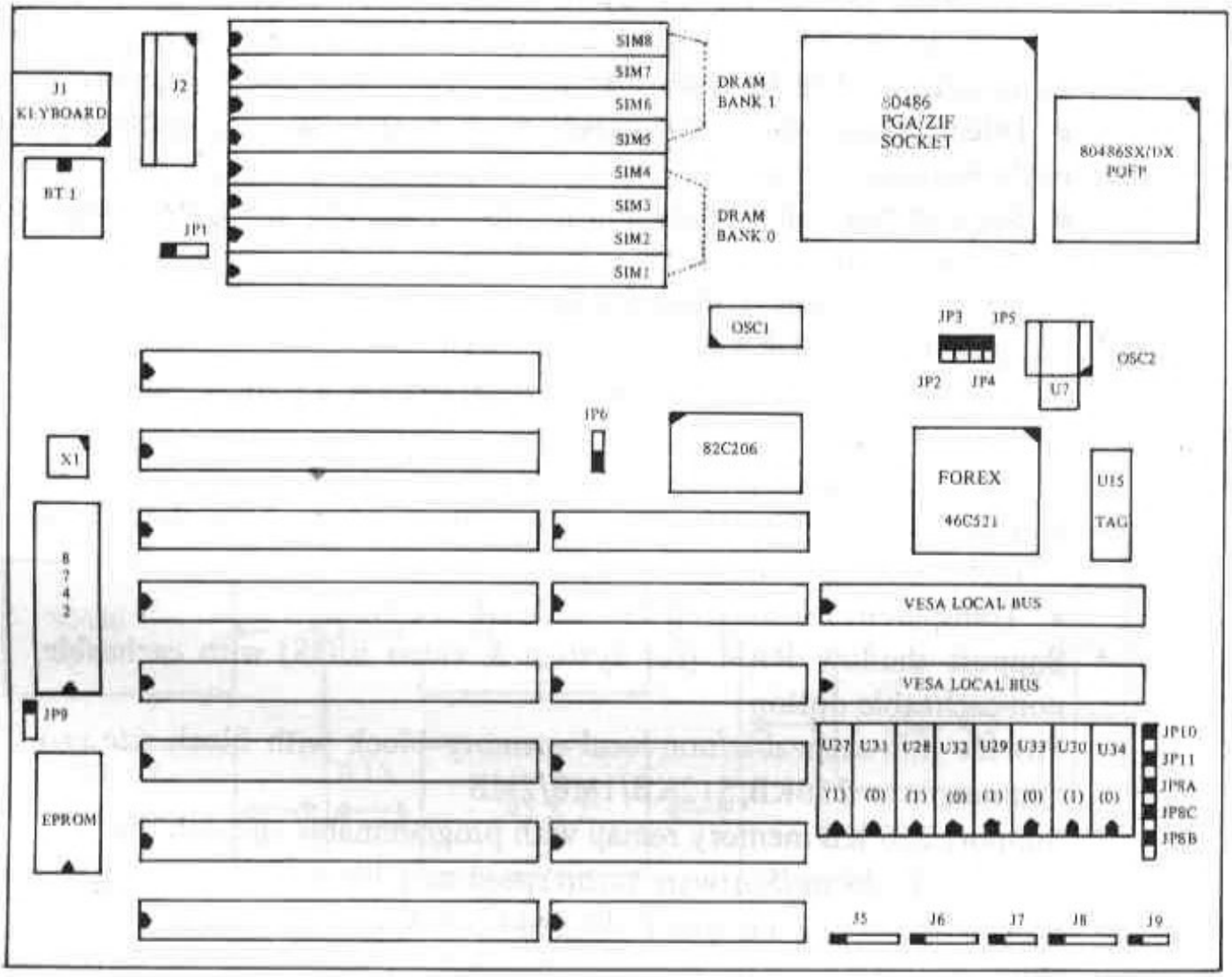
SYSTEM BOARD LAYOUT



FEATURES

* One 160-pin PQFP single chip solution
* Fully PC/AT compatible @ 50/40/33/25 MHz 486DX/486SX/ 66/50 MHz 486 DX2, and Cyrix 486DLC systems

* Fully integrated cache controller
  - Direct mapped 64K/128K/256K/512K byte write back cache
  - 16-byte cache line size
  - Support 486 burst mode and no update penalty for systems without ext. cache
  - Option of 2-Bank/1-Bank Cache
* Highly optimized DRAM controller
  - Support up to 64 MB DRAM (1/2/4/5/6/8/9/12/16/20/24/32/36/ 48/64 MB).
  - Support 16-Mega-bit DRAM
  - Fast page mode DRAM access with programmable wait states (0,1,2, or 3 wait states)
  - Transparent memory refresh without CPU hold
* Support shadow RAM (for system & video BIOS) with cacheable/ non-cacheable option
* Provide non-cacheable/non-local memory block with block size programmable to 256KB/512KB/1MB/2MB
* Support 256 KB memory remap with programmable cacheability
* Support Hardware/Software turbo speed switching
* Programmable AT bus speed: divided by 2, 3, 4, 5, 6 or 8 from system clock
* Support Single (512K bits) BIOS EPROM.
* Support AT bus I/O-command-recovery option for slow I/O adapters
* Support fast gate A20
* Support complete VESA local bus interface (support up to 2 VESA Bus Master)

SYSTEM OVERVIEW

The FOREX 486 Cache system board is 2/3 Baby AT-sized, fully PC/AT compatible and offers outstanding performance and feautures.

With 64K, 128K, or 256K cache memory on board, this system board is really a high speed machine that is well suited for building advanced personal computers or workstations.

The FOREX 486 Cache system board is designed with the FRX46C521 chipset which are highly integrated. With this chipset, there are only a few discrete devices required, which allows 2 memory banks to be placed on the board. The size of the memory can be scaled from 1 MB up to 64 MB.

FEATURES

The FOREX 486 Cache system board supports (or includes) the following features:

* Intel 80486DX CPU at 25/33/50 MHz, Intel 80486DX2 at 50/66 MHz

* FOREX 486 chipset, FRX46C521, which contain:
  Cache Controller - 0 wait state memory access if cache hit
  Memory Controller - fast page mode operation
  Bus Controller - fully PC/AT compatible

* Direct mapped cache memory, upto 256KB
  SRAM speed:

  For Double Bank (64K/256K)

Clock (MHz)	TAG SRAM	DATA SRAM
20	35 ns	35 ns
25	30 ns	30 ns
33	20 ns	25 ns
50	15 ns	20 ns

For Single Bank (128K)

Clock (MHz)	TAG SRAM	DATA SRAM
20	35 ns	35 ns
25	30 ns	25 ns
33	20 ns	20 ns
50	20 ns	15 ns

* Support Intel 487SX numerical co-processor and P24T CPU
* 2 memory banks on board
  Supports 1 MB upto 64 MB memory size
  DRAM speed: fast page mode, 80 ns or 100 ns

* Software bus speed selection for maximum compatibility with add-on cards

* Dual processing speed selection via software or hardware switch

  Turbo mode: <CTRL><ALT><+>
  Enable the internal 8KB cache of Intel 80486

  Non-turbo: <CTRL><ALT><–>
  Disable the internal 8KB cache of Intel 80486

* Software-controlled shadow RAM for system and/or video BIOS.

* Two 32-bit VESA local bus slot, four 16-bit expansion slots, two 8-bit expansion slot

* Real time clock

* Hardware turbo switch

SYSTEM PERFORMANCE

Clock oscillators used for the system performance measurement

DRAM SIMM SOCKETS

The FOREX 486 Cache system board will support 2 DRAM banks, Bank 0 and Bank 1 in SIMM sockets, on board.

With the use of 256Kx9, 1Mx9 or 16Mx9 DRAM modules, 1M and upto 64 M of local memory can be attained. Please refer to the following table for the detailed installation.

memory size		bank 0	bank 1
1 M	==>	256K	
2 M	==>	256K	256K
5 M	==>	256K	1M
20 M	==>	1M	4M
4 M	==>	1M	
8 M	==>	1M	1M
16 M	==>	4M	
32 M	==>	4M	4M
64 M	==>	16M	

The corresponding part reference are as below:

Bank 0 – SIM 1, SIM 2, SIM 3, SIM 4 (SIMM SOCKET)
Bank 1 – SIM 5, SIM 6, SIM 7, SIM 8 (SIMM SOCKET)

CONNECTORS

A connector is two or more pins that are used to make connections to the system standard accessories (such as power, battery, etc.)
The following is a list of connectors on board, as well as descriptions of each individual connector.

(A) BT1 Rechargeable Battery

Pin #	Assignment
1	Battery Positive
2	Ground

(F) J6 Speaker

Pin #	Assignment
1	Speaker Data
2	No Connection
3	Ground
4	+ 5V DC

(G) J7 Turbo Switch

Pin #	Assignment	Pin 1 & 2	Function
1	Pullup (+ 5V DC)	Open	Non-Turbo
2	Turbo Control	Closed	Turbo

(H) J8 Front Panel Key Lock and Power LED

Pin #	Assignment
1	Power LED
2	No Connection
3	Ground
4	Keyboard Lock
5	Ground

(I) J9 Reset Switch

Pin #	Assignment	Pin 1 & 2	Function
1	Reset control	Open	No action
2	Ground	Closed	Reset

JUMPERS

A jumper is two or three pins which may, or may not be covered by a plastic connector plug. A jumper is used to select different system options.

(A) JP2, JP3, JP4, JP5 CPU Selection

JP2, JP5 Pin #	Function
1 - 2	486DX/DX2 PGA CPU
2 - 3	486SX/DX PQFP/486SX/487SX/P23T PGA CPU

JP3, JP4	Pin #	Function
	1 - 2	486DX/DX2 CPU/487SX/P23T PGA CPU
	2 - 3	486SX/DX PQFP CPU

(B) JP6 IPC 206 Discharge (to reset system CMOS setup)

(C) JP7A, 7B, 7C CPU clock Select (for clock IC)

Pin #	JP7A	JP7B	JP7C	CPU Clock (MHz)
	2-3	1-2	1-2	20
	1-2	2-3	1-2	25
	1-2	1-2	2-3	33,33
	2-3	1-2	2-3	50

(D) JP8A, 8B, 8C Cache Memory Size Select

JP8A&C	Pin #	Function
	1-2	128K/256K cache memory
	2-3	64K cache memory

JP8B	Pin #	Function
	1-2	64K/256K cache memory
	2-3	128K cache memory

(E) JP9 Keyboard Diagnostic (for system dynamic burning test)

(F) JP10 Local bus high speed Write wait Selection

JP10	Pin #	Function
	1-2	to select 0 WS (<= 33 MHz clock)
	2-3	to select 1 WS (> 33 MHz clock)

(G) JP11 Local bus high speed clock Selection

JP11	Pin #	Function
	1-2	to select <= 33 MHz clock
	2-3	to select > 33 MHz clock