	PCISYS-56
	PROCESSOR

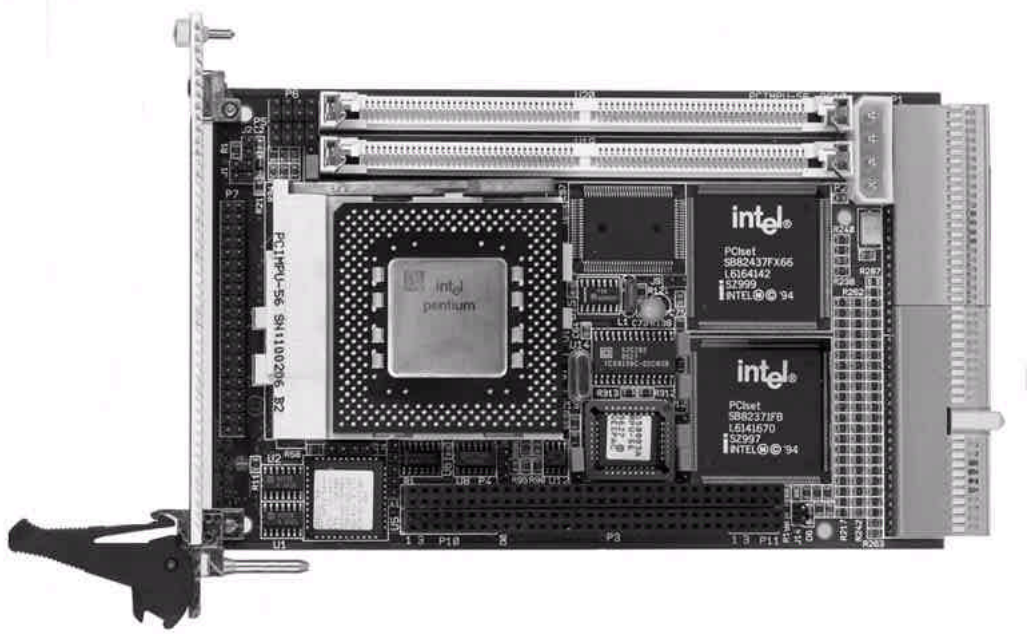
Revision 1.2

HIGH PERFORMANCE *CompactPCI*® PENTIUM SYSTEM

The PCISYS-56 is a very high performance, highly integrated Pentium assembly built on a compact 3U Eurocard format. It uses a Pentium 75 to 200 MHz processor, two standard 72-pin SIMM modules for up to 64MB of EDO memory, and the Intel "TRITON" chip set to provide the highest level of performance in a compact format. This combination of power and rugged industrial packaging makes the board an ideal choice for industrial automation, real-time machine control, telecommunication or medical systems applications. The *CompactPCI*® bus provides the features and benefits of the PCI bus specification 2.0 (32 or 64 bit, 132 or 264 MB/s bandwidth, Plug & Play) on a 3U or 6U Eurocard and an IEC-1076 compliant shielded, high density connector, allowing up to 8 boards to be connected in the same backplane.
The PCISYS-56 includes the PCIMPU-56 core CPU board with a PC/104 expansion connector that can be used to connect to GESPAC's GESPCI-1A or the GESPCI-1 Peripheral Modules to add the basic PC functions, including COM1/2, LPT1, keyboard, floppy and VGA for CRT or LCD. The PCISYS-56 is fully compatible with the PC architecture and can run any PC based operating system: DOS, WINDOWS, WINDOWS 95, WINDOWS™ NT, OS/2™, or any other operating system and application designed for the PC platform.

Technical features

- Pentium @ 75 to 200 MHz
- ZIF socket mounted CPU, Fan unit and Temp sensor
- 16 Kb of internal cache memory
- 72-pin SIMMs for 8, 16, 32 or 64MB RAM
- EDO memory supported
- Enhanced IDE interface (two hard disks)
- 512 Kb FLASH EPROM BIOS
- 3U format (100x160mm)
- Fully compatible with CompactPCI®
- Power supply: +3.3V, +5V, +12V
- 32-bit CompactPCI® bus interface (5 Volt)
- 16-bit PC-104 extension port
- Watchdog timer, Real Time Clock
- COM1&2 serial port (16550)
- Optional Infrared on COM2
- LPT1 parallel interface (EPP/ECP)
- Floppy disk interface
- Keyboard controller
- Optional Fully compatible G-96 bus extension
- SVGA controller for CRT and LCDs
  - Up to 1024x768 / 256 colors (1MB VRAM)
  - EL, STN, TFT, Plasma display compatible
  - Simulscan



References

PCISYS-56: Pentium-based CompactPCI® Assembly

TABLE OF CONTENTS

1. GENERAL INFORMATION 5
1.1 PCIMPU-56 CPU MODULE 5
1.2 GESPCI-1 PERIPHERAL MODULE 5
1.3 GESPCI-1A PERIPHERAL MODULE 5
1.4 TECHNICAL FEATURES 5
2. PREPARATION FOR USE AND INTERCONNECTION 6
2.1 PCIMPU-56 JUMPER DESCRIPTIONS 6
2.2 PCIMPU-56 CONNECTOR DESCRIPTION 8
2.3 GESPCI-1 JUMPERS AND CONNECTORS 9
2.4 GESPCI-1 CONNECTOR DESCRIPTION 11
2.5 FUNCTIONAL DESCRIPTION 14
2.5.1 CPU 14
2.5.2 PERFORMANCE UPGRADE 14
2.5.3 SYSTEM MEMORY 14
2.5.3.1 EDO DRAM 15
2.5.4 PCI (PERIPHERAL COMPONENT INTERCONNECT) 15
2.5.4.1 82437FX Triton System Controller (TSC) 15
2.5.4.2 82438FX Triton Data Path (TDP) 15
2.5.4.3 82371FB CompactPCI® PC/104/IDE Accelerator (PIIX) 15
2.5.5 NATIONAL SEMICONDUCTOR 87306 SUPER I/O CONTROLLER 15
2.5.5.1 Two NS16C550-compatible UARTs with send/receive 16 byte FIFO 15
2.5.5.2 Multi-mode bi-directional parallel port ... 15
2.5.5.3 Industry standard floppy controller 15
2.5.5.4 Integrated Real Time Clock 15
2.5.5.5 Integrated 8042 compatible keyboard controller 15
2.5.5.6 Keyboard Interface. 15
2.5.5.7 Real Time Clock (RTC) 15
2.5.5.8 CMOS RAM 16
2.5.5.9 Battery 16
2.5.5.10 IrDA (InfraRed) Support 16
2.5.5.11 VGA VIDEO Controller 16
2.5.5.12 FLASH Implementation 16
2.5.6 SET-UP UTILITY 16
2.5.7 POWER MANAGEMENT 17
2.5.8 POWER CONSUMPTION 17
2.5.9 ENVIRONMENTAL 17
2.6 USER-INSTALLABLE UPGRADES 17
2.6.1 SYSTEM MEMORY 17
2.6.2 PCIMPU-56 MEMORY MAP 17
2.6.3 I/O MAP 18
2.6.4 PCIMPU-56 DMA MAP 18
2.6.5 PCIMPU-56 CompactPCI® CONFIGURATION SPACE MAP 18
2.6.6 PCIMPU-56 INTERRUPTS 19
2.6.7 PLUG & PLAY BIOS 19
3. GETTING STARTED 20
3.1 GENERAL INFORMATION 20
3.2 CPU UPDATE 20
3.3 THE BIOS UPDATE UTILITY 20
3.3.1 MR_ZAPPA SYSTEM BIOS AND FLASH UPLOAD UTILITY 20
3.4 FAILSAFE RECOVERY PREPARATION 20
3.4.1 MR BIOS ® INSTALLATION INSTRUCTIONS 21
3.4.2 FAILSAFE RECOVERY - CORRUPTED FLASH BIOS 21
3.5 PRECAUTION FOR USE 22

REVISION HISTORY

Rev	Date (m/d/y)	By	Modification
0.1	10/20/96	JCR	Preliminary version
1.0	1/27/96	CP	Reformatted to word7 Added schematics
1.1	3/03/97	JCR	Corrections
1.2	09/22/97	JCR	Modifications and adding

Updated revision of this document can be obtained on the Gespac Web sites:
`http://www.gespac.com` (USA site)
`http://www.gespac.ch` (European site)

IMPORTANT NOTICE

Gespac reserves the right to change products or specifications detailed in this documentation at any time without notice, and assumes no responsibility for any errors within this document. Gespac does not make any commitment to update this information. Gespac assumes no responsibility for the use of any products described in

this documentation, nor does the Company assume responsibility for the functioning of undescribed features or parameters.

CompactPCI® and CompactPCI® logo are registered trademarks of the PCI Industrial Computers Manufacturers Group.

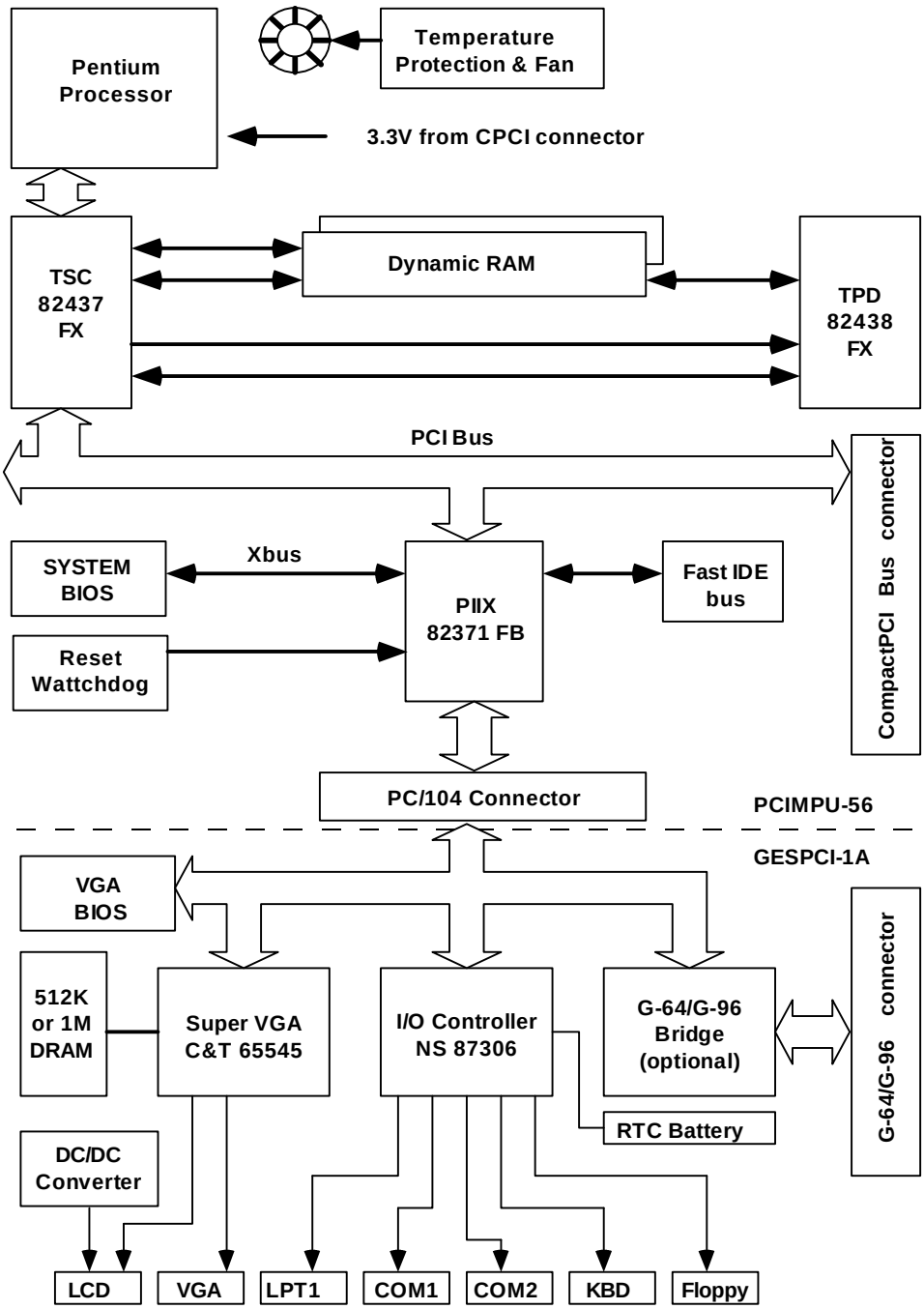


Figure 1.1 Block diagram

1. GENERAL INFORMATION

1.1 PCIMPU-56 CPU MODULE

The PCIMPU-56 board is the core CPU board of the PCISYS-56 CompactPCI® System. It includes the Pentium processor, the "TRITON" chip set, Two sockets for SIMM memory modules allowing for up to 64Mb of DRAM. The Pentium CPU is a 64 bit wide architecture and two 32-bit wide memory modules are required to provide 64-bit wide memory access. This module supports the fully Synchronous 25/30/33 MHz PCI Bus Interface on the 8 slots CompactPCI® Bus. The PCI Bus Arbiter supports the ISA BRIDGE (PIIX) and four PCI Bus Masters.

A PC-104 8/16 bit connector makes it possible to add the GESPCI-1, GESPCI-1A and/or other external PC-104 modules.

1.2 GESPCI-1 PERIPHERAL MODULE

The GESPCI-1 module is the peripheral board of the PCIMPU-56. This peripheral module is mounted onto the PCIMPU-56 board using the PC/104 connector. It includes both the video controller and the I/O controller. The I/O controller provides the Real time clock, COM1, COM2, LPT1 ports and the keyboard controller. The VGA interface on the GESPCI-1 uses the Chips and Technology 65545 controller chip. The C&T 65545 can drive a CRT display and most LCD displays such as STN (monochrome or color), EL or TFT technology.

1.3 GESPCI-1A PERIPHERAL MODULE

The GESPCI-1A module is a limited version of the GESPCI-1 module featuring only the I/O controller. The I/O controller provides the Real time clock, COM1, COM2, LPT1 ports and the keyboard controller. This module is used for blind node configuration with PCIMPU-56 or with another display controller module on the CompactPCI® BUS.

1.4 TECHNICAL FEATURES

CPU Type	Intel Pentium or Cyrix/IBM 6x86, 75,90,100,120,133, 166, 200 MHz
Cache memory	16 k Internal cache on the CPU
Memory	8,16,32 or 64 MB. Two SIMM modules of EDO or Fast Page Mode DRAM
FLASH EPROM	128 KB BIOS, programmable on board
CPU Mounting	ZIF socket
Intel “TRITON” Chip set	82437FX system controller, 82438FX data path, 82371FB PCI / ISA / IDE accelerator bridge: PCI to DRAM > 100 MB/s
BIOS	Plug & Play BIOS from UNICORE
Safety	Watchdog timer, CPU Fan Unit and CPU Temperature monitoring
Mass storage	40 pins EIDE interface for two drives
Bus interface	CompactPCI® revision 1.0. PCI interface 2.0 compliant PC/104 8/16 bit connectors G-96 industrial I/O bus
Video interface	Chips & Technology 65545 SVGA controller with 512Kb or optional 1Mb video RAM Compatible with CRT and EL display, STN monochrome or color, TFT
I/O controller	National Semiconductor 87306 I/O chip
Serial interface	Two NS16C550 compatible UARTs with 16 Bytes FIFO. Support for IRDA compliant device on COM2
Parallel interface	Multi-mode bi-directional parallel port, IBM CENTRONIC compatible.Enhanced Parallel Port (EPP) with BIOS/Driver, High speed mode: ECP compatible
Floppy disk controller	720Kb,1.2 and 1.44 or 2.88Mb controller
Real time clock	Software compatible with DS1287/MC146818
Keyboard controller	8042AH/PC87911 Compatible keyboard controller
Power supply	+3.3, +5, +12Volt from PCI bus
Stand alone operation	Power supply (+3.3, +5) plug-in socket for PCIMPU-56 Power supply (+5, +12Volt) plug-in socket for GESPCI-1
Typical Consumption	75MHz Pentium +5V @ 3.3 Amps +12V @ 75 mA
Operating temperature	0 to 50 Degrees Celsius with forced-air cooled CPU
EMC	EMC compliant
Electrical and mechanical specifications	PC/AT, PCI 2.0 and CompactPCI® 1.0 specifications
Dimensions	PCIMPU-56 100x160 mm GESPCI-1 100x160 mm

2. PREPARATION FOR USE AND INTERCONNECTION

Table 2.1 identifies jumpers and connectors of the PCIMPU-56. Figure 2.1 shows their locations on the printed circuit.

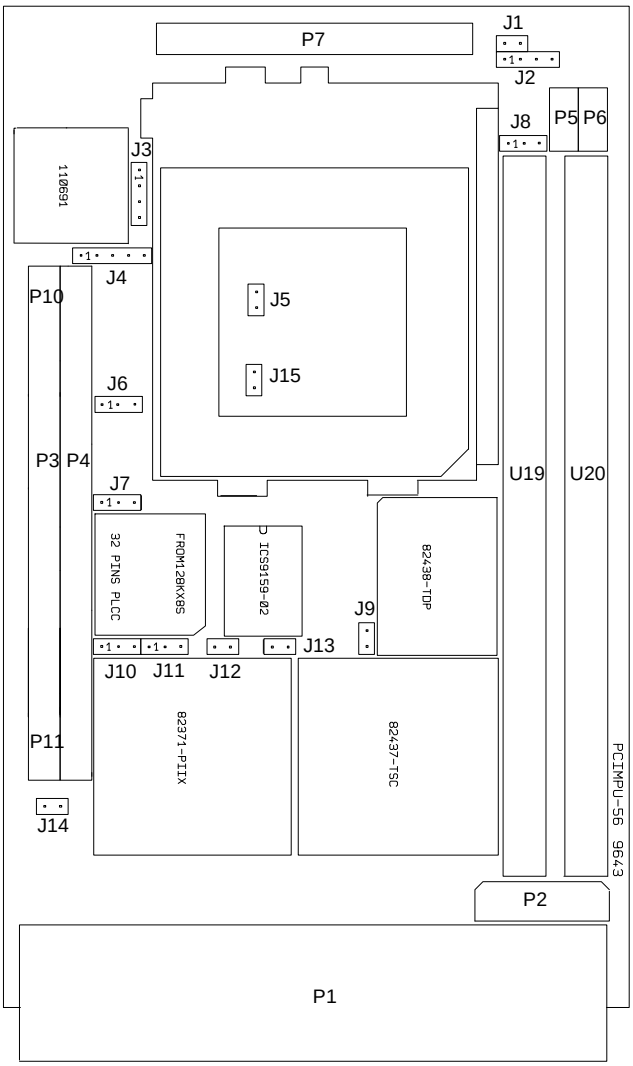


Figure 2.1 Jumper and Connector locations on the PCIMPU-56

2.1 PCIMPU-56 JUMPER DESCRIPTIONS

Designation	Function
J1	LED connection for Enhanced IDE interface activity monitoring
J2	External speaker connection
J3	Fan unit power
J4	External reset switch
J5	Multiplying factor for the INTERNAL PLL of the PENTIUM
J6	Select watchdog timer action (Interrupt or hard RESET)
J7	BIOS FLASH EPROM programming mode (RECOVERY or NORMAL)
J8	DRAM power supply (Vcc or 3.3 Volt)
J9	Enable over-temperature status on NMI bus
J10	FLASH EPROM programming (+12V or PWOK)
J11	FLASH EPROM programming (+12V or TTL Level 1)
J12	Bus Frequency selection (CLKSEL 1)
J13	Bus Frequency selection (CLKSEL 0)
J14	Operational mode (Standby or Active)
J15	idem as J5

Table 2.1 Jumpers Identification

Header J1 -LED connection for Enhanced IDE interface

Front panel LED is mounted directly onto this connector to indicate the status of the Enhanced IDE device. The LED is blinking when the IDE device is accessed.

Pin 1 is cathode
Pin 2 is anode

Header J2 - External speaker connection

The external speaker can be connected to this connector between pin 1 and 4.

Pin 1 is the output
Pin 2 is not connected
Pin 3 is the Ground
Pin 4 is the Vcc

Header J3 - Fan unit power connection

The PCIMPU-56 comes with a "Boxed Pentium". It include the CPU plus a fan unit. This fan unit should be powered in order to cool the CPU. Fan unit power connectors should be mounted onto jumper 3 between pin 3 and 4.

Pin 1 and 4 are grounded
Pin 2 is +5V
Pin 3 is +12V

Header J4 - External reset connection

An external Reset switch can be mounted into the system. This switch should be directly connected onto this connector between pin 1 and 2.

Pin 1 is the reset input
Pin 2 is grounded
Pin 3-4 are not connected
Pin 5 is 5V (Vcc)

Jumpers J5-J15 - MPU frequency selections

This jumper is used to select the different internal clock speed multiplying factor according to the type of CPU.

J5(BF0)	J15(BF1)	PENTIUM Frequency	BUS Frequency
OFF	ON	200 MHz	66 MHz
ON	ON	166	66
ON	ON	150	60
ON	OFF	133	66
ON	OFF	120	60
OFF	OFF	100	66
ON	OFF	100	50
OFF	OFF	90	60
OFF	OFF	75	50

See J12& J13 jumper table for BUS Frequency Selection

Jumper J6 - Select watch dog interrupt on NMI or HARD RESET

The PCIMPU-56 can be programmed with a watchdog timer in order to continuously monitor the activity of the CPU board. If for some reason the CPU is stopped, an IRQ or RESET is generated 1.2 seconds later. This IRQ is used in application programs to shut down the system in a stable state.

J6 Position	Operation
(1-2) OFF	watchdog NMI disabled
(1-2) ON	watchdog NMI enabled
(2-3) OFF	watchdog Hard Reset disabled
(2-3) ON	watchdog Hard Reset enabled

The watchdog function must be enabled with software.

Jumper J7 - BIOS FLASH EPROM programming mode (RECOVERY or NORMAL)

This jumper is used to set the FLASH EPROM BIOS programming mode (See J10 & J11 operation table for details).

Jumper J8 - DRAM power supply (Vcc or 3.3V)

This jumper selects the voltage level used by the DRAM SIMM module.

J8 Position	Operation
(1-2) ON	5V DRAM
(2-3) ON	3.3V DRAM

Jumper J9 - Enable temperature monitoring

The PCIMPU-56 board is designed for rugged industrial environment. If the fan unit on top of the Pentium CPU fails, the Pentium internal temperature may become so high that the CPU can be destroyed. This situation is unacceptable and the PCIMPU-56 board is designed to monitor the temperature of the Pentium CPU. This jumper is used to generate an NMI interrupt if the temperature of the Pentium CPU becomes dangerously high.

J9 Position	Operation
OFF	NO NMI generated on overtemp
ON	NMI generated on overtemp

This function must be enabled with software.

Jumpers J7/J10 & J11 - FLASH EPROM programming

These jumpers are used to select the programming mode of the FLASH EPROM that is mounted on the PCIMPU-56 board.
The default factory positions are for Normal operation or BIOS Update.

Operation	J7	J10	J11
Normal	2-3	2-3	1-2
BIOS Update	2-3	2-3	1-2
BIOS Recovery	1-2	1-2	1-2

Jumper J12 & J13 - Bus Frequency selection

These jumpers are used to select the CPU external bus speed and the PCI speed.

J12	J13	CPU	PCI operation
on	on	50 MHz	25 MHz
off	on	60 MHz	30 MHz
on	off	66 MHz	33 MHz

Jumper J14 - Operational MODE

This jumper can be connected to a push-button for manual sleep mode activation. These functions can be activated by software (see BIOS function).

J14 Position	Operation
OFF	CPU activated
ON(OFF)	Sleep mode /normal operation

2.2 PCIMPU-56 CONNECTOR DESCRIPTION

The following tables describe the connector available on the PCIMPU-56 board (see PCIMPU-56 connector implantation figure).

Designation	Function
P1	CompactPCI® connector
P2	+3.3V, +5V stand alone power supply (+12V must be supplied on GESPCI-1)
P3	PC/104 connector (16 bit)
P4	PC/104 connector (8 bit)
P5	Emulation connector
P6	Emulation connector
P7	Enhanced IDE connector (two mass storage master/slave)
P10	+3.3V Power supply/GND from GESPCI-1 and Sideband signals
P11	+3.3V from GESPCI-1 and others control signal

Connector P1 - CompactPCI®

All the PCI signals of the CompactPCI® connector are included in this IEEC-1076-4 standard connector. The distribution of the different signals of the PCI bus have been engineered to minimize the cross-talk. This connector also provides external shielding in order to maximize the signal to noise ratio on the PCI bus. Complete details on the CompactPCI® are available in the CompactPCI® specification.

Connector P2 - +3.3, +5 Volt stand alone power supply

This connector is used to power the PCIMPU-56 board for standalone configurations. The P2 connector should be externally powered as follows:

Pin	Signals
4	+5V (Vcc)
2	GND
3	GND
1	+3.3 V

WARNING:
You must be careful with Connector P2!
It uses the same connector type as the disk drive connector (+12,+5). Do not exchange the P2 cable with a disk drive power cable!
Connector P3 & P4 - PC/104 connector

The PCIMPU-56 module interconnects directly to the PC/104 bus (8 and 16 bit interface). For more information on the PC104 bus please refer to the PC/104 reference manual.

PC-104 modules can be of two bus types, 8-bit and 16-bit. The two defined modules are supported with P3 and P4 connectors. The 16-bit,Option 1 Stackthrough P3 is fully implemented on this card.

For more information on the BUS, refer to the PC-104 specification manual.

P4 ROW A	P4 ROW B	P3 ROW C	P3 ROW D	Pin
--	--	GND	GND	0
/IOCHCHKP	GND	/SBHE	/MEMCS16	1
SD7	RSDRV	LA23	/IOCS16	2
SD6	+5V	LA22	IRQ10	3
SD5	IRQ9	LA20	IRQ11	4
SD4	nc	LA21	IRQ12	5
SD3	nc	LA19	IRQ15	6
SD2	nc	LA18	IRQ14	7
SD1	/WS0	LA17	nc	8
SD0	+12V	/MEMR	nc	9
IOCHRDY		/MEMW	/DACQ5	10
AEN	/SMEMW	SD8	DRQ5	11
SA19	/SMEMR	SD9	/DACK6	12
SA18	/IOW	SD10	DRQ6	13
SA17	/IOR	SD11	nc	14
SA16	/DACK3	SD12	nc	15
SA15	DRQ3	SD13	+5V	16
SA14	/DACK1	SD14	/MASTER	17
SA13	DRQ1	SD15	GND	18
SA12	/REF		GND	19
SA11	SYSCLK			20
SA10	nc			21
SA9	nc			22
SA8	IRQ5			23
SA7	nc			24
SA6	nc			25
SA5	nc			26
SA4	TC			27
SA3	BALE			28
SA2	+5V			29
SA1	OSC			30
SA0	GND			31
GND	GND			32

Table 2.2 PC/104 Connector

Connector P7 - Enhanced IDE interface

One or two IDE Hard Disk drive units can be interfaced to the MPU-56A board using the 40-pin IDC connector. The following table identifies the pin numbers of the P7 connector and the corresponding signal names and functions.

Signal Name	Pin	Pin	Signal Name
Reset IDE	1	2	Ground
Host Data 7	3	4	Host Data 8
Host Data 6	5	6	Host Data 9
Host Data 5	7	8	Host Data 10
Host Data 4	9	10	Host Data 11
Host Data 3	11	12	Host Data 12
Host Data 2	13	14	Host Data 13
Host Data 1	15	16	Host Data 14
Host Data 0	17	18	Host Data 15
Ground	19	20	Key
DRQ3	21	22	Ground
I/O Write-	23	24	Ground
I/O Read-	25	26	Ground
IOCHRDY	27	28	BALE
DACK3-	29	30	Ground
IRQ14	31	32	IOCS16-
Addr 1	33	34	Ground
Addr 0	35	32	Addr 2
Chip Select 0-	37	38	Chip Select 1-
Activity	39	40	Ground

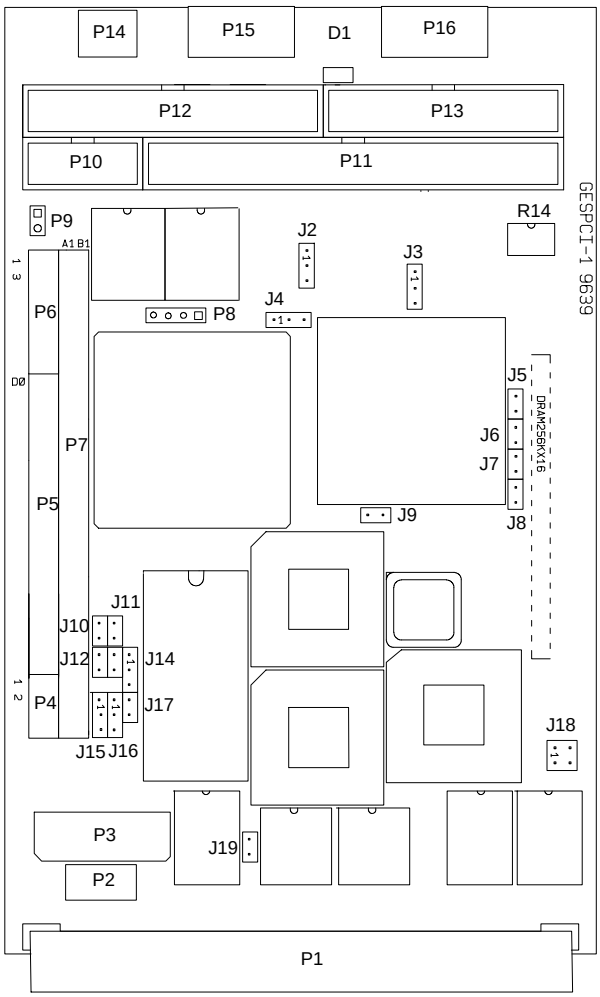
Connector P10 & P11 - Additional signals for PCIMPU-56 and GESPCI-1

GESPAC includes additional signals in the external part of the PC/104 connector (16 bit extension). But full PC/104 (8 or 16 bit) is guaranteed. These signals are as follows:

P10 pin	Name	Function
1	BERR1	G-96 Bus error
2	IRQ1	IRQ1 from KBC
3	IRQ8	IRQ8 from RTC
4	CS0	Chip select from 87306
5	GATEA20	A20 from KBC controller
6	HP OUT	Timer out to ext HP
7	spare	
8	MRRST	Reset input to ext RESET
9-10-11-12	VCC3	+3.3V from ext Power Connector
13-14-15-16	GND	Power Ground

P11 pin	Name	Function
1-3		spare
2	GND	GND
3	SRST	soft reset from KBD
5-6-7-8	VCC	+5V from ext Power Connector

2.3 GESPCI-1 JUMPERS AND CONNECTORS



GESPCI-1 Jumper description

Designation	Function
J2	Selects ±VEE from DC/DC converter
J3	+3.3 Volt / VCC selection for LCD display
J4	IRQ selection from VGA or G-96
J5	DRAM mode selection
J6	DRAM mode selection
J7	DRAM mode selection
J8	DRAM mode selection
J9	Internal VGA or PCI VGA selection
J10	IRQ5 from G96 to PC/104
J11	IRQ10 from G96 to PC/104
J12	IRQ15 from G96 to PC/104
J13	IRQ11 from G96 to PC/104
J14	IRQ12 from G96 to PC/104
J15	Battery on / clear selection
J16	Bus error (NMI or BERR) selection
J17	NMI or PFAIL from G-96 to PC/104
J18/1	Selects memory access from G-96 or PC/104
J18/2	Selection SSD on G-96 bus
J19	Enable G-96 access

Jumper J2 - ±VEE selection from DC/DC converter

J2 Position	Operation
OFF	DC/DC out disabled
1-2	+Vee adjustable with R14
2-3	-Vee adjustable with R14

The DC/DC converter is only activated when the graphic controller is programmed in LCD or SIMULSCAN Mode.

Jumper J3 - 3.3 Volt/Vcc selection for LCD display

J3 Position	Operation
OFF	not permitted
1-2	3.3V
2-3	5V (factory default)

Jumper J4 - IRQ selection from VGA or G-96

J4 Position	Operation
OFF	IRQ 9 Available for other resources
1-2	IRQ 9 from G-96 BUS
2-3	IRQ 9 dedicated to VGA

Jumper J5, J6, J7, J8 - DRAM type selection. These jumpers are FACTORY POSITIONNED and must not be changed.

Jumper J9 - Internal VGA or PCI VGA selection

J9 Position	Operation
OFF	VGA on CPCI
ON	VGA on GESPCI-1

Jumper J10, J11, J12, J13, J14 - IRQ from G-96 to PC-104

Position	Operation
J10 OFF	IRQ5 free for ISA/PCI peripherals
J10 ON	IRQ5 from G-96
J11 OFF	IRQ10 free for ISA/PCI peripherals
J11 ON	IRQ10 from G-96
J12 OFF	IRQ15 free for ISA/PCI peripherals
J12 ON	IRQ15 from G-96
J13 OFF	IRQ11 free for ISA/PCI peripherals
J13 ON	IRQ11 from G-96
J14 OFF	IRQ12 free for ISA/PCI peripherals
J14 1-2 ON	IRQ12 from G-96
J14 2-3ON	IRQ12 reserved for SUPER I/O

Jumper J15 - Battery / clear selection

J15 Position	Operation
OFF	For Storage
1-2	RTC connected to battery
2-3	clear RTC backup-RAM

Jumper J16 - Bus error (NMI or BERR) selection

J16 Position	Operation
OFF	G-96 Bus error disabled
1-2	G-96 Berror to Pentium Berror
2-3	G-96 Berror to NMI

Jumper J17 - NMI or PFAIL from G-96 to PC/104

J17 Position	Operation
OFF	NMI/PWFAIL from G-96 disabled
ON	NMI/PWFAIL enabled

If J16 and J17 are OFF, NMI is free for others peripherals

Jumper J18/1 - Select memory access from G-96 or PC/104

J18/1 Position	Operation
OFF	D000-D7FF on G-96
1-2	D000-D7FF on PC-104 BUS

This option is only valid with the G-96 Bridge activated. In CPCI ONLY configuration D000-D7FF is allocated to PC-memory or PC-104 memory modules.

Jumper J18/2 - Selection SSD module for G-96

J18/2 Position	Operation
OFF	C800-CBFF on PC-104 BUS
1-2	C800-CBFF redirected to G-96

This option is only valid with the G-96 Bridge activated. In CPCI ONLY configuration CB00-CBFF is allocated to PC-memory or PC-104 memory modules.

Jumper J19 - Enable G-96 access

J19 Position	Operation
OFF	G-96 Bridge disabled
ON	G-96 Bridge activated

2.4 GESPCI-1 CONNECTOR DESCRIPTION

The following tables describe the connectors available on the GESPCI-1 board.

Designation	Function
P1	G-96 connector
P2	+5, +12 Volt stand alone power supply (Not using the G-96 connector)
P3	+3.3, +5Volt for PCIMPU-56 and LCD display
P4	VCC power supply for PCIMPU-56 and soft reset
P5	PC/104 connector (16 bit)
P6	Power supply 3.3V / GND + additional signals for ISA bridge
P7	PC/104 connector (8 bit)
P8	IRDA connector
P9	Keyboard lock connector
P10	COM1
P11	LCD Connector
P12	Floppy disk interface
P13	LPT1
P14	PS/2 style KBD connector
P15	COM2
P16	VGA connector for CRT

Connector P1 - G-96 Connector

This connector is only installed if G-96 Bus is used. For additional information see the G-96 specifications.

The connectors **P2** and **P3** are used to power the GESPCI-1 board for standalone configurations.

Following Documentation is correct for revision 9618.

Connector P2 - 5, 12 Volt stand alone power supply

Pin	Signals
1	+12 Volt
2	GND
3	GND
4	+5 Volt

This external power connector is used to power the GESPCI-1 board for standalone configurations. The connector is compatible with HARD-DISK power connectors.

Connector P3 - +3.3 Volt for PCIMPU-56 and LCD display

Pin	Signals
1	+3.3 Volt
2	GND

This connector is used to power the PCIMPU-56 and the GESPCI-1 in a standalone configuration.

Pin	*Signals*
1	**+12V**
2	GND
3	GND
4	**VCC**

P2 Cable Connections for GESPCI-1 9639 rev. **C**

Pin	*Signals*
1	**VCC**
2	GND
3	GND
4	**+12V**

P2 Cable Connections for GESPCI-1 9639 rev. **C1**

On the GESPCI-1 Rev 9639, the P3 connector type was changed. It is now similar to a power supply connector for hard-disk drive. You must **take care** with this connector: don't plug directly "standard" disk-drive cable on it. Voltage on pin 1 must be **3.3V** and not 12V. The connections must be done according to the following table:

Pin	*Signals*
1	**3.3 V**
2	GND
3	GND
4	VCC

P3 Cable Connections

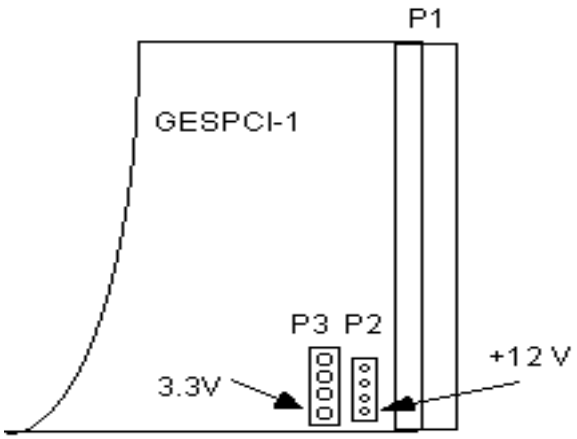


Figure 2.2 GESPCI-1 board implant

Connector P4 - VCC and GND for PCIMPU-56 and SOFT RESET

See P11 connector for PCIMPU-56.

Connector P6 - +3.3V and GROUND for PCIMPU-56 and additional signals for ISA bridge

See P10 connector for PCIMPU-56.

Connector P5 & P7 - PC/104 connector

The PCIMPU-56 module interconnects directly to the PC/104 bus (8 and 16 bit interface). For more information on the PC104 bus please refer to the PC/104 reference manual and see the PC-104 and PCIMPU-56 connectors description.

Connector P8 - IRDA connector

This connector is used to plug an external IRDA module. This facility is very useful in industrial system for collecting data, maintenance information and software upgrade.

Pin	Signals
1	GND
2	IrRX (input)
3	IrTX(output)
4	VCC (5V)

Connector P9 - Keyboard Lock

P9	Function
OFF	KBD unlocked
ON	KBD locked

Connector P10 - COM1 (HE10 Connector)

Pin	Signal Name
1	DCD
2	DSR
3	Serial In - (SIN)
4	RTS
5	Serial Out - (SOUT)
6	CTS
7	DTR
8	RI
9	GND
10	N.C.

Connector -P15 - COM2 (DB9 male Connector)

Pin	Signal Name
1	DCD
2	Serial In - (SIN)
3	Serial Out - (SOUT)
4	DTR
5	GND
6	DSR
7	RTS
8	CTS
9	RI
10	N.C.

Connector P11 - LCD Flat Panel Connector

P11 Pin n°	Signal name	LCD CONNECTOR	Signal Name	Pin Description
1	VDDSAFE	28,29	+5V Power	+5 or +3V (depend of J3)
2	+12VSAFE			+12V for BACKLIGHT DC/DC
3	VEESAFE			+ or - (0 to 40V max) (with R14) for monochrome LCD
4	NC			
5	ENABKL			Enable Backlight Output
7	M	27	Hor display Pos	BLANKING
8	NC			
10	LP	3	Hsync	Flat panel equivalent of HSYNC
11	FLM	4	Vsync	Flat panel equivalent of VSYNC
13	SHFCLK	2	Clock	Pixel Clock for flat panel Data
15	P0 (UD3)			8 ,9,12,16,18,24-bit flat panel data output
16	P1 (UD2)			
18	P2 (UD1)	20	B0	
19	P3 (UD0)	21	B1	
21	P4 (LD3)	22	B2	
22	P5 (LD2)	23	B3	
24	P6 (LD1)	24	B4	
25	P7 (LD0)	25	B5	
27	P8			
28	P9			
30	P10	13	G0	
31	P11	14	G1	
33	P12	15	G2	
34	P13	16	G3	
36	P14	17	G4	
37	P15	18	G5	
39	P16			
40	P17			
42	P18	6	R0	
43	P19	7	R1	
45	P20	8	R2	
46	P21	9	R3	
48	P22	10	R4	
49	P23	11	R5	
6,9,12,50, 14,17,20, 23,26,29, 32,35,38, 41,44,47	GND Ground Return and Shield	1,5,12,19 26	GND GROUND RETURN and SHIELD	

Connector P11 provides all interface signals for driving most flat panel displays. Power supply for Bias or Backlight are provided. Currently no display cables are provided by GESPAC. Contact GESPAC for cable and Video BIOS information.

Connector P12 - Floppy disk interface

Signal Name	Pin	Pin	Signal Name
Ground	1	2	FDHDIN
Ground	3	4	Reserved
Key	5	6	FDEDIN
Ground	7	8	Index-
Ground	9	10	Motor Enable A-
Ground	11	12	Drive Select B-
Ground	13	14	Drive Select A-
Ground	15	16	Motor Enable B-
Ground	17	18	DIR-
Ground	19	20	STEP-
Ground	21	22	Write Data-
Ground	23	24	Write Gate-
Ground	25	26	Track 00-
Ground	27	28	Write Protect-
Ground	29	30	Read Data-
Ground	31	32	Side 1 Select-
Ground	33	34	Diskette Change-

Connector P13 - LPT1

Signal Name	Pin	Pin	Signal Name
STROBE-	1	2	AUTO FEED-
Data Bit 0	3	4	ERROR-
Data Bit 1	5	6	INIT-
Data Bit 2	7	8	SLCT IN-
Data Bit 3	9	10	Ground
Data Bit 4	11	12	Ground
Data Bit 5	13	14	Ground
Data Bit 6	15	16	Ground
Data Bit 7	17	18	Ground
ACJ-	19	20	Ground
BUSY	21	22	Ground
PE (Paper End)	23	24	Ground
SLCT	25	26	N.C.

Connector P14 - PS/2 Keyboard

Pin	Signal Name
1	Data
2	nc
3	GND
4	VCC fused
5	Clock

Adaptor Cable for standard Keyboard is available from GESPAC.

Connector P16 - VGA CRT Connector

This 15-pin mini SUB-D female connector provides standard pin assignment for video adapter.

Pin	Signal Name
1	ROUT
2	GOUT
3	BOUT
13	HSYNC
14	VSYNC
4,5,6,7,8,10,11	GND

2.5 FUNCTIONAL DESCRIPTION

2.5.1 CPU

The PCISYS-56 dual-board system is designed to operate with 3.3 volt Pentium processors. An external voltage regulator circuit provides the required 3.3 volts from the 5 volt Power provided by a standard PC power supply. The processor board supports the Pentium processors at 75 to 200 MHz. The Pentium processor is backward-compatible with the 8086, 80286, i386^{TM} and i486^{TM} CPUs. It supports both read and write burst mode bus cycles, and includes separate 8K on-chip code and data memory caches which employ a write-back policy. Also integrated into the Pentium processor is an advanced numeric coprocessor which significantly increases the speed of floating point operations, while maintaining backward compatibility with i486DX math coprocessor and complying to ANSI/IEEE standard 754-1985.

2.5.2 PERFORMANCE UPGRADE

A 320-pin Type 5 Zero Insertion Force socket provides users with a processor performance upgrade path.

2.5.3 SYSTEM MEMORY

The PCIMPU-56 CPU board provides two 72-pin SIMM sockets for memory expansion. The sockets support 1M x 32 (4Mb), 2M x 32 (8Mb), 4M x 32 (16Mb), and 8M x 32 (32Mb) single-sided or double-sided SIMM modules. Minimum memory size is 8Mb and maximum memory size, using two 8M x 32 SIMM modules, is 64Mb. Memory timing requires 60Ns Fast-Page Mode devices or, for optimum performance, 60Ns EDO DRAM modules. Parity generation and checking is not supported. The two sockets are arranged as ROW HIGH and ROW LOW, and together provide a 64-bit wide data path. Both SIMMs must be of the same memory size and type and both sockets must be populated. There are no jumper settings required for the memory size or type, which is automatically detected by the system BIOS. Tin lead SIMMs are required to be used when adding Fast Page or EDO DRAM.

2.5.3.1 EDO DRAM

Extended Data Out (or Hyper Page Mode) DRAM is designed to improve the DRAM read performance. EDO DRAM holds the memory data valid until the next CAS# falling edge, unlike standard Fast-Page Mode DRAM which tri-states the memory data when CAS# negates to precharge for the next cycle. With EDO, the CAS# precharge overlaps the data valid time, allowing CAS# to negate earlier while still satisfying the memory data valid window time.

2.5.4 PCI (PERIPHERAL COMPONENT INTERCONNECT)

The Intel Triton 82430FX PCIset consists of the 82437FX Triton System Controller (TSC), two 82438FX Triton Data Path (TDP) devices, and one 82371FB PCI ISA /IDE Accelerator (PIIX) bridge chip.

2.5.4.1 82437FX Triton System Controller (TSC)

The 82437FX provides all control signals necessary to drive a second level cache and the DRAM array, including multiplexed address signals. It also controls system access to memory and generates snoop controls to maintain cache coherency. The TSC comes in a 208 pin QFP package.

2.5.4.2 82438FX Triton Data Path (TDP)

There are two 82438FX components which provide data bus buffering and dual port buffering to the memory array. Controlled by the 82437FX, the 82438FX devices perform all the necessary byte and word swapping required. Memory and I/O write buffers are included in these devices. The TDP devices are 100 pin QFP packages.

2.5.4.3 82371FB CompactPCI® PC/104/IDE Accelerator (PIIX)

The 82371FB provides the interface between the CompactPCI® and PC/104 buses and integrates a dual channel fast IDE interface capable of supporting up to 4 devices, seven type F DMA channels, five 16-bit timer/counters, two eight-channel interrupt controllers, CompactPCI® -to- AT interrupt mapping circuitry, NMI logic, PC/104 refresh address generation, and CompactPCI®/PC/104 bus arbitration circuitry together onto the same device. The PIIX comes in a 208 pin QFP package.

2.5.5 NATIONAL SEMICONDUCTOR 87306 SUPER I/O CONTROLLER

Control for the integrated serial ports, parallel port, floppy drive, RTC and keyboard controller is incorporated into a single National Semiconductor 87306. This component provides:

2.5.5.1 Two NS16C550-compatible UARTs with send/receive 16 byte FIFO

- Support for an IrDA compliant Infrared interface.

2.5.5.2 Multi-mode bi-directional parallel port

- Standard mode ; IBM and Centronics compatible
- Enhanced Parallel Port (EPP) with BIOS/Driver support
- High Speed mode ; Enhanced Capabilities Port (ECP) compatible

2.5.5.3 Industry standard floppy controller

- With 16 byte data FIFO (2.88 MB floppy support)

2.5.5.4 Integrated Real Time Clock

- Accurate within ±13 minutes/year

2.5.5.5 Integrated 8042 compatible keyboard controller

2.5.5.6 Keyboard Interface.

Configuration of these interfaces is possible via the CMOS Setup program that can be invoked during boot-up. The serial ports can be enabled as COM1, COM2, IrDA, or disabled. The parallel port can be configured as normal, extended, or disabled. The floppy interface can be configured for 720 Kb, 1.2 MB, 1.44 Mb, or 2.88 Mb 3½" media. Header pins located near the back of the board allow cabling to use these interfaces.

2.5.5.7 Real Time Clock (RTC)

The integrated Real Time Clock (RTC) is DS1287 and MC146818 compatible and provides a time of day clock, 100-year calendar with alarm features and is accurate to

within 13 minutes/year. The RTC can be set via the BIOS SETUP program.

2.5.5.8 CMOS RAM

The DS1287 includes 242-bytes of battery-backed CMOS RAM in two banks which is reserved for BIOS use. The CMOS RAM can be set to specific values or cleared to the system default values using the BIOS SETUP program. Also, the CMOS RAM values can be cleared to the system defaults by using a configuration jumper on the PCIMPU-56 CPU board.

2.5.5.9 Battery

An lithium style battery provides power to the RTC and CMOS memory. The battery has an estimated lifetime of seven years.

2.5.5.10 IrDA (InfraRed) Support

Serial port 2 can be configured to support an IrDA module via a 4 pin header connector. Once configured for IrDA, the user can transfer files to/from portable devices such as laptops, PDA's and printers using application software such as LapLink. The IrDA specification provides for data transfers at 115Kbps from a distance of 1-meter. A 4-pin header is provided to allow connection to a Hewlett-Packard HSDSL-1000 compatible Infrared transmitter/ receiver.

2.5.5.11 VGA VIDEO Controller

The CHIPS and Technology 65545 video graphic controller is 100% Hardware and Software compatible with the IBM standard VGA. Graphic BIOS is in 32Kbytes EPROM at C0000-C7FFF and is accessed via 8-bit internal data path. In terms of access time, no penalty is added since the chipset controller supports shadow memory on the video BIOS.

The video controller is equipped with 512Kb DRAM (optionally 1Mb.) The video buffer supports standard resolution from 640x480 and 800x600 in 256 Colors to 1024x768 in 16,256 Colors. In addition to the analog CRT interface, these chips support both monochrome and Color STN/TFT LCD panel interface and EL panels.

In addition the C&T 65545 offers a 32-bit graphic engine, Integrated programmable linear address, and hardware cursor, thus improving Windows performance. Other incorporated features, such as memory write buffer, and internal asynchronous display data FIFOs, also boost performance.

The programmable linear address feature is only possible with less than 12 Mbytes of system DRAM. GESPAC provides normal (65530) and linear (65545) Windows drivers.

2.5.5.12 FLASH Implementation

The Intel 28F001BXT 1 Mb FLASH component is organized as 128K x 8 (128 KB). The Flash device is divided into five areas, as described below.

System Address		FLASH Memory Area
FFB2BH	FFFFFH	BIOS
FF938H	FFB2AH	UTILS
FF16CH	FF937H	POST
FF0ADH	FF16BH	SETUP
FE000H	FEFFFH	Vacant

Table 2.3 Flash Memory Organization

The FLASH device resides in system memory in one 64 KB segment starting at F0000H, and can be mapped two different ways, depending on the mode of operation. In *Normal Mode,* address line A16 is inverted, setting the E000H and F000H segments so that the BIOS is organized as shown in the system address column above. *Recovery mode* removes the inversion on address line A16, swapping the E000H and F000H segments so that the 8 Kb boot block resides at FE000H where the CPU expects the bootstrap loader to exist. This mode is only necessary in the unlikely event that a BIOS upgrade procedure is interrupted, causing the BIOS area to be left in an unusable state. For information on recovering the BIOS in the event of a catastrophic failure, refer to Paragraph 3.4, "**Failsafe Recovery Preparation**".

2.5.6 SET-UP UTILITY

The ROM-based Setup utility allows the configuration to be modified without opening the system for most basic changes. The PCIMPU-56 CPU board also incorporates additional capabilities in the Flash EEPROM, including:
Auto configuration of IDE hard disks (manual selection of the drive type is no longer required). Support for ONE IDE disk interface provides access to two ATAPI IDE devices including CD-ROM readers. An option allowing the user to assign a block of addresses below the 1 Mb boundary as un-shadowed to allow for expansion card ROM which can cause timing problems when shadowed and cached. The default setting assigns this area as Vacant and not shadowed. (SEE in BIOS setup the SHADOW menu). Interrupts IRQ9, IRQ10 and IRQ11 (typically used for PCI) may be assigned to add-in card PC/104 adapters, thereby informing the CompactPCI® configuration utility which interrupts are not available. The Setup utility is accessed during the Power-On Self Test (POST) by pressing the

<ESC> key after the POST memory test has begun and before system boot begins. An option in BIOS setup can be set to prevent user access to Setup for security purposes. In other case the key sequence CTRL-ALT-<ESC> provide setup access during operating mode.

2.5.7 POWER MANAGEMENT

The PCIMPU-56 BIOS supports power management via System Management Mode (SMM) interrupts to the CPU The BIOS Energy management capabilities will allow the system to be put into a power managed standby state by:

1. Pressing a sleep/resume button, or
2. Expiration of the user configurable system inactivity timer (programmable in the SETUP BIOS)

Standby mode reduces power consumption to Energy Star levels by utilizing the power saving capabilities of the Pentium processor and turning off DPMS compliant monitors and hard drives. Standby mode also allows the system to be responsive to external interrupts.

2.5.8 POWER CONSUMPTION

The table below lists the current used by a typical system configured with 8Mb of DRAM, VGA controller and Floppy Drive while sitting at a DOS prompt. This information is preliminary and is provided only as a guide for calculating approximate total system power usage with additional resources added.

DC Voltage	75 MHz	90 MHz
+5V	3.3A	3.45A
+12V	75mA	75mA

PCIMPU-56 Current Requirements (Preliminary)

2.5.9 ENVIRONMENTAL

Operating temperature	0 to 50° Celsius
Storage temperature (package of origin)	-40 to 85° Celsius
Non-condensing relative	Less than 95% at 40° Celsius

2.6 USER-INSTALLABLE UPGRADES

2.6.1 SYSTEM MEMORY

The following table shows the possible memory combinations. The PCIMPU-56 will support both Fast Page DRAM or EDO DRAM SIMMs, but they cannot be mixed. Parity generation and detection is NOT supported. SIMM requirements are 60 Ns Fast Page Mode or 60 Ns EDO DRAM with tin-lead connectors.

SIMM Type (Size)	Total System Memory
Two 1M X 32 SIMMs (4Mb)	8Mb
Two 2M X 32 SIMMs (8Mb)	16Mb
Two 4M X 32 SIMMs (16Mb)	32Mb
Two 8M X 32 SIMMs (32Mb)	64Mb

Table 2.4 SIMM Memory Combinations

2.6.2 PCIMPU-56 MEMORY MAP

Address Range		Size	Note
(Decimal)	(HEX)		
1024K-131072K	100000-800000	127M	1
960K-1023K	F0000-FFFFF	64K	2
952K-959K	EE000-EFFFF	8K	
948K-951K	ED000-EDFFF	4K	
944K-947K	EC000-ECFFF	4K	
896K-943K	E0000-EBFFF	48K	
800K-895K	C8000-DFFFF	96K	3
640K-799K	A0000-C7FFF	160K	3
639K	9FC00-9FFFF	1K	4
512K-638K	80000-9FBFF	127K	5
0K-511K	00000-7FFFF	512K	6

Notes:

1. Extended Memory
2. System BIOS
3. Available HI DOS memory (open to PC/104 and CompactPCI® bus)
4. Extended BIOS Data (moveable by QEMM, 386MAX)
5. Extended conventional
6. Conventional

The table above details the PCIMPU-56 memory map. The ECSD area from ED000-EDFFF is not available for use as an Upper Memory Block (UMB) by memory managers. The area from E0000-EBFFF is currently not used by the BIOS and is available for use as UMB by memory managers. Parts of this area may be used by future versions of the BIOS to add increased functionality.

2.6.3 I/O MAP

Address (hex)	Size	Description
0000 - 000F	16 bytes	PIIX - DMA 1
0020 - 0021	2 bytes	PIIX - Interrupt Controller 1
0040 - 0043	4 bytes	PIIX - Timer 1
0060	1 byte	Keyboard Controller Data Byte
0061	1 byte	PIIX - NMI, speaker control
0064	1 byte	KBD Controller, CMD/STAT Byte
0070, bit 7	1 bit	PIIX - Enable NMI
0070, bits 6:0	7 bits	PIIX - Real Time Clock, Address
0071	1 byte	PIIX - Real Time Clock, Data
0078	1 byte	Reserved - Board. Config.
0079	1 byte	Reserved - Board. Config. RD Only
0080 - 008F	16 bytes	PIIX - DMA Page Register
00A0 - 00A1	2 bytes	PIIX - Interrupt Controller 2
00C0 - 00DE	31 bytes	PIIX - DMA 2
00F0	1 byte	Reset Numeric Error
0170 - 0177	8 bytes	Secondary IDE Channel
01F0 - 01F7	8 bytes	Primary IDE Channel
02F8 - 02FF	8 bytes	On-Board Serial Port 2
0376	1 byte	Sec IDE Channel Command Port
0377	1 byte	Sec IDE Channel Status Port
0378 - 037F	8 bytes	Parallel Port 1
03BC - 03BF	4 bytes	Parallel Port x
03F0 - 03F5	6 bytes	Floppy Channel 1
03F6	1 bytes	Primary IDE Channel Command Port
03F7 (Write)	1 byte	Floppy Channel 1 Command
03F7, bit 7	1 bit	Floppy Disk Change Channel 1
03F7, bits 6:0	7 bits	Primary IDE Channel Status Port
03F8 - 03FF	8 bytes	On-Board Serial Port 1
0CF8-0CFB*	4 bytes	CPCI Config Address Register
0CFC-0CFF*	4 bytes	CPCI Config Data Register
FF00-FF07	8 bytes	IDE Bus Master Reg.

2.6.4 PCIMPU-56 DMA MAP

DM	Size	System Resource
0	8- or 16-bits	Open
1	8- or 16-bits	Open - Normally used for LAN
2	8- or 16-bits	Floppy
3	8- or 16-bits	Parallel Port
4		Reserved - Cascade channel
5	16-bits	Open
6	16-bits	Open
7	16-bits	PC/104 IDE

2.6.5 PCIMPU-56 CompactPCI® CONFIGURATION SPACE MAP

The Triton chipset uses Configuration Mechanism 1 to access CompactPCI® configuration space. The CompactPCI® Configuration Address register is a 32-bit register located at CF8h, the CompactPCI® Configuration Data register is a 32-bit register located at 0CFCh. These registers are only accessible by full DWORD accesses. The table below lists the CompactPCI® bus and device numbers used by the external CPCI BUS.

Bus #	Dev #	Funct.	Description
(HEX)	(Dec)	(HEX)	
00	00	00	Intel 82437FX (TSC)
00	07	00	Intel 82371FB (PIIX) CPCI/PC-104 bridge
00	07	01	Intel 82371FB (PIIX) IDE Bus Master
00	14		CPCI Expansion Slot 1
00	15		CPCI Expansion Slot 2
00	16		CPCI Expansion Slot 3
00	17		CPCI Expansion Slot 4
00	18		CPCI Expansion Slot 5
00	19		CPCI Expansion Slot 6
00	20		CPCI Expansion Slot 7

2.6.6 PCIMPU-56 INTERRUPTS

IRQ	System Resource
NMI	PC-104 NMI, watchdog, or overtemp
0	Reserved, Interval Timer
1	Reserved, Keyboard buffer full
2	Reserved, Cascade interrupt from slave
3	Serial Port 2
4	Serial Port 1
5	User available(G96/PC-104) or Parallel
6	Floppy
7	Parallel Port 1
8	Real Time Clock
9	User available(G96/PC-104)
10	User available(G96/PC-104)
11	User available(G96/PC-104)
12	user available(G96/PC-104) or PS2
13	Reserved, Math coprocessor
14	Primary IDE if enabled, else available to
15	User available(G96/PC-104)

2.6.7 PLUG & PLAY BIOS

Plug & Play BIOS used on the PCIMPU-56 board has the following features:

Plug 'n Play card support
- Auto resource steering
- Win95 compatible

PCI and Bridge support
- Auto resource steering
- DEC PCI-PCI bridges
- Cogent PCI-PCI Ethernet

Energy Star power management
- APM for Windows and DOS
- VESA DPMS video management
- SMI and STPCLK, all X86's
- Timewarp correction

Fast-ATA support
- ATA Mode 4/5 (to 20 MB/S)
- Built-in IDE drivers (ADI2, CMD, OPTi, more)

Enhanced IDE support
- LBA and CHS translations
- EDPT Table support
- IBM/Microsoft INT13 extensions
- 8 discs max, each to 137 GByte
- Name any disc C:
- Boot SCSI (ahead of IDE)

RAID-0 Disc Striping
- Interleave 2-8 IDEs for astonishing throughput ATAPI and Removable IDE
- CD-ROM recognition
- SyQuest and Ejectable media Enhanced Floppy support
- 4 Floppy/tape-drives max
- Name any floppy A:

Enhanced Parallel Port
- SPP, Bidir, EPP and ECP modes

Upper Memory Blocks (UMB)
- Compact runtime core approx 24K
- Available runtime space approx 100K (of 128K)
- Compact total binary near 64K

Password
Security
Anti-Virus Protection
PS/2 Mouse support
Flash-ROM support
Instant! Boot

3. GETTING STARTED

3.1 GENERAL INFORMATION

The PCISYS-56 CompactPCI® industrial PC/AT consists of a PCIMPU-56 processor board equipped with a Plug and Play BIOS and a GESPCI-1 peripheral board. The keyboard, the communication ports and the video connections are straightforward. The user needs only a 40-pin flat cable for the IDE hard disk and a PC/AT compatible floppy disk cable equipped with one or two drive connections in order to complete the system.

WARNING: Jumper J15 (GESPCI-1) position 1-2 must be shorted to provide back-up power to the Real-Time Clock from the on-board battery.

3.2 CPU UPDATE

In order to update the CPU, you must change the clock speed and the PLL multiplying factor according to the CPU selected.

Speed (MHz)			PLL Mult.		
Pentium	Bus	CPCI	factor	J12	J13
75	50	25	1.5	on	on
90	60	30	1.5	off	on
100	66	33	1.5	on	off
100	50	25	2	off	on
120	60		1.5	off	on
133	66		2	on	off
150	60		2.5	off	on
166	66		2.5	on	off
200	66	33	3	on	off

3.3 THE BIOS UPDATE UTILITY

3.3.1 MR_ZAPPA SYSTEM BIOS AND FLASH UPLOAD UTILITY

Three files are included in this distribution kit:

MR_ZAPPA.BIO - MR BIOS ® System BIOS
MR_ZAPPA.EXE - Flash Loader Utility
AUTOEXEC.BAT - For Flash-Recovery disk

The System BIOS file contains the Microid Research BIOS ("MR BIOS ®"), customized for your PCIMPU-56. The 1995 MR BIOS ® core provides the latest state-of-the-art BIOS technologies that automate most of your computer's setup and deliver unmatched performance and utility.

Unlike most programs that you are familiar with, the System BIOS does not execute from disk. Instead, it is stored in a Flash-ROM component that resides on the PCIMPU-56 and begins executing immediately upon powerup. This Flash-ROM can be reprogrammed by means of a Flash Loader Utility. In order to install MR BIOS ® in your computer, you'll need to reprogram its Flash-ROM through use of the MR_ZAPPA.EXE Flash Loader.

The Flash Loader Utility is simple to use, and performs its job very quickly. Select option "3. Install" to initiate the Flash upload procedure. After it completes the Flash upload, it will direct you to reset the computer or re-cycle its power. Upon doing so, you will be greeted with an alarming message that the "CMOS Memory is Corrupt", and the BIOS Setup Utility will be activated. This is normal. The Flash Loader Utility clears the CMOS to simulate a factory-new condition and provoke a Setup session.

Upon arriving in the Setup Utility, you will need to reset the time and date, and manually input the types of Floppy drives in your computer. Beyond that, everything else will already be set for optimal performance and you can simply exit by pressing <F10>. Or, you might browse around and tailor some options like Password Security or Power Management per your preference. After this Setup session, your computer should reboot thereafter without the "CMOS Memory is Corrupt" error message.

Be advised that there is an element of danger in reprogramming the computer's Flash System BIOS. If the Flash Load procedure does not complete for some reason (for example, if the power is shut off in the middle of the procedure), or if the binary image being uploaded into the Flash-ROM is not appropriate, then the computer will simply not operate correctly (or at all). For this reason, your PCIMPU-56 board implements a failsafe recovery mode that can reload the original BIOS image from floppy diskette, even when the existing System BIOS is faulty. Please be sure to read the following section, “Failsafe Recovery Preparation”, before uploading the MR BIOS ® System BIOS.

3.4 FAILSAFE RECOVERY PREPARATION

The PCIMPU-56 board Flash-ROM contains a protected "Boot-Block" that cannot be erased. Its purpose is to provide failsafe recovery code that reloads the Flash-ROM in the event it somehow becomes corrupted. Under normal conditions, there should never be occasion to activate the failsafe recovery mode. However, as a precaution you should be aware of this facility, and prepare a recovery diskette in advance.

Step 1
Format a floppy with the "/S" switch to make it bootable: “FORMAT A:/S”

Step 2
Copy the contents of this distribution kit to the floppy. At minimum, the files AUTOEXEC.BAT and MR_ZAPPA.EXE need to be transferred onto it.

Step 3
Generate ZAPPA.BAK backup image file:

1. Run the MR_ZAPPA Flash Loader program directly from the floppy in drive A:.
2. Select option "1. Backup" upon entering the utility. This will copy the content of your computer's Flash-BIOS into the file ZAPPA.BAK.

Select “Option 5. Exit" to exit the program. Type DIR A: and confirm that ZAPPA.BAK was generated on the floppy in drive A:. (If not, you probably ran the program from drive C:, right? In this case, COPY the ZAPPA.BAK file onto the floppy).

Step 4
With this floppy in drive A:, reboot your computer via <Ctrl Alt Del>. If the floppy is prepared correctly, its AUTOEXEC.BAT file should put you directly into the MR_ZAPPA Flash Loader program.

Select option "2. Verify". This compares the Flash-BIOS in your computer with the backup file ZAPPA.BAK and reports the results.

Select option "5. Exit" to exit the program.

Step 5
Assuming the Step 4 verification is successful, the floppy is now fully prepared. Set the Write-Protect notch, label it, and put it away for safekeeping.

The recovery diskette should contain the following files:
1. DOS and COMMAND.COM
2. AUTOEXEC.BAT
3. MR_ZAPPA.EXE, the Flash Loader Utility
4. ZAPPA.BAK, the original BIOS backup image

3.4.1 MR BIOS ® INSTALLATION INSTRUCTIONS

Step 1
If you haven’t done so yet, prepare a Failsafe Recovery diskette according to instructions above.

Step 2
Invoke MR_ZAPPA.EXE Flash Loader, and select option "3. Install".
This loads the MR_ZAPPA.BIO file into Flash. Wait briefly for a message that indicates the procedure is completed. Then press the reset button or recycle your computer's power.

Be sure to wait for the completion message before resetting the computer.

Step 3
The first bootup after loading the new BIOS, you will be directed into the BIOS Setup Utility. Configure floppy drive(s) and other options.

Exit by pressing <F10>.

Step 4
Win95 Users: In a few installations, Windows 95 has been reported to "remember" certain properties of the BIOS that has been replaced by MR BIOS. This can lead to some bewildering behavior. The best rule of thumb is to unconditionally run Win95's "Add New Hardware” Wizard once after installing MR BIOS. If weirdness persists, use the sledge-hammer approach and run Win95's "Setup".

3.4.2 FAILSAFE RECOVERY - CORRUPTED FLASH BIOS

In the unlikely event that your PCIMPU-56 board Flash BIOS somehow becomes corrupted and the computer will no longer boot, you will need to reload its BIOS from the Failsafe Recovery diskette.

Begin by turning off all power, opening the PCISYS-56, and locating the J7/J10/J11 jumpers of the PCIMPU-56 board. Carefully using a small needle nose pliers, set the shorting jumpers for the RECOVERY mode as described below.

J10, pins 1-2
J11, pins 1-2
J7, pins1-2

Insert the Failsafe Recovery diskette in drive A:, then turn the power back on. The floppy drive's LED will illuminate and stay that way for a minute or so.

When drive A: LED turns back off, the Failsafe Recovery procedure is completed and the Flash BIOS is restored. Shut off the computer's power and replace the shorting jumpers J7/J10/J11 in the normal operation position:

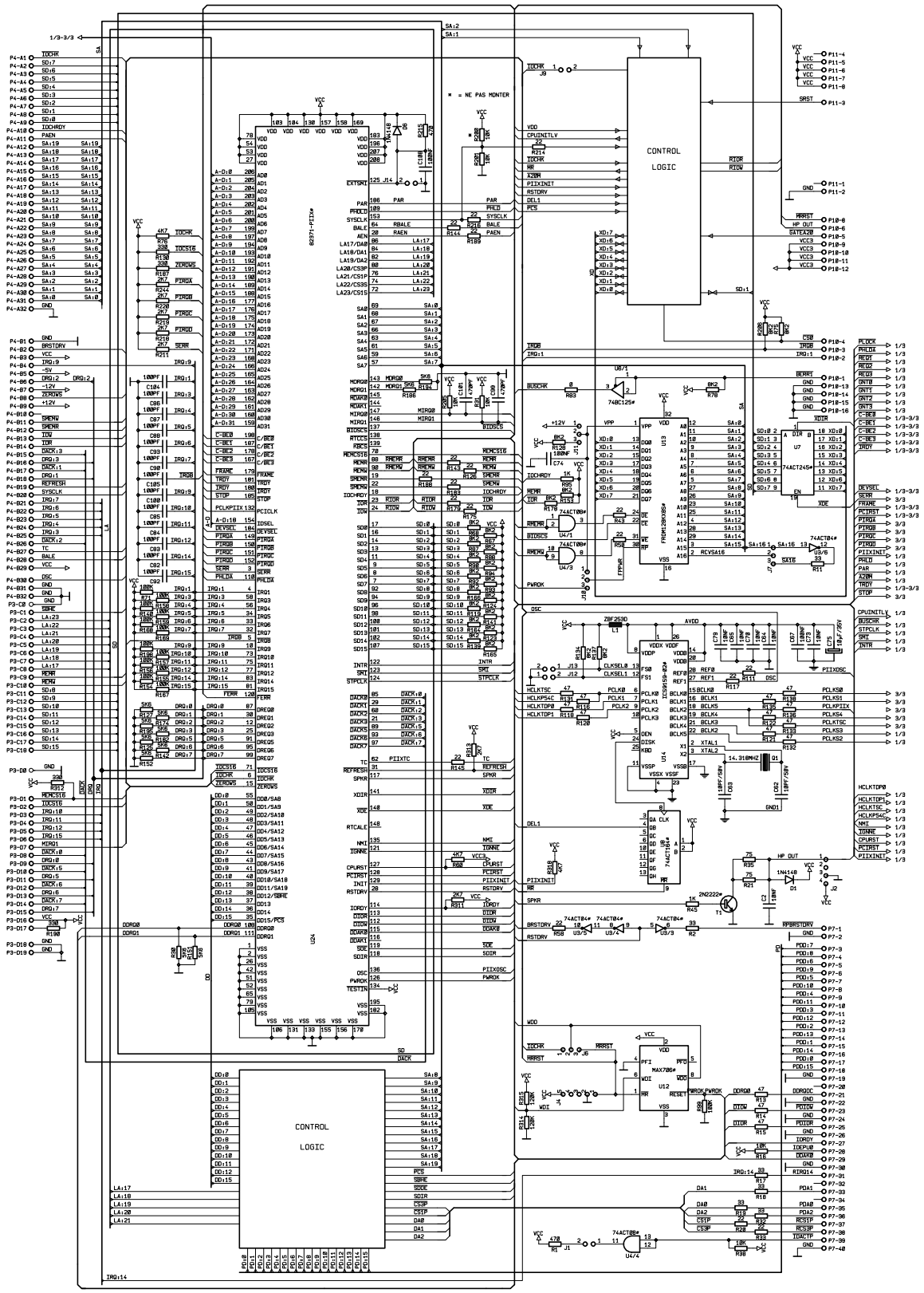
J10, pins 2-3
J11, pins 1-2
J7, pins 2-3

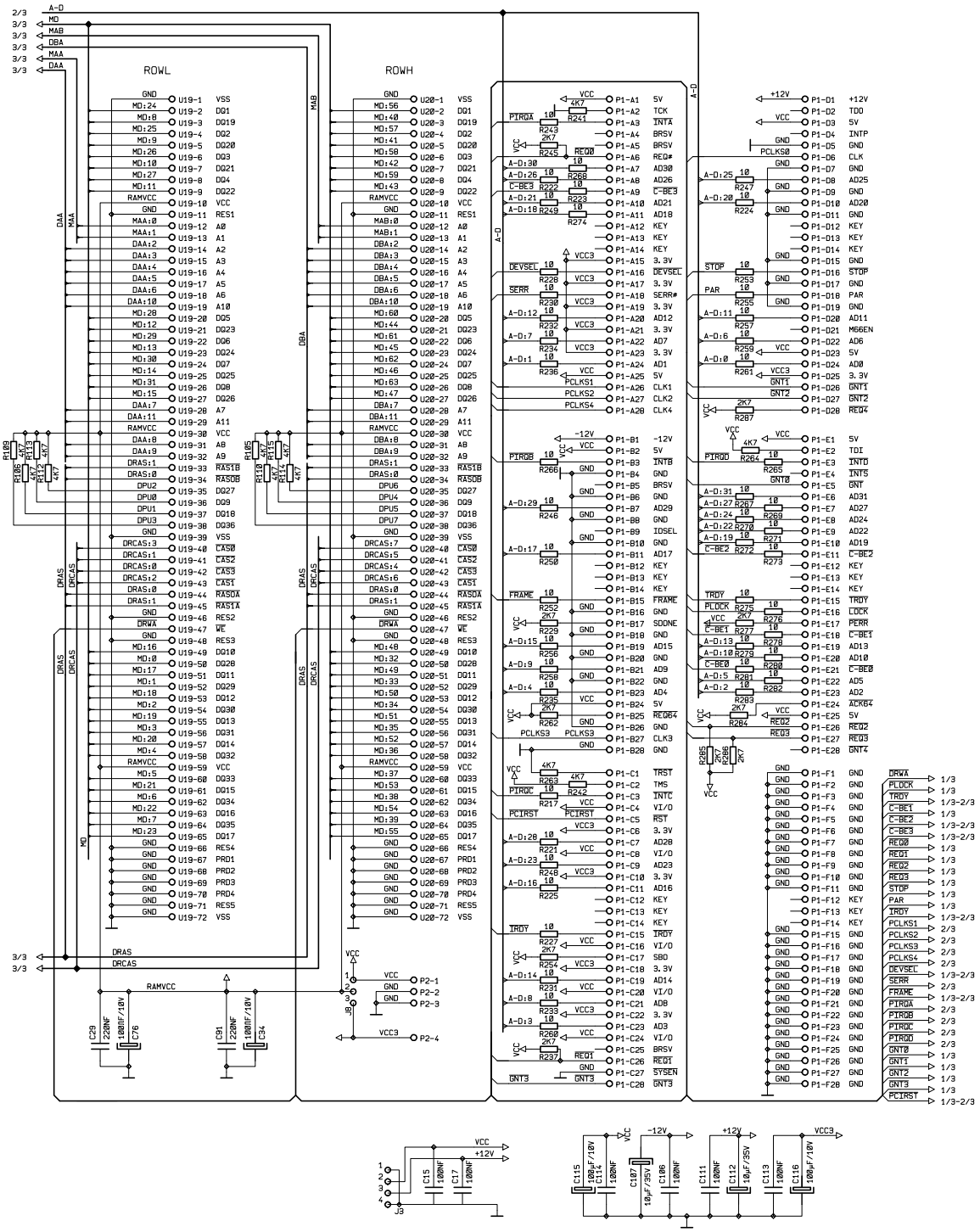
Note: When the Recovery Diskette is booted, the MR_ZAPPA.EXE Flash Loader is invoked. When run, it checks the status of the recovery jumpers and automatically executes the "4 Restore" option. If the jumpers are set for Normal Mode the menu is presented and MR_ZAPPA waits for your manual input).

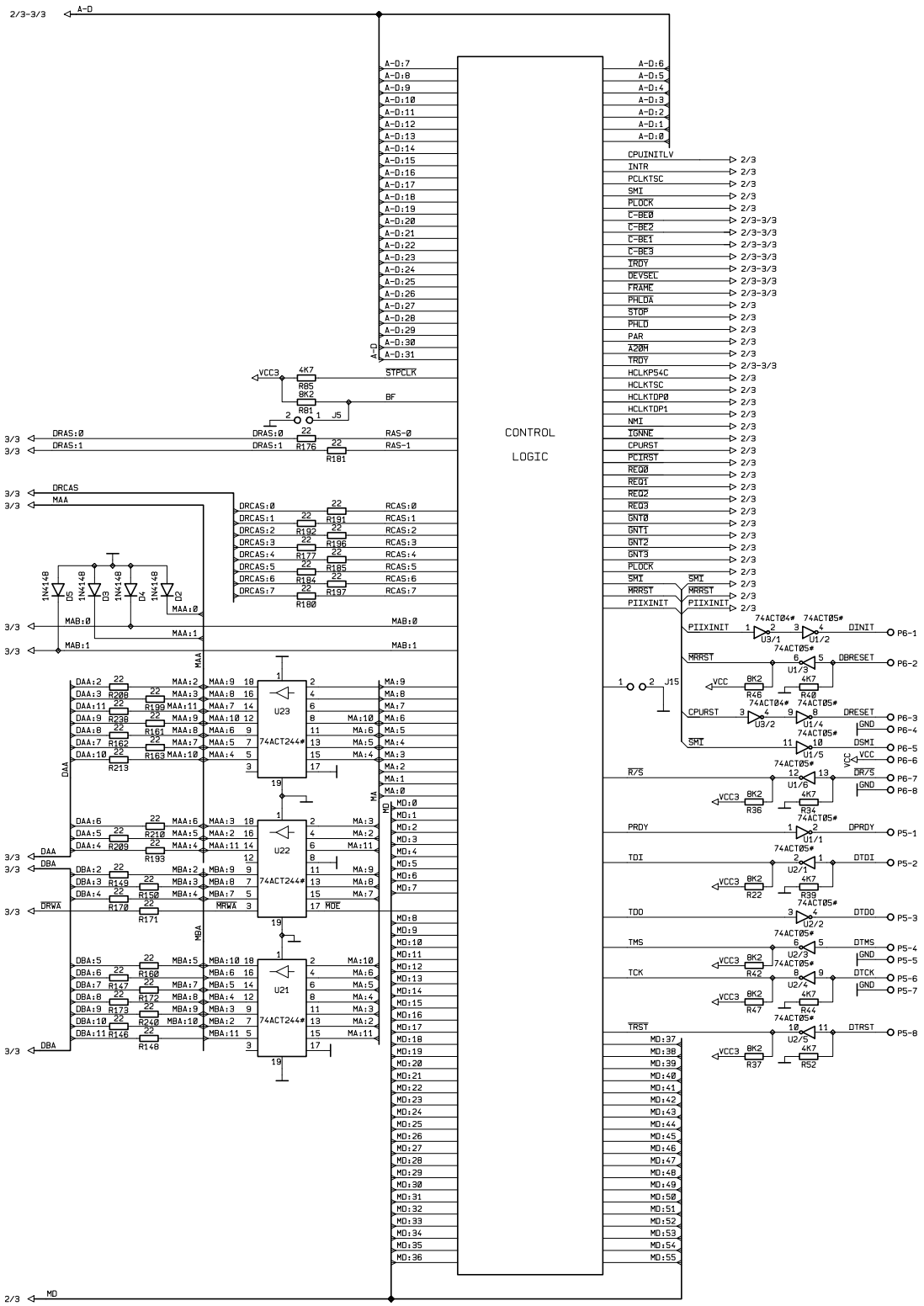
3.5 PRECAUTION FOR USE

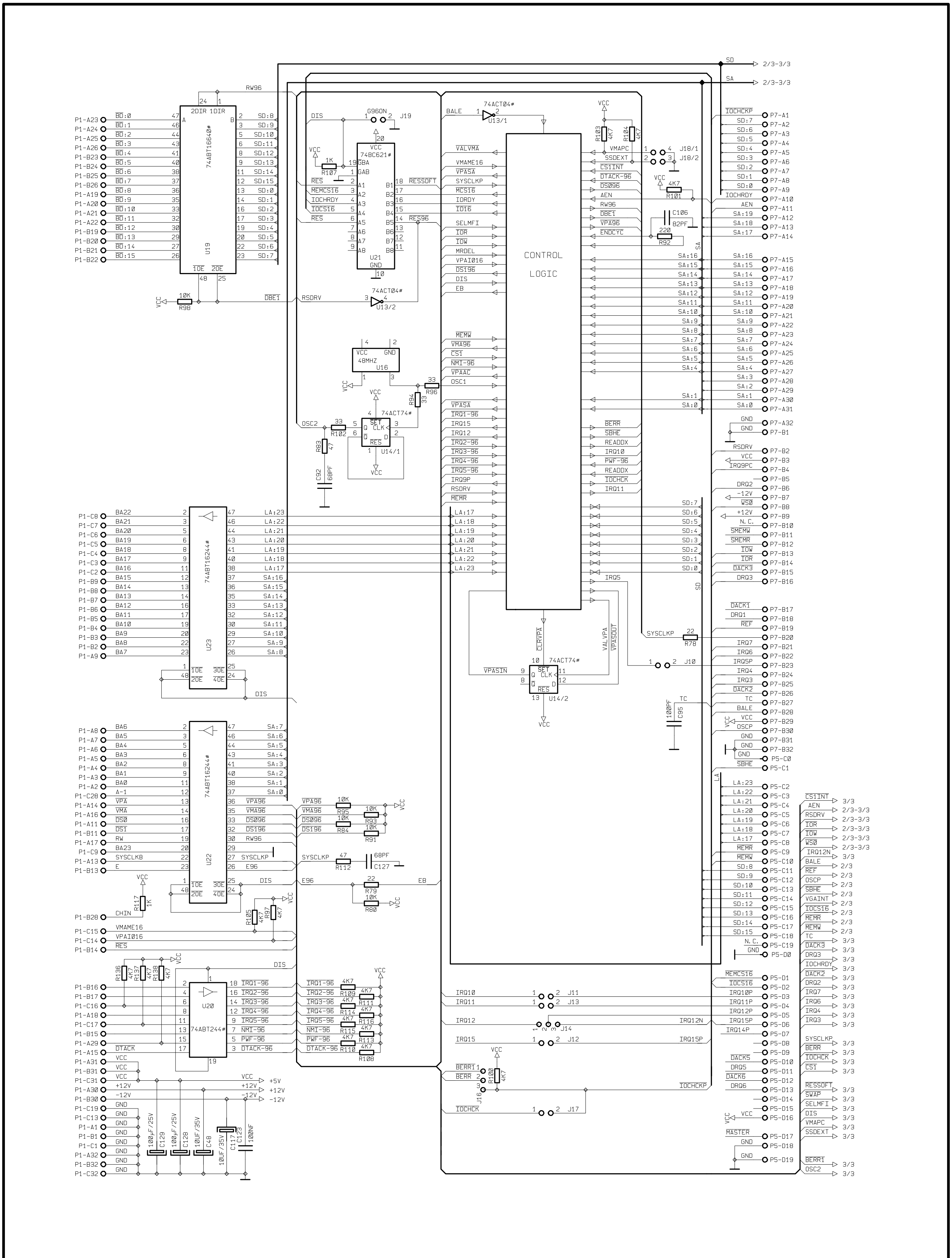
Due to the high integration of the PCISYS-56, it is necessary to provide a good airflow for cooling this module. The Pentium processor is designed to operate with a case temperature between 0-70ºC. The integral fan unit on top of the Pentium chip effects a 20-degrees difference between ambient temperature and case temperature. You must not exceed an ambient temperature of 50 degrees.

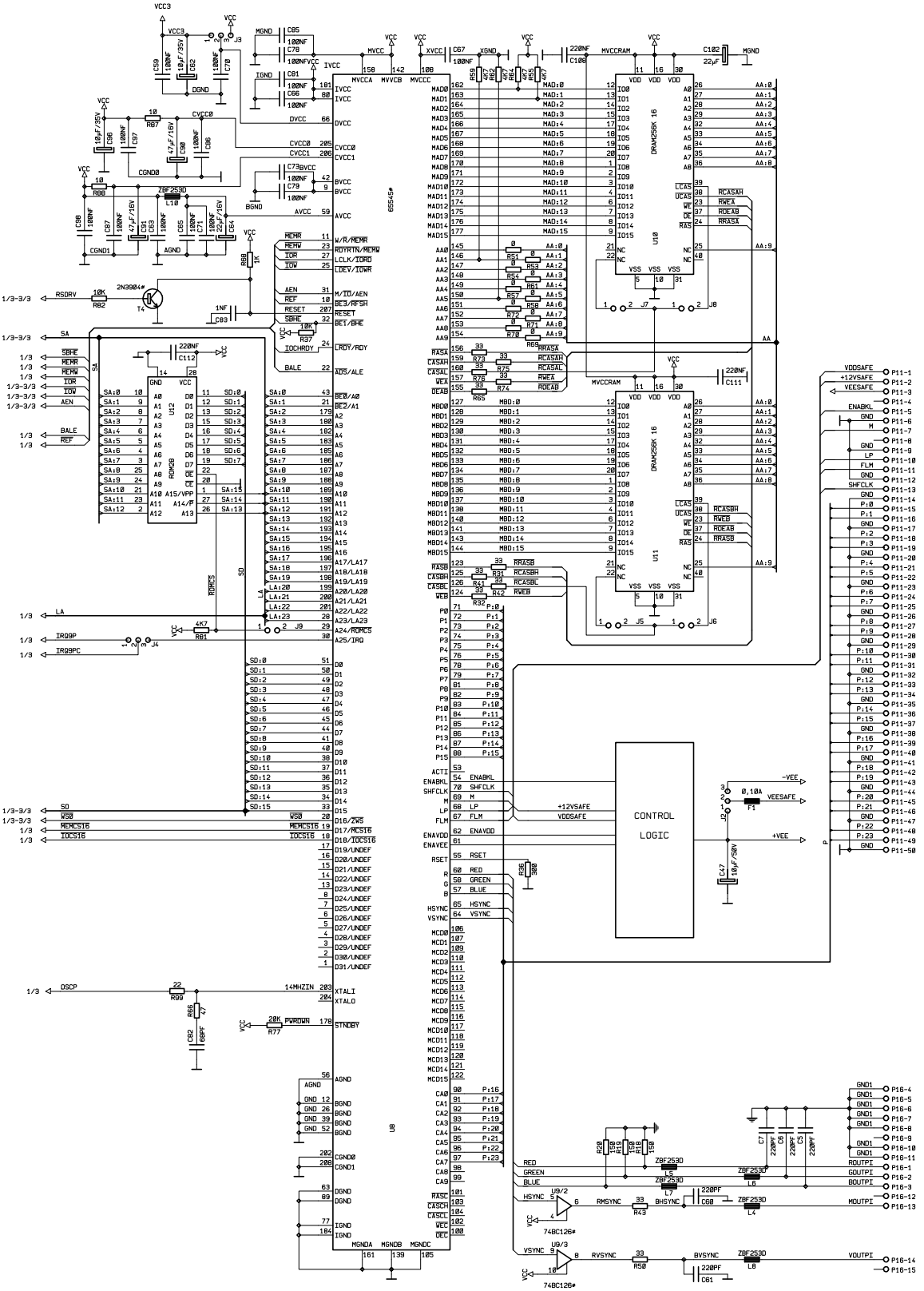
If these conditions are not respected, the warranty of the board is lost.

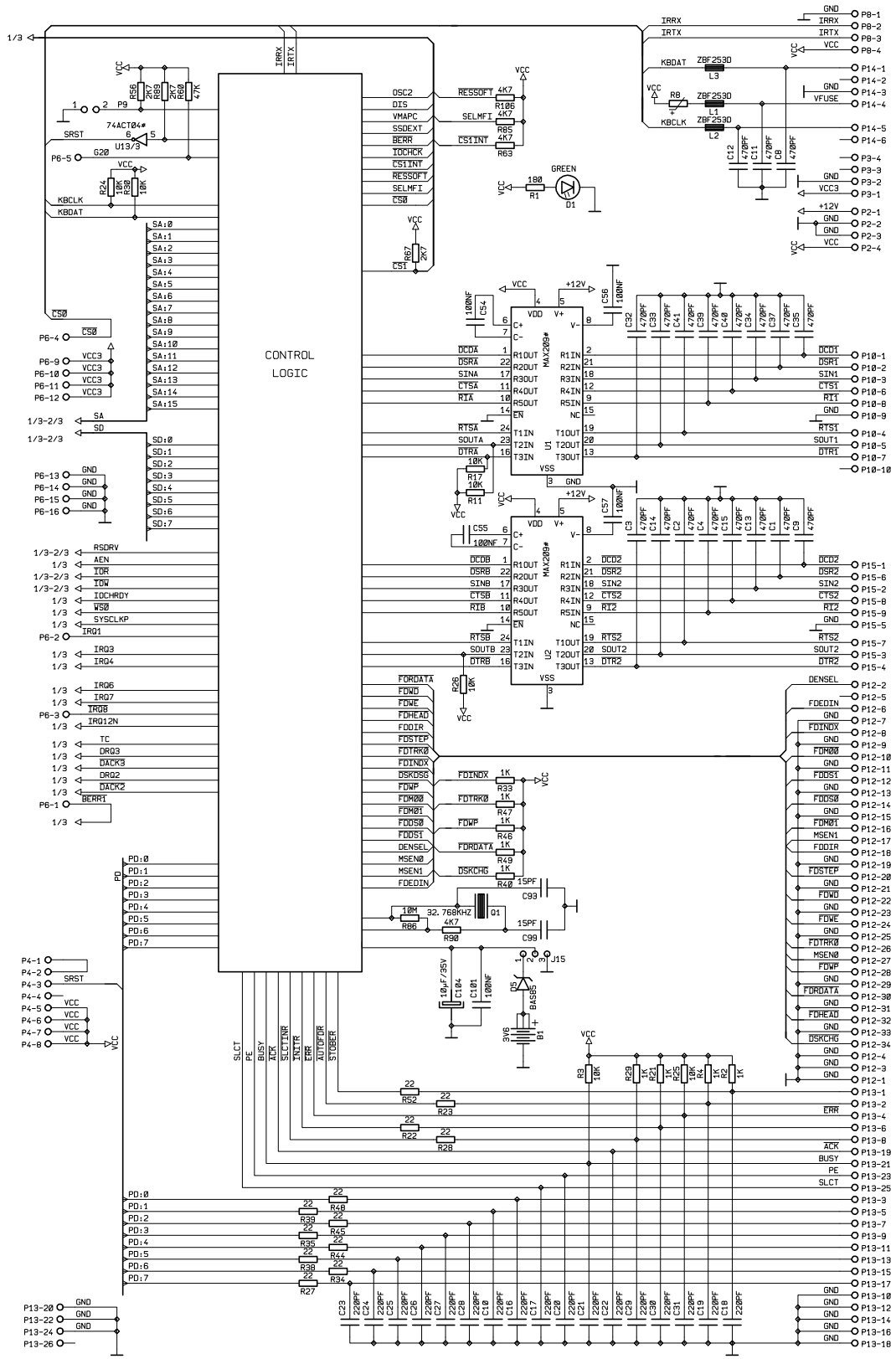



ROWL
ROWH
A-D
MD
MAB
DBA
MAA
DAA
DRAS
DRCAS
RAMVCC
VCC
VCC3
+12V
-12V
J8
J9
C29 220NF
C76 100NF/10V
C31 220NF
C34 100NF/10V
C15 100NF
C17 100NF
C115 100µF/10V
C114 100NF
C107 10µF/35V
C106 100NF
C111 100NF
C112 10µF/35V
C113 100NF
C116 100µF/10V


CONTROL
LOGIC
A-D
MD
MAA
MBA
DAA
DBA
MA
U23
U22
U21
74ACT244#
U3/1
U1/2
U1/3
U3/2
U1/4
U1/5
U1/6
U2/1
U2/2
U2/3
U2/4
U2/5
74ACT04#
74ACT05#
J5
J15
VCC3
VCC
GND
STPCLR
BF
DRAS:0
DRAS:1
RAS-0
RAS-1
DRCAS
MAA
MAB:0
MAB:1
DRCAS:0
DRCAS:1
DRCAS:2
DRCAS:3
DRCAS:4
DRCAS:5
DRCAS:6
DRCAS:7
RCAS:0
RCAS:1
RCAS:2
RCAS:3
RCAS:4
RCAS:5
RCAS:6
RCAS:7
1N4148
D5
D3
D4
D2
MRWA
MOE
CPUINITLV
INTR
PCLKTSC
SMI
PLOCK
C-BE0
C-BE2
C-BE1
C-BE3
IRDY
DEVSEL
FRAME
PHLDA
STOP
PHLD
PAR
A20M
TRDY
HCLKP54C
HCLKTSC
HCLKTDP0
HCLKTDP1
NMI
IGNNE
CPURST
PCIRST
REQ0
REQ1
REQ2
REQ3
GNT0
GNT1
GNT2
GNT3
PCLOCK
SMI
MRRST
PIIXINIT
DINIT
DRESET
DSMI
DR7S
DPRDY
DTDI
DTDO
DTMS
DTCK
DTRST
R7S
PRDY
TDI
TDO
TMS
TCK
TRST
P6-1
P6-2
P6-3
P6-4
P6-5
P6-6
P6-7
P6-8
P5-1
P5-2
P5-3
P5-4
P5-5
P5-6
P5-7
2/3
2/3-3/3
3/3


CONTROL LOGIC
74ABT16640#
U19
74BC621#
U21
74ACT04#
U13/1
U13/2
48MHZ
U16
74ACT74#
U14/1
U14/2
74ABT16244#
U23
U22
74ABT244#
U20
SD 2/3-3/3
SA 2/3-3/3
J10
J11
J12
J13
J14
J16
J17
J18/1
J18/2
J19
+5V
+12V
-12V


CONTROL
LOGIC
DRAM256K 16
74BC126#
ROM28
ZBF2530
MVCCRAM
VCC3
VCC
VCCA
VCCB
VCCC
MVCC
XVCC
IVCC
DVCC
CVCC0
CVCC1
BVCC
AVCC
CGND0
CGND1
AGND
BGND
DGND
IGND
MGNDA
MGNDB
MGNDC
XGND
MGND
SA
SD
LA
AA
MAD0
MAD1
MAD2
MAD3
MAD4
MAD5
MAD6
MAD7
MAD8
MAD9
MAD10
MAD11
MAD12
MAD13
MAD14
MAD15
MBD0
MBD1
MBD2
MBD3
MBD4
MBD5
MBD6
MBD7
MBD8
MBD9
MBD10
MBD11
MBD12
MBD13
MBD14
MBD15
RSDRV
SBHE
MEMR
MEMW
IOR
IOW
AEN
BALE
REF
IRQ9P
IRQ9PC
OSCP
14MHZIN
XTALI
XTALO
PWRDWN
STNDBY
RESET
RSET
RED
GREEN
BLUE
HSYNC
VSYNC
RMSYNC
BHSYNC
BVSYNC
RVSYNC
ENABKL
SHFCLK
VDDSAFE
+12VSAFE
VEESAFE
-VEE
+VEE
VOUTPI
ROUTPI
GOUTPI
BOUTPI
MOUTPI


CONTROL
LOGIC
MAX209#
U1
U2
Q1
32.768KHZ
D1
GREEN
D5
BAS85
B1
3V6
J15
P9
U13/3
74ACT04#
SRST
IRRX
IRTX
KBCLK
KBDAT
ZBF253D
VFUSE
VCC3
+12V
SA
SD
RSDRV
AEN
IOR
IOW
IOCHRDY
WS0
SYSCLKP
IRQ1
IRQ3
IRQ4
IRQ6
IRQ7
IRQ8
IRQ12N
TC
DRQ3
DACK3
DRQ2
DACK2
BERRI
FDRDATA
FDWD
FDWE
FDHEAD
FDDIR
FDSTEP
FDTRK0
FDINDX
DSKCHG
FDWP
FDM00
FDM01
FDDS0
FDDS1
DENSEL
MSEN0
MSEN1
FDEDIN
SLCT
PE
BUSY
ACK
SLCTINR
INITR
ERR
AUTOFDR
STROBER
RESSOFT
SELMFI
CS1INT
CS0
CS1
OSC2
DIS
VMAPC
SSDEXT
BERR
IOCHCK
DCDA
DSRA
SINA
CTSA
RIA
RTSA
SOUTA
DTRA
DCDB
DSRB
SINB
CTSB
RIB
RTSB
SOUTB
DTRB
DCD1
DSR1
SIN1
CTS1
RI1
RTS1
SOUT1
DTR1
DCD2
DSR2
SIN2
CTS2
RI2
RTS2
SOUT2
DTR2

Notes

Notes

INTERNATIONAL
Gespac S.A.
18, chemin des Aulx
1228 Geneva
Switzerland
Tel. +41 (22) 706 21 00
Fax +41 (22) 794 64 77

USA
Gespac Inc.
50 W. Hoover Ave.
Mesa, AZ 85210
1-800-4-GESPAC
Tel. +1 (602) 962 5559
Fax +1 (602) 962 5750

FAR EAST
Gespac Co, Ltd.
Minami Aoyama 1-15-18
Minato-ku
Tokyo 107-0062 Japan
Tel. +81 (3) 3470 0640
Fax +81 (3) 3478 8648

FRANCE
Gespac Systemes S.A.
Les Algorithmes
Bât. Epicure
91194 Saint Aubin Cedex
Tel. +33 (1) 69 85 33 73
Fax +33 (1) 69 85 36 60

GERMANY
Gespac GmbH
Langstrasse 76
63450 Hanau
Tel. +49 (0) 6181 24052
Fax +49 (0) 6181 24051

Printed in Switzerland