

DRAGON EISA
486

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REVISION: 1.2

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RADIO FREQUENCY INTERFERENCE STATEMENT

This equipment generates and uses radio frequency energy and if not installed and used properly, that is, in strict accordance with the manufacturer's instructions, may cause interference with radio and television reception.

If this equipment does cause interference to radio or TV reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- * Reorient the receiving antenna.*
- * Relocate the computer away from the receiver.*
- * Move the computer away from the receiver.*
- * Plug the computer into a different outlet so that computer and receiver are on different branch circuits.*
- * Ensure that card slot covers are in place when no card is installed.*
- * Ensure that card mounting screws, attachment connector screws, and ground wires are tightly secured.*
- * If peripherals are used with this system, it is suggested to use shielded, grounded cables, with in-line filters if necessary.*

If necessary, the user should consult the dealer service representative for additional suggestions.

The manufacturer is not responsible for any radio or TV interference caused by unauthorized modifications to this equipment. It is the responsibility of the user to correct such interference.

Note

1. *Electronic components are sensitive to dust and dirt. Do inspect and clean the computer system regularly.*
2. *Turn off the power whenever you install or remove any connector, memory module and add-on card. Before turning on the power, make sure that all the connectors, memory modules and add-on cards are secured.*
3. *After power is on, wait for a minute. The system BIOS are going through a self-test during this period and nothing is shown on the screen. After the self-test, the system BIOS will initialize the display adaptor and show messages.*
4. *The SIMM sockets are fragile device. Do not force the SIMM modules into the sockets. It may break the locking latches.*

Preface

The manual provides information about the installation and maintenance of OCTEK DRAGON EISA motherboard. In-depth explanations of the functions of this motherboard are provided. In the appendix, the system BIOS setup and EISA configuration utility are explained.

The content in this manual is only for reference and is intended to provide the basic information for the general users. There are also technical information for hardware and software engineers.

In this manual, there are 4 chapters. Chapter 1 contains a brief introduction and specification of OCTEK DRAGON EISA motherboard. In the Chapter 2, the functions of DRAGON EISA are explained. It also outlines many advanced features of the CPU and the system architecture. Chapter 3 explains the installation of coprocessor, DRAM modules and jumpers. Technical information is provided in the Chapter 4.

System BIOS is described in the Appendix A. Information about EISA configuration utility is in Appendix B. Additional information is given in the Appendix C and D for maintenance purpose.

Table of Content

Chapter 1 **INTRODUCTION**

Chapter 2 **GENERAL FEATURES**

<i>Specification</i>	2-1
<i>Processor</i>	2-3
<i>External Cache</i>	2-7
<i>DRAM System</i>	2-10
<i>EISA BUS</i>	2-12

Chapter 3 **CONFIGURING THE SYSTEM**

<i>Configuring Weitek 4167 Coprocessor</i>	3-1
<i>Configuration of Cache Memory</i>	3-2
<i>Installing DRAM SIMM Modules</i>	3-4
<i>Configuration of Memory</i>	3-5
<i>DRAM Configuration</i>	3-6
<i>System Board Jumper Setting</i>	3-7
<i>System Board Connectors</i>	3-8

Chapter 4 **TECHNICAL INFORMATION**

	<i>Memory Mapping</i>	4-1
	<i>System Expansion Bus</i>	4-2
	<i>I/O Address Map</i>	4-
12		
	<i>System Interrupts</i>	4-
15		
	<i>Direct Memory Access (DMA)</i>	4-
17		
	<i>Real Time Clock and CMOS RAM</i>	4-19
	<i>CMOS RAM Address Map</i>	4-20
	<i>Real Time Clock Information</i>	4-21

Appendix A **SYSTEM BIOS**

	<i>Self-Test</i>	A-1
	<i>System Setup</i>	A-4

Appendix B **EISA CONFIGURAITON UTILITY**

	<i>EISA System Configuration</i>	B-1
	<i>ECU for the Dragon EISA</i>	B-2
	<i>Installation of AMI ECU</i>	B-3
	<i>Operation of AMI ECU</i>	B-4

Appendix C **OPERATION AND MAINTENANCE**

<i>Static Electricity</i>	C-1
<i>Keeping The System Cool</i>	C-1
<i>Cleaning The 'Golden Finger'</i>	C-2
<i>Cleaning The Motherboard</i>	C-2

Appendix D **TROUBLESHOOTING**

<i>Main Memory Error</i>	D-1
<i>Cache Memory Failure</i>	D-1
<i>Improper Setting of Wait State</i>	D-2

Appendix E **SYSTEM BOARD LAYOUT**

Chapter 1

Introduction

The OCTEK DRAGON EISA system board is a low cost, high performance EISA system board which offers a true 32 bit platform where a 32-bit CPU is matched with a 32-bit EISA bus.

The OCTEK DRAGON EISA contains the powerful 80486 microprocessor which has 8K bytes of internal cache and an internal numeric coprocessor. The board adopts a highly integrated OPTI EISA 4 chipset which build in an advanced write back cache controller capable of bursting to cache size ranging from 64 KB to 512 KB.

Owing to 32 bit EISA bus, the board is able to sustain at a maximum of 33 MB/sec data transfer rate between peripherals attached to its slots. The high transfer rate means the board is suitable for those applications involving transfer of large volume of data, such as network file servers, engineering work-stations, workstation for software development, multi-user systems, some multi-media applications etc.

The board contains two banks of 32-bit high performance DRAMs using SIMM modules. It is capable of holding DRAM of total size from 4 MB to 128 MB of DRAMs without using memory expansion cards.

The board has been fully certified for compatibility and reliability under a vast number test environments. In particular, the board has been tested and found compatible with most EISA products available in the market.

Chapter 2

General Features

SPECIFICATION

Processor :

- *INTEL 80486 microprocessor with built-in 8KB internal cache and enhanced 80387 coprocessor*
- *WEITEK WTL-4167 coprocessor socket*

Cache :

- *8 KB four way set associative internal cache*
- *64 KB to 512 KB Interleaved, write back external cache*

Memory :

- *8 SIMM socket for 1 MB, 4 MB or 16 MB memory module*
 - *support 70 ns fast page mode DRAM*
 - *Maximum of 128 MB DRAM on board.*
 - *Page mode and hidden refresh*
 - *Shadow RAM for system and video BIOS*
-

GENERAL FEATURES

Slot :

- *8 EISA compatible slots that can support 8-bit and 16-bit AT bus add-on cards and EISA bus add-on cards.*
- *6 EISA slot available for EISA bus master*
- *maximum 33 MB/sec burst data transfer rate*
- *Auto-configuration for Add-on card setting*

System Support Functions :

- *Real time clock*
- *4 KB EISA CMOS RAM with battery back-up*
- *7 DMA channels for 8-, 16- or 32-bits DMA*
- *33 MB/sec DMA transfer rate*
- *Fast A20 gate and fast reset*

Other Features :

- *6 layer, baby AT size*
-

GENERAL FEATURES

PROCESSOR

The 80486 microprocessor is the state-of-art microprocessor which merges many innovative features on a single chip for advanced applications and operating systems. Fabricating with the 1 μ m process, this CPU consists of more than one million transistors. With such high density, this CPU incorporates as many as new features to make itself the most powerful microprocessor.

80486 is a 32-bit microprocessor with 32-bit external data bus and 32-bit external address bus. It not only contain a central processing but also integrates a numeric processor and a four-way set associate cache memory. It is fully binary compatible with 80386 and 80387. All existing software for PC XT/AT can be used on the DRAGON EISA. However, due to the new internal architecture, the performance of 80486 is two or four times of 80386.

The overall performance of computer system can be improved by cache memory. Nevertheless, if the cache memory is separated from CPU, CPU still needs to fetch code and data through external bus. That means the data transfer rate should not be too fast so that the external device are able to keep pace with the CPU. In 80486, the cache controller and cache memory are integrated into the chip. Most of the operations can be carried out inside the CPU, which reduces the bus operations on external data and address bus and thus speeds up the internal execution.

GENERAL FEATURES

The internal cache memory is a 8K bytes, 16 bytes line size, four-way set associative configuration. The hit rate of this configuration in a multitasking and multi-processor environment is much higher than 32K bytes two-way set associative external cache.

Bus snooping feature keeps the cache memory consistent with the main memory. When an external processor overwrites the content in main memory, the corresponding data in the internal cache memory will be invalidated and will be fetched from main memory when CPU reads this data.

When a read miss occurs, the CPU will initiate a burst mode read operation. In this operation, CPU performs four successive read operations each of which takes only one cycle. Total 128 bits data are fetched into the CPU's internal cache. Since burst mode read operation is very fast, the traffic of the CPU bus is greatly reduced and the bus is available to other bus masters, such as DMA controller.

Reading 128 bits data into CPU will take some times. In order to reduce the delay, the internal cache controller works parallel with CPU. It fetches the data needed by CPU for the present operation and the CPU read cycle is terminated. Then the other data are read into the internal cache memory while CPU is doing something else. This arrangement permits the CPU to run at zero wait state.

GENERAL FEATURES

By eliminating the access to external bus, operations with the internal cache can be completed in a single cycle. 80386 at least needs two cycles for an operation. To further increase the rate of data transfer inside the CPU, the internal bus of the cache memory is increased to 128 bits, which is four times of the external bus. Since, in most of the time, the CPU is using the internal cache, the large bus size substantially improves the overall performance.

When the CPU writes data to the main memory, the data is first stored in a write buffer. There are four write buffers. When the external bus is idle, data will be sent to main memory. If all buffers are filled, it can start write operation in burst mode. Since the internal cache is updated immediately, the CPU need not suspend its operation and there is no need to wait or the external device to update the main memory.

Many often-used instructions are executed in a clock cycle and some instructions are modified to take fewer cycles than in 80386. On the contrary, 80386 may take two to three more cycles for the same instruction. The CPU contains an advanced instruction pipeline structure and a 32-byte code queue to speed up the execution.

80486 includes all the functions of 80386 and is able to support sophisticated software and operation systems which are widely employed now. It is able to operate in real mode, protected mode and virtual 8086 mode.

GENERAL FEATURES

Internal memory management unit provides a flexible addressing scheme for the next generation operation system. Multitasking, concurrent operation and manipulating huge data base can be accomplished with excellent performance. Paging mechanism is employed to allow powerful operating system to implement virtual memory. Each segment is divided into several pages which are 4K bytes per page. Page mechanism is transparent to software and allows software to address 64 terabytes. Furthermore, the 64KB segment boundary which is an barrier of 8088 and 80286 is removed and the segment length can be increased up to 4GB.

The demand for sophisticated, number-crunching scientific and business applications has rapidly increased in recent years. In the past, microprocessor features an integer Arithmetic Logic Unit which only handles simple integer operations such as addition and multiplication. Floating point operations which are actually utilized by applications must be accomplished through software routines.

To meet the demand of floating-point calculation, a numeric coprocessor is necessary. However, an external coprocessor has been found to the bottleneck of data transfer. 80486 integrates the coprocessor on chip and thus the data transfer to external bus is eliminated. The on-chip coprocessor is compatible with 80387. It works parallel with other units in the CPU, which results in a better performance of numeric process.

GENERAL FEATURES

EXTERNAL CACHE

Although 80486 comes with 8 KB internal cache memory, there are many applications, such as those found in multi-user, multitasking, or multi bus master environments, the internal cache memory were found insufficient and cause system bottleneck. Thus, an external cache memory using an interleaved write back cache designed in the DRAGON EISA board to support upto 512 KB of external cache memory.

In a single user, single task environment, such as system running common DOS business applications, where only few megabytes memory is installed, the 80486 internal cache memory is able to provide adequate hit rate and the performance can still be very high.

In a multi-user or multitasking environments such as networking, UNIX server, CPU has to switch back and forth between tasks, a large amount of data is necessary to bring in and out of the cache, the 8K bytes internal cache memory is found to have low hit rate. The performance can be improved by adding an external cache memory to increase the overall hit rate. Owing to the randomness of the nature of memory reference found in multi-user or multi-tasking environments, the size of an external cache must be large enough to act as a big sponge to shelter the random accesses from hitting on the DRAM subsystem. Furthermore, as the size of main memory is increasing so as to hold more and more tasks in run time, the randomness of memory reference would increase substantially, a big external cache is more necessary.

In a system installed with one or more bus master devices other than CPU, the CPU has to share the DRAM with other masters. When other bus master is accessing the DRAM, the CPU is put in wait states if it also requires to access the DRAM. A cache memory allow CPU to

GENERAL FEATURES

continue to execute program out of the cache while the other bus master occupying the DRAM. Alternately, a cache memory reduces the CPU's utilisation onto the DRAM. The CPU is only put into wait state when it has to utilize the DRAM to exchange information between the cache and DRAM while other bus master is using it. This should be quite rare in a system having a good external cache memory design to minimize CPU utilisation onto DRAM. Thus, a cache memory can effectively decouple the CPU from the rest of bus master. The higher the hit rate, the better the write policy, the smaller the read miss penalty, the better is the decoupling effect.

The external cache of the DRAGON EISA board adopt a write back design. In a cache based system, when CPU perform a write operation, the content of cache would be different from that of DRAM if the operation is only perform to the cache. The cache content is said to be stalled. In some system, the CPU write operation is performed simultaneously to the DRAM as well as to the cache. Such write policy is termed as write-through and the performance of write operation is limited by the slow DRAM. In some system, the CPU write is performed to the cache as well as a buffer in the DRAM subsystem. The speed of the write operation is not limited to DRAM. Such design is called post-write. However, post-write cache design can only buffer a single write. If CPU perform more write operation before the buffered data has been stored onto DRAM, CPU is still put into wait states. In other systems, the DRAM subsystem has included several buffers to hold more continuous write operations. In a write-back cache design, CPU is performed only to the cache so that write operation is completed in the fastest manner. Data in cache is referred as dirty as soon as it is written by CPU. The dirty data is only put back to DRAM when the same cache location have to be re-used by a later read miss, by which new data is read from DRAM and stored in the cache.

Write-back design provide best write performance and lowest DRAM utilisation because CPU write data is

GENERAL FEATURES

only perform to the fast cache memory and only a fraction of dirty write data get to put back to DRAM. The low DRAM utilisation means the availability of DRAM to other bus master has been improved. In an EISA system, where more than one bus master device are often installed, the write-back cache design can improve the overall system performance.

GENERAL FEATURES

DRAM SYSTEM

The DRAGON EISA board can be installed with two banks of DRAM in its 8 SIMM sockets. The board support up to eight 1 MB, 4 MB or 16 MB SIMM module giving total DRAM size upto 128 MB. The DRAM should be fast-page mode DRAM with CAS before RAS refresh capability.

The DRAM subsystem provides a flexible memory configuration. Several combinations of DRAM type are allowed. The DRAM type and the memory size are automatically detected by the system BIOS. So, you may easily change the configuration of the system.

The DRAM controller supports page mode. The DRAM is divided into pages with equal size. Successive DRAM accesses within the same page need not require wait state. Furthermore, a burst line fill mode is implemented. In case of a read miss occurred in cache memory, 16 bytes data will be fetched from DRAM to the cache. The page mode operation can speed up the line fill operation. To enhance the system performance, shadow RAM is also supported. By shadow RAM, it means system BIOS and video BIOS contained in low speed EPROM are copied into DRAM. Improvement is significant because access to DRAM is much faster than EPROM. The DRAGON EISA board is able to copy the BIOS onto its cache memory to further improve the performance.

GENERAL FEATURES

The DRAM refresh logic is redesigned to improve the overall system performance and power consumption. In the original PC/AT design, the DRAM refresh operation will suspend the CPU operation because it has to access the DRAM. In high speed system like DRAGON EISA board, the CPU indeed can process a large amount of data during the DRAM refresh period.

By implementing hidden refresh, the refresh operations for expansion card on the EISA slot and for the DRAM are separated. To be compatible with AT bus add on card, the refresh operation for EISA bus is same as that found in the original PC/AT. But the refresh operation for the DRAM will be carried out individually and will be done when there is no access to the DRAM.

GENERAL FEATURES

EISA BUS

Since the inception eleven years ago, the growth of the business personal computer market has been driven to a substantial degree by the emergence of a de facto industry standard. This industry standard grew from the original IBM PC system architecture and evolved tremendously in the ensuing years. There are three key elements of this architecture: Intel 8086-family of microprocessors, an "open" I/O bus and the MS-DOS operating system.

The benefit of the industry-standard architecture (ISA) to the PC users have been enormous. ISA has provided a stable platform for software and hardware development which has given customers the largest selection of products in the history of computing. ISA has also facilitated the rapid utilization of the latest technology in PCs in a compatible manner, protecting the customers' investment. It has also freed customers from a single-vendor, proprietary architecture and for the first time, given customers real freedom of choice in selecting the best computers, software and peripherals to meet their needs. Over the last eleven years, ISA has become a customer-controlled standard rather than a vendor-controlled standard.

In this eleven year, each key elements of this industry-standard architecture has evolved significantly. In 1984, IBM introduced Intel's 80286 processor to personal computers and extended the existing 8-bit open I/O bus to 16-bit capabilities in a compatible manner. In 1986, fully compatible personal computers were introduced to the market using Intel's next generation microprocessor, the 386. At the processor subsystem level, the full 386 capabilities were harnessed, but without a compatible 32-bit extension to the ISA I/O bus. The 386 was introduced in this manner because of the enormous customer demand for higher processor performance. At the time, the 32-bit I/O bus extension was not needed since most of the I/O peripherals did not

GENERAL FEATURES

require the full performance of the 16-bit standard, let alone new 32-bit bus capabilities.

The introduction of this fully compatible 32-bit processor architecture has facilitated the timely development operating systems that take advantage of the 386 capabilities. Windows/386, XENIX/386 and a wide variety of 386-specific operating systems are currently available and providing a platform for application software development. A version of OS/2 (OS/2 2.0) that takes more complete advantage of the 386 architecture will probably be available by the time DRAGON EISA board reach its customer.

The combination of the 386 and 486 architecture and new operating system will drive 386 and 486-based PC into new, more demanding user applications and will increase the need to extend the ISA I/O bus to full 32-bit capabilities. As 386 and 486-based machines has already become the standard PC platform for business applications, a full-function 32 bit I/O bus will be more than necessary.

A number of industry leaders were working together to come up an extension to the industry standard architecture in 1989. The Extended Industry Standard Architecture (EISA) is both fully compatible with the vast installed base of ISA PCs and delivers the capabilities required to meet market needs by delivering high-performance 32-bit I/O capabilities. This bus architecture has been developed by industry leaders to assure its open availability to all interested parties, without any financial or technical constraints. In this way, the benefits of open industry standards will be delivered to the market in a way that will be optimal to customers.

Since its introduction, EISA was limited to be very "high end" applications where cost is not an issue. The main cause to limited application of EISA is the EISA motherboard and add on card were very expensive

GENERAL FEATURES

compared with their AT counter-part. Beginning from 1992, with the mass production of cost effective EISA motherboard and add on cards, it is expected that EISA to begin to assume its expected role and take part into all classes of applications that are expected to be benefit from the advance architecture.

EISA is a superset of the 16-bit AT bus. It extends the capabilities of that standard while maintaining compatibility with AT bus expansion card.

GENERAL FEATURES

EISA introduces the following major advances :

- *32-bit memory addressing for CPU, DMA and bus masters*
- *32-bit data transfers for CPU, DMA and bus masters*
- *allow high speed burst data transfer*
- *support intelligent bus master peripheral controllers*
- *enhanced DMA transfer rates*
- *33 MB/s data transfer rate for bus masters and DMA*
- *shareable interrupts, programmable for edge or level triggering-automatic configuration of system and expansion boards.*

EISA systems provide a number of DMA enhancements, including 32-bit addressability, 32-bit data transfers and higher data transfer rate. EISA DMA is backward compatible with AT bus and is a low cost alternative to an intelligent bus master and can be used for I/O peripheral that do not require local intelligent on the peripheral.

EISA based system support a bus master architecture for intelligent expansion cards. The bus master architecture provide a high speed data transfer rate upto 33 MB/s using EISA burst cycles. The bus master provides local intelligence by including a dedicated I/O processor and local memory. It can relieve the burden on the main CPU by performing sophisticated memory access functions, such as non-ordered scatter-gather data transfers. Examples of applications that might benefit from a 33 MB/s transfer rate and/or a bus master implementation include disk controllers, LAN controller, communication gateways, data acquisition systems, and certain classes of graphic controllers. Those applications might be found in network file servers, engineering workstations, workstation for software development, multi-user systems, some multi-media applications etc.

GENERAL FEATURES

EISA system provide level-triggered, shareable interrupts. Any EISA interrupt can be individually configured for level- or edge-triggered operation. Edge-triggered operation provides full compatibility with existing, interrupt-driven AT devices. Level-triggered operation facilitates the sharing of a single system interrupt by a number of devices. Level-triggered interrupts might be used, for example, to share a single interrupt between a number of serial ports.

EISA provides the capabilities for automatic configuration of system and expansion boards. EISA expansion boards should come with configuration files. The configuration files can be included with either new, fully programmable EISA boards or switch-configurable AT products. The configuration files are used at system configuration time to assign system resources (such as DMA channels, interrupt levels) and thus prevent conflicts between the installed expansion boards. For switch-configurable boards, the configuration files can be used to outline the proper assignment of resources and instruct the user about the proper selection of switch settings.

To accomplish the automatic system and expansion board configuration, EISA provides a method for accessing I/O port ranges that are slot specific. This means that a board using these ranges can be plugged into any slot in the system without the risk of I/O range conflicts. These I/O ranges can be used for expansion board initialization or for normal I/O port assignments that are guaranteed not to conflict with any other expansion board installed in the system.

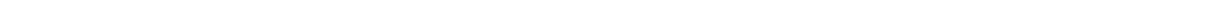
The DRAGON EISA system board has eight 32-bit EISA expansion slots. Each EISA slot is fully compatible with AT bus slot. The major difference in EISA slot are:

- EISA slots are physically deeper and have total of 188 pins.*
 - The top 98 pins are used for the PC/AT card signal.*
-

GENERAL FEATURES

- *The remaining deeper set of 90 pins are used for the EISA card signal.*

Because the EISA slots are downward compatible to AT slots, so an AT expansion card can be inserted into these EISA slots and will work properly.



GENERAL FEATURES

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Chapter 3

Configuring The System

Important Note : Turn off the power of your computer before installing or replacing any component.

CONFIGURING WEITEK 4167 COPROCESSOR

Math coprocessor WEITEK 4167 is a PGA devices. Beside the CPU, there is a 144-pin PGA socket. To install Math Coprocessor, be sure to line up pin 1 of the Math coprocessor with pin 1 of the socket as shown below.

CONFIGURING THE SYSTEM

<i>Cache Size</i>	<i>U53,55,65,67</i>	<i>U52,54,66,68</i>	<i>U56,57,69,70</i>
<i>64KB</i>	<i>8Kx8</i>	<i>---</i>	<i>8Kx8</i>
<i>128KB</i>	<i>32Kx8</i>	<i>---</i>	<i>----</i>
<i>256KB</i>	<i>32Kx8</i>	<i>---</i>	<i>32Kx8</i>
<i>512KB</i>	<i>32Kx8</i>	<i>128Kx8</i>	<i>---</i>

<i>Cache Size</i>	<i>U50</i>	<i>U51</i>	<i>U64</i>
<i>64KB</i>	<i>8Kx8</i>	<i>---</i>	<i>16Kx1 or 64Kx1</i>
<i>128KB</i>	<i>8Kx8</i>	<i>---</i>	<i>16Kx1 or 64Kx1</i>
<i>256KB</i>	<i>8Kx8</i>	<i>8Kx8</i>	<i>16Kx1 or 64Kx1</i>
<i>512KB</i>	<i>32Kx8</i>	<i>---</i>	<i>64Kx1</i>

CONFIGURING THE SYSTEM

INSTALLING DRAM SIMM MODULES

There are two banks of memory and totally 8 SIMM sockets on the DRAGON EISA board. Whenever you add memory to the motherboard, install four modules at the same time. That means at least one bank of memory is filled on each time of adding memory. If the SIMM modules is installed correctly then the SIMM modules should be locked firmly by the locking latches of the sockets.

To install a module, the module edge is angled into the socket's contact and then the module is pivoted into position, where the locking latches will secure it. If the module edge is not completely inserted into the socket, it cannot be pivoted to be in vertical position and should be dragged out and re-inserted again. Do not force the module into the SIMM socket. It will damage the locking latches.

You can install different size of memory system by using one of following types of SIMM memory.

- 1) 1M bit x 9 SIMM*
- 2) 4M bit x 9 SIMM*
- 3) 16M bit x 9 SIMM*

If the BIOS reports an memory error or parity error, drag out the modules and insert again.

CONFIGURING THE SYSTEM

CONFIGURATION OF MEMORY

The configuration of the memory is very flexible. There are several combinations of DRAM types you may consider. 1MB, 4MB or 16MB SIMM are acceptable. So, a basic system can be equipped with fewer memory and later more memory can be installed when upgrading the system. The memory size is detected automatically by system BIOS and indicated during memory test after reset. No jumper is needed to be set for the memory size and DRAM type.

To determine what DRAM speed rating should be used depends on the system speed and wait state. The highest performance is accomplished by using zero wait state, but high speed DRAM has to be used. If zero wait state is selected, fast page mode DRAM is needed. The wait state setting is applied to all banks of memory. Therefore make sure to install DRAM with the same speed rating, or accommodate the wait state setting to the slow DRAM type.

Because of the shadow RAM function, the 384KB memory between 640KB to 1MB can not accessed. So, the memory size found by the system BIOS is not equal to the actual memory size. For example, when there is 4MB on board, the BIOS will show 3712KB.

CONFIGURING THE SYSTEM

DRAM CONFIGURATION

Bank 0	Bank 1	Total
<i>1M</i>	---	<i>4M</i>
<i>1M</i>	<i>1M</i>	<i>8M</i>
<i>4M</i>	---	<i>16M</i>
<i>1M</i>	<i>4M</i>	<i>20M</i>
<i>4M</i>	<i>4M</i>	<i>32M</i>
<i>16M</i>	---	<i>64M</i>
<i>16M</i>	<i>16M</i>	<i>128M</i>

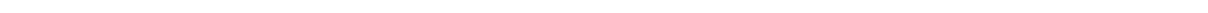
CONFIGURING THE SYSTEM

SYSTEM BOARD JUMPER SETTING

There are several options which allows user to select by hardware switches.

Display Selection

<i>JP4</i>	
<i>ON</i>	<i>CGA, EGA, VGA</i>
<i>OFF</i>	<i>Monochrome display</i>



CONFIGURING THE SYSTEM

SYSTEM BOARD CONNECTORS

There are six connectors on the system board.

	<i>Description</i>
<i>S9</i>	<i>Hardware reset connector</i>
<i>J1</i>	<i>Keyboard connector</i>
<i>J2,J3</i>	<i>Power supply connector</i>
<i>J4</i>	<i>Speaker connector</i>
<i>J5</i>	<i>Key lock connector</i>
<i>JP17</i>	<i>Heat sink with fan connector</i>

Pin assignment of the connector are illustrated as follows:

S9 - Hardware Reset Connector

<i>Pin</i>	<i>Assignment</i>
<i>1</i>	<i>Selection Pin</i>
<i>2</i>	<i>Ground</i>

CONFIGURING THE SYSTEM

J1 - Keyboard Connector

<i>Pin</i>	<i>Assignment</i>
<i>1</i>	<i>Keyboard Clock</i>
<i>2</i>	<i>Keyboard Data</i>
<i>3</i>	<i>Spare</i>
<i>4</i>	<i>Ground</i>
<i>5</i>	<i>+5 Vdc</i>

J2,J3 - Power Supply Connector

<i>Pin</i>	<i>Assignment</i>
<i>1</i>	<i>Powergood</i>
<i>2</i>	<i>+5 Vdc</i>
<i>3</i>	<i>+12 Vdc</i>
<i>4</i>	<i>-12 Vdc</i>
<i>5</i>	<i>Ground</i>
<i>6</i>	<i>Ground</i>

<i>Pin</i>	<i>Assignment</i>
<i>1</i>	<i>Ground</i>
<i>2</i>	<i>Ground</i>
<i>3</i>	<i>-5 Vdc</i>
<i>4</i>	<i>+5 Vdc</i>
<i>5</i>	<i>+5 Vdc</i>

CONFIGURING THE SYSTEM

6	+5 Vdc
---	--------



CONFIGURING THE SYSTEM

J4 - Speaker Connector

<i>Pin</i>	<i>Assignment</i>
<i>1</i>	<i>Data out</i>
<i>2</i>	<i>+5 Vdc</i>
<i>3</i>	<i>Ground</i>
<i>4</i>	<i>+5 Vdc</i>

J5 - Key Lock

<i>Pin</i>	<i>Assignment</i>
<i>1</i>	<i>+5Vdc</i>
<i>2</i>	<i>Key</i>
<i>3</i>	<i>Ground</i>
<i>4</i>	<i>Keyboard Inhibit</i>
<i>5</i>	<i>Ground</i>

JP22 - Heat Sink with Fan Connector

<i>Pin</i>	<i>Assignment</i>
<i>1</i>	<i>+5 Vdc</i>
<i>2</i>	<i>Ground</i>

Chapter 4

Technical Information

MEMORY MAPPING

<i>Address</i>	<i>Range</i>	<i>Function</i>
000000-7FFFFFFF	000K-512K	System Board Memory (512K)
080000-09FFFF	512K-640K	System Board Memory (128K)
0A0000-0BFFFF	640K-768K	Display Buffer (128K)
0C0000-0DFFFF	768K-896K	Adaptor ROM / Shadow RAM (128K)
0E0000-0EFFFF	896K-960K	System ROM / Shadow RAM (64K)
0F0000-0FFFFFFF	960K-1024K	System BIOS ROM / Shadow RAM (64K)
100000-7FFFFFFF	1024K-8192K	System Memory
800000-FFFFFFFF	8192K-16318K	System Memory

TECHNICAL INFORMATION

SYSTEM EXPANSION BUS

The DRAGON EISA provides 8 EISA slots. Each EISA slot has its own I/O address range. For example, I/O address 1000-1FFF belong to slot 1; I/O address 2000-2FFF belong to slot 2.

The following figure shows the pin numbering for I/O channel connectors (A-side, B-side, E-side and F-side)



TECHNICAL INFORMATION

The following figure shows the pin numbering for I/O channel connectors (C-side, D-side, G-side and H-side).

TECHNICAL INFORMATION

The following tables summarize pin assignments for the I/O channel connectors.

I/O Channel (A-Side)

I/O Pin	Signal Name	I/O
A1	-I/O CH CK	I
A2	SD7	I/O
A3	SD6	I/O
A4	SD5	I/O
A5	SD4	I/O
A6	SD3	I/O
A7	SD2	I/O
A8	SD1	I/O
A9	SD0	I/O
A10	-I/O CH RDY	I
A11	AENx	O
A12	SA19	I/O
A13	SA18	I/O
A14	SA17	I/O
A15	SA16	I/O
A16	SA15	I/O
A17	SA14	I/O
A18	SA13	I/O
A19	SA12	I/O
A20	SA11	I/O
A21	SA10	I/O
A22	SA9	I/O
A23	SA8	I/O
A24	SA7	I/O
A25	SA6	I/O

TECHNICAL INFORMATION

A26	SA5	I/O
A27	SA4	I/O
A28	SA3	I/O
A29	SA2	I/O
A30	SA1	I/O
A31	SA0	I/O

TECHNICAL INFORMATION

I/O Channel (B-Side)

<i>I/O Pin</i>	<i>Signal Name</i>	<i>I/O</i>
<i>B1</i>	<i>GND</i>	<i>Ground</i>
<i>B2</i>	<i>RESET DRV</i>	<i>I</i>
<i>B3</i>	<i>+5 Vdc</i>	<i>Power</i>
<i>B4</i>	<i>IRQ9</i>	<i>I</i>
<i>B5</i>	<i>-5 Vdc</i>	<i>Power</i>
<i>B6</i>	<i>DRQ2</i>	<i>I</i>
<i>B7</i>	<i>-12 Vdc</i>	<i>Power</i>
<i>B8</i>	<i>OWS</i>	<i>I</i>
<i>B9</i>	<i>+12 Vdc</i>	<i>Power</i>
<i>B10</i>	<i>GND</i>	<i>Ground</i>
<i>B11</i>	<i>-SMEMW</i>	<i>O</i>
<i>B12</i>	<i>-SMEMR</i>	<i>O</i>
<i>B13</i>	<i>-IOW</i>	<i>I/O</i>
<i>B14</i>	<i>-IOR</i>	<i>I/O</i>
<i>B15</i>	<i>-DACK3</i>	<i>I</i>
<i>B16</i>	<i>DRQ3</i>	<i>O</i>
<i>B17</i>	<i>-DACK1</i>	<i>I</i>
<i>B18</i>	<i>DRQ1</i>	<i>O</i>
<i>B19</i>	<i>-Refresh</i>	<i>I/O</i>
<i>B20</i>	<i>BCLK</i>	<i>O</i>
<i>B21</i>	<i>IRQ7</i>	<i>I</i>
<i>B22</i>	<i>IRQ6</i>	<i>I</i>
<i>B23</i>	<i>IRQ5</i>	<i>I</i>
<i>B24</i>	<i>IRQ4</i>	<i>I</i>
<i>B25</i>	<i>IRQ3</i>	<i>I</i>
<i>B26</i>	<i>-DACK2</i>	<i>O</i>
<i>B27</i>	<i>T/C</i>	<i>O</i>
<i>B28</i>	<i>BALE</i>	<i>O</i>

TECHNICAL INFORMATION

<i>B29</i>	<i>+5 Vdc</i>	<i>Power</i>
<i>B30</i>	<i>OSC</i>	<i>O</i>
<i>B31</i>	<i>GND</i>	<i>Ground</i>

TECHNICAL INFORMATION

I/O Channel (C-Side)

<i>I/O Pin</i>	<i>Signal Name</i>	<i>I/O</i>
<i>C1</i>	<i>SBHE</i>	<i>I/O</i>
<i>C2</i>	<i>LA23</i>	<i>I/O</i>
<i>C3</i>	<i>LA22</i>	<i>I/O</i>
<i>C4</i>	<i>LA21</i>	<i>I/O</i>
<i>C5</i>	<i>LA20</i>	<i>I/O</i>
<i>C6</i>	<i>LA19</i>	<i>I/O</i>
<i>C7</i>	<i>LA18</i>	<i>I/O</i>
<i>C8</i>	<i>LA17</i>	<i>I/O</i>
<i>C9</i>	<i>-MEMR</i>	<i>I/O</i>
<i>C10</i>	<i>-MEMW</i>	<i>I/O</i>
<i>C11</i>	<i>SD8</i>	<i>I/O</i>
<i>C12</i>	<i>SD9</i>	<i>I/O</i>
<i>C13</i>	<i>SD10</i>	<i>I/O</i>
<i>C14</i>	<i>SD11</i>	<i>I/O</i>
<i>C15</i>	<i>SD12</i>	<i>I/O</i>
<i>C16</i>	<i>SD13</i>	<i>I/O</i>
<i>C17</i>	<i>SD14</i>	<i>I/O</i>
<i>C18</i>	<i>SD15</i>	<i>I/O</i>

TECHNICAL INFORMATION

I/O Channel (D-Side)

<i>I/O Pin</i>	<i>Signal Name</i>	<i>I/O</i>
<i>D1</i>	<i>-MEM CS16</i>	<i>I</i>
<i>D2</i>	<i>-I/O CS16</i>	<i>I</i>
<i>D3</i>	<i>IRQ10</i>	<i>I</i>
<i>D4</i>	<i>IRQ11</i>	<i>I</i>
<i>D5</i>	<i>IRQ12</i>	<i>I</i>
<i>D6</i>	<i>IRQ15</i>	<i>I</i>
<i>D7</i>	<i>IRQ14</i>	<i>I</i>
<i>D8</i>	<i>-DACK0</i>	<i>O</i>
<i>D9</i>	<i>DRQ0</i>	<i>I</i>
<i>D10</i>	<i>-DACK5</i>	<i>O</i>
<i>D11</i>	<i>DRQ5</i>	<i>I</i>
<i>D12</i>	<i>-DACK6</i>	<i>O</i>
<i>D13</i>	<i>DRQ6</i>	<i>I</i>
<i>D14</i>	<i>-DACK7</i>	<i>O</i>
<i>D15</i>	<i>DRQ7</i>	<i>I</i>
<i>D16</i>	<i>+5 Vdc</i>	<i>Power</i>
<i>D17</i>	<i>-MASTER</i>	<i>I</i>
<i>D18</i>	<i>GND</i>	<i>Ground</i>

TECHNICAL INFORMATION

I/O Channel (E-Side)

<i>I/O Pin</i>	<i>Signal Name</i>	<i>I/O</i>
E1	-CMD	O
E2	-START	I/O
E3	EXRDY	I/O
E4	-EX32	I/O
E5	GND	Ground
E6	ACCESS KEY	---
E7	-EX16	I/O
E8	-SLBURST	I
E9	-MSBURST	I/O
E10	W-R	I/O
E11	GND	Ground
E12	RESERVED	---
E13	RESERVED	---
E14	RESERVED	---
E15	GND	Ground
E16	ACCESS KEY	---
E17	-BE1	I/O
E18	-LA31	I/O
E19	GND	Ground
E20	-LA30	I/O
E21	-LA28	I/O
E22	-LA27	I/O
E23	-LA25	I/O
E24	GND	Ground
E25	ACCESS KEY	---
E26	LA15	I/O
E27	LA13	I/O
E28	LA12	I/O

TECHNICAL INFORMATION

<i>E29</i>	<i>LA11</i>	<i>I/O</i>
<i>E30</i>	<i>GND</i>	<i>Ground</i>
<i>E31</i>	<i>LA9</i>	<i>I/O</i>

TECHNICAL INFORMATION

I/O Channel (F-Side)

<i>I/O Pin</i>	<i>Signal Name</i>	<i>I/O</i>
F1	GND	Ground
F2	+5 Vdc	Power
F3	+5 Vdc	Power
F4	XXXXXX	---
F5	XXXXXX	---
F6	ACCESS KEY	---
F7	XXXXXX	---
F8	XXXXXX	---
F9	+12 Vdc	Power
F10	M-IO	I/O
F11	-LOCK	0
F12	RESERVED	---
F13	GND	Ground
F14	RESERVED	---
F15	-BE3	I/O
F16	ACCESS KEY	---
F17	-BE2	I/O
F18	-BE0	I/O
F19	GND	Ground
F20	+5 Vdc	Power
F21	-LA29	I/O
F22	GND	Ground
F23	-LA26	I/O
F24	-LA24	I/O
F25	ACCESS KEY	---
F26	LA16	I/O
F27	LA14	I/O
F28	+5 Vdc	Power

TECHNICAL INFORMATION

<i>F29</i>	<i>+5 Vdc</i>	<i>Power</i>
<i>F30</i>	<i>GND</i>	<i>Ground</i>
<i>F31</i>	<i>LA10</i>	<i>I/O</i>

TECHNICAL INFORMATION

I/O Channel (G-Side)

<i>I/O Pin</i>	<i>Signal Name</i>	<i>I/O</i>
G1	LA7	I/O
G2	GND	Ground
G3	LA4	I/O
G4	LA3	I/O
G5	GND	Ground
G6	ACCESS KEY	---
G7	D17	I/O
G8	D19	I/O
G9	D20	I/O
G10	D22	I/O
G11	GND	Ground
G12	D25	I/O
G13	D26	I/O
G14	D28	I/O
G15	ACCESS KEY	---
G16	GND	Ground
G17	D30	I/O
G18	D31	I/O
G19	-MREQX	I

TECHNICAL INFORMATION

I/O Channel (H-Side)

<i>I/O Pin</i>	<i>Signal Name</i>	<i>I/O</i>
<i>H1</i>	<i>LA8</i>	<i>I/O</i>
<i>H2</i>	<i>LA6</i>	<i>I/O</i>
<i>H3</i>	<i>LA5</i>	<i>I/O</i>
<i>H4</i>	<i>+5 Vdc</i>	<i>Power</i>
<i>H5</i>	<i>LA2</i>	<i>I/O</i>
<i>H6</i>	<i>ACCESS KEY</i>	<i>---</i>
<i>H7</i>	<i>D16</i>	<i>I/O</i>
<i>H8</i>	<i>D18</i>	<i>I/O</i>
<i>H9</i>	<i>GND</i>	<i>Ground</i>
<i>H10</i>	<i>D21</i>	<i>I/O</i>
<i>H11</i>	<i>D23</i>	<i>I/O</i>
<i>H12</i>	<i>D24</i>	<i>I/O</i>
<i>H13</i>	<i>GND</i>	<i>Ground</i>
<i>H14</i>	<i>D27</i>	<i>I/O</i>
<i>H15</i>	<i>ACCESS KEY</i>	<i>---</i>
<i>H16</i>	<i>D29</i>	<i>I/O</i>
<i>H17</i>	<i>+5 Vdc</i>	<i>Power</i>
<i>H18</i>	<i>+5 Vdc</i>	<i>Power</i>
<i>H19</i>	<i>-MAKx</i>	<i>O</i>

TECHNICAL INFORMATION

I/O ADDRESS MAP

I/O Address Map on System Board

I/O address hex 000 to 0FF are reserved for the system board I/O.

<i>ADDRESS (HEX)</i>	<i>DEVICE</i>
<i>0000-001F</i>	<i>DMA Controller 1, 8237</i>
<i>0020-003F</i>	<i>Interrupt Controller 1, 8259, Master</i>
<i>0040-005F</i>	<i>Timer, 8254</i>
<i>0060-006F</i>	<i>Keyboard Controller</i>
<i>0070-007F</i>	<i>Real Time Clock, NMI (non-maskable interrupt) mask</i>
<i>0080-009F</i>	<i>DMA Page Register, 74LS612</i>
<i>00A0-00BF</i>	<i>Interrupt Controller 2, 8259</i>
<i>00C0-00DF</i>	<i>DMA Controller 2, 8237</i>
<i>00F0</i>	<i>Clear Math Coprocessor Busy</i>
<i>00F1</i>	<i>Reset Math Coprocessor</i>
<i>00F8-00FF</i>	<i>Math Coprocessor Port</i>

TECHNICAL INFORMATION

I/O address hex 100 to 3FF are available on the I/O channel.

<i>ADDRESS (HEX)</i>	<i>DEVICE</i>
<i>01F0-01F8</i>	<i>Fixed Disk</i>
<i>0200-0207</i>	<i>Game I/O</i>
<i>0278-027F</i>	<i>Parallel Printer Port 2</i>
<i>02F8-02FF</i>	<i>Serial Port 2</i>
<i>0300-031F</i>	<i>Prototype Card</i>
<i>0360-036F</i>	<i>Reserved</i>
<i>0378-037F</i>	<i>Parallel Printer Port 1</i>
<i>0380-038F</i>	<i>SDLC, bisynchronous 2</i>
<i>03A0-03AF</i>	<i>Bisynchronous 1</i>
<i>03B0-03BF</i>	<i>Monochrome Display and Printer Adapter</i>
<i>03C0-03CF</i>	<i>Reserved</i>
<i>03D0-03DF</i>	<i>Color Graphics Monitor Adapter</i>
<i>03F0-03F7</i>	<i>Diskette Controller</i>
<i>03F8-03FF</i>	<i>Serial Port 1</i>
<i>0400-4FFF</i>	<i>System Board</i>
<i>0500-07FF</i>	<i>Alias of 100h-3FFh</i>
<i>0800-08FF</i>	<i>System Board</i>
<i>0900-0BFF</i>	<i>Alias of 100h-3FFh</i>
<i>0C00-0CFF</i>	<i>System Board</i>
<i>0D00-0FFF</i>	<i>Alias of 100h-3FFh</i>

TECHNICAL INFORMATION

ADDRESS (HEX)	DEVICE
1000-10FF	Slot 1
1100-13FF	Alias of 100h-3FFh
1400-14FF	Slot 1
1500-17FF	Alias of 100h-3FFh
1800-18FF	Slot 1
1900-1BFF	Alias of 100h-3FFh
1C00-1CFF	Slot 1
1D00-1FFF	Alias of 100h-3FFh
:	:
:	:
:	:
:	:
x000-x0FF	Slot `x`
x100-x3FF	Alias of 100h-3FFh
x400-x4FF	Slot `x`
x500-x7FF	Alias of 100h-3FFh
x800-x8FF	Slot `x`
x900-xBFF	Alias of 100h-3FFh
xC00-xCFF	Slot `x`
xD00-xFFF	Alias of 100h-3FFh

Note: I/O addresses between 1000h and FFFFh that are not identified as "Alias of 100h-3FFh" are reserved for slot-specific addressing of expansion boards. The most significant digit in the address represents the slot number (indicated in the table by "Slot x", where 'x' can be any value from 1 to 8). The system board I/O range resides at I/O address between 0000h and 0FFFh ('x' = 0).

I/O address between 0400h and 04FFh are reserved for current and future EISA system board peripherals defined by this specification. System board manufacturers may use system board address 0800-08FFh and 0C00-0CFFh for manufacturer specific I/O devices.

SYSTEM INTERRUPTS

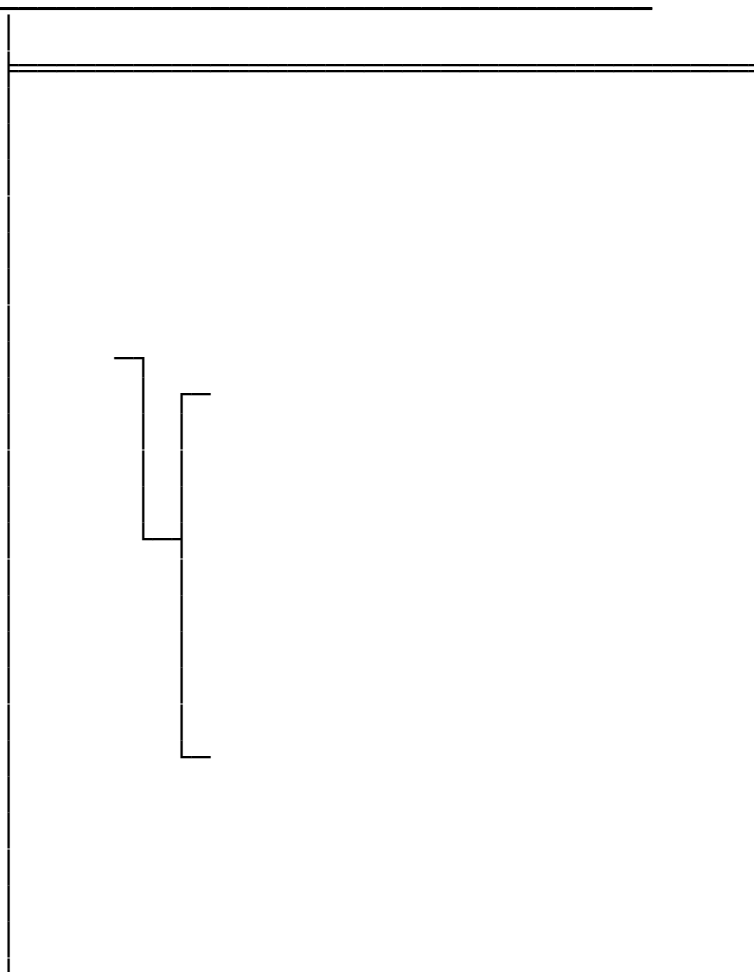
EISA systems provide an ISA compatible interrupt controller with the EISA enhancement. Interrupts can be set as edge trigger tive or level trigger. The EISA interrupt controller incorporates the functionality of two 8259 interrupt controllers. There are total sixteen levels of system interrupt on the DRAGON EISA board. However, IRQ2 channel is used to cascade interrupts, therefore only 15 levels of interrupt are available on the system board.

The following shows the interrupt-level assignment in decreasing priority.

TECHNICAL INFORMATION

Level	Function
<i>Microprocessor NMI</i>	<i>Parity or I/O Channel Check</i>
<i>Interrupt Controllers</i>	
<i>CTLR 1</i>	<i>CTLR 2</i>
<i>IRQ0</i>	<i>Timer Output 0</i>
<i>IRQ1</i>	<i>Keyboard (Output Buffer Full)</i>
<i>IRQ2</i>	<i>Interrupt from CTLR 2</i>
	<i>IRQ8 Real-time Clock Interrupt</i>
	<i>IRQ9 Software Redirected to INT 0AH (IRQ2)</i>
	<i>IRQ10 Reserved</i>
	<i>IRQ11 Reserved</i>
	<i>IRQ12 Reserved</i>
	<i>IRQ13 Coprocessor</i>
	<i>IRQ14 Fixed Disk Controller</i>
	<i>IRQ15 Reserved</i>
<i>IRQ3</i>	<i>Serial Port 2</i>
<i>IRQ4</i>	<i>Serial Port 1</i>
<i>IRQ5</i>	<i>Parallel Port 2</i>
<i>IRQ6</i>	<i>Diskette Controller</i>
<i>IRQ7</i>	<i>Parallel Port 1</i>

TECHNICAL INFORMATION



TECHNICAL INFORMATION

DIRECT MEMORY ACCESS (DMA)

EISA system provide seven ISA compatible DMA channels. Any channel can be programmed to provide EISA performance and addressing benefits to existing 8- and 16-bit DMA devices while maintaining full ISA compatibility.

Any DMA channel can be programmed for 8-, 16-, 32-bit DMA device size.

The function of each channel are shown below :

<i>Channel</i>	<i>Function</i>
<i>0</i>	<i>Spare</i>
<i>1</i>	<i>SDLC</i>
<i>2</i>	<i>Floppy Disk</i>
<i>3</i>	<i>Spare</i>
<i>4</i>	<i>Cascade for DMA Controller 1</i>
<i>5</i>	<i>Spare</i>
<i>6</i>	<i>Spare</i>
<i>7</i>	<i>Spare</i>

TECHNICAL INFORMATION

The following shows the addresses for the LOW and HIGH page register.

<i>Low Page Register</i>	<i>I/O Address (HEX)</i>
<i>DMA Channel 0</i>	<i>0087</i>
<i>DMA Channel 1</i>	<i>0083</i>
<i>DMA Channel 2</i>	<i>0081</i>
<i>DMA Channel 3</i>	<i>0082</i>
<i>DMA Channel 5</i>	<i>008B</i>
<i>DMA Channel 6</i>	<i>0089</i>
<i>DMA Channel 7</i>	<i>008A</i>
<i>Refresh</i>	<i>008F</i>

<i>High Page Register</i>	<i>I/O Address (HEX)</i>
<i>DMA Channel 0</i>	<i>0487</i>
<i>DMA Channel 1</i>	<i>0483</i>
<i>DMA Channel 2</i>	<i>0481</i>
<i>DMA Channel 3</i>	<i>0482</i>
<i>DMA Channel 5</i>	<i>048B</i>
<i>DMA Channel 6</i>	<i>0489</i>
<i>DMA Channel 7</i>	<i>048A</i>
<i>Refresh</i>	<i>048F</i>

TECHNICAL INFORMATION

REAL TIME CLOCK AND CMOS RAM

Real time clock and CMOS RAM are contained on board. Real time clock provides the system date and time. CMOS RAM stores system information. Both are backed up by battery and will not lose information after power off. The following page shows the CMOS RAM Address Map.

TECHNICAL INFORMATION

CMOS RAM ADDRESS MAP

<i>Addresses</i>	<i>Description</i>
<i>00-0D</i>	<i>* Real-time clock information</i>
<i>0E</i>	<i>Diagnostic status byte</i>
<i>0F</i>	<i>Shutdown status byte</i>
<i>10</i>	<i>Diskette drive type byte - drives A and B</i>
<i>11</i>	<i>Reserved</i>
<i>12</i>	<i>Fixed disk type byte - drives C and D</i>
<i>13</i>	<i>Reserved</i>
<i>14</i>	<i>Equipment</i>
<i>15</i>	<i>Low base memory byte</i>
<i>16</i>	<i>High base memory byte</i>
<i>17</i>	<i>Low expansion memory byte</i>
<i>18</i>	<i>High expansion memory byte</i>
<i>19-2D</i>	<i>Reserved</i>
<i>2E-2F</i>	<i>2-byte CMOS checksum</i>
<i>30</i>	<i>Low expansion memory byte</i>
<i>31</i>	<i>High expansion memory byte</i>
<i>32</i>	<i>Date century byte</i>
<i>33</i>	<i>Information flags (set during power on)</i>
<i>34-3F</i>	<i>Reserved</i>

TECHNICAL INFORMATION

REAL TIME CLOCK INFORMATION

The following table describes real-time clock types and specifies their addresses.

<i>Byte</i>	<i>Function</i>	<i>Address</i>
<i>0</i>	<i>Seconds</i>	<i>00</i>
<i>1</i>	<i>Second alarm</i>	<i>01</i>
<i>2</i>	<i>Minutes</i>	<i>02</i>
<i>3</i>	<i>Minute alarm</i>	<i>03</i>
<i>4</i>	<i>Hours</i>	<i>04</i>
<i>5</i>	<i>Hour alarm</i>	<i>05</i>
<i>6</i>	<i>Day of week</i>	<i>06</i>
<i>7</i>	<i>Date of month</i>	<i>07</i>
<i>8</i>	<i>Month</i>	<i>08</i>
<i>9</i>	<i>Year</i>	<i>09</i>
<i>10</i>	<i>Status Register A</i>	<i>0A</i>
<i>11</i>	<i>Status Register B</i>	<i>0B</i>
<i>12</i>	<i>Status Register C</i>	<i>0C</i>
<i>13</i>	<i>Status Register D</i>	<i>0D</i>

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Appendix A

System BIOS

The system BIOS in DRAGON EISA system board provides an interface for operating systems and applications to access the hardware. It is fully compatible with standard AT BIOS. It supports all extended features on EISA specifications such as initialisation of EISA adapters and EISA bus master support. It also performs self-test after reset and includes a setup program to setup the system.

SELF-TEST

To ensure the computer hardware is functional, the system BIOS will carry out a self-test upon reset. The test is very intensive and covers all parts of hardware. It takes a while before some messages are shown on the screen. It does not mean that the system is not working when the screen is blank. So wait for a while after turning on the power and listen carefully to the speaker. Some errors are reported by a number of beep sounds. After completing the self-test, the BIOS will display some messages on the screen.

In case of serious errors, the BIOS will suspend the test. If the display is not initialized, the BIOS will report the error through a sequence of beep sounds. Otherwise, error message will be shown on the screen.

SYSTEM BIOS

These fatal errors are usually communicated through a series of audible beeps. The numbers on the fatal error list below correspond to the number of beeps for the corresponding error. All errors listed, with the exception of #8, are fatal errors.

<i>No. of Beeps</i>	<i>Error Message</i>
<i>1</i>	<i>DRAM Refresh Failure</i>
<i>2</i>	<i>Base 64KB Memory Parity Error</i>
<i>3</i>	<i>Base 64KB Memory Failure</i>
<i>4</i>	<i>System Time Failure</i>
<i>5</i>	<i>Processor Error</i>
<i>6</i>	<i>Keyboard Controller Gate A20 Failure</i>
<i>7</i>	<i>Processor Exception Interrupt Error</i>
<i>8</i>	<i>Display Memory Read / Write Error (Video Adapter)</i>
<i>9</i>	<i>ROM Checksum Error</i>
<i>10</i>	<i>CMOS Shutdown Register Read/Write Error</i>

If no error is found during self-test, the system BIOS will proceed to boot from floppy disk or hard disk. The system BIOS will list the system configuration on the screen shown in next page.

SYSTEM BIOS

System Configuration (C) Copyright 1985-1992, American Megatrends Inc.,

Main Processor	: 80486	Base Memory Size	: 640 KB
Numeric Processor	: None	Ext. Memory Size	: 7424 KB
Floppy Drive A:	: 1.2 MB, 5¼"	Hard Disk C: Type	: 2
Floppy Drive B:	: 1.44MB, 3½"	Hard Disk D: Type	: None
Display Type	: VGA or EGA	Serial Port(s)	: None
ROM-BIOS Date	: 07/07/90	Parallel Port(s)	: 3BC

Do check the list to make sure that the configuration is correct. Sometimes, problems arise because of the incorrect information of the configuration. For example, if you forget to modify the setup after changing the floppy disk drive from one type to another, it can not boot from floppy disk or may not work properly. If you check the list, you can find the cause of the problem.

SYSTEM BIOS

SYSTEM SETUP

The BIOS incorporates :

- (1) *Standard CMOS Setup*
- (2) *Advanced CMOS Setup*
- (3) *Advanced Chipset Setup*
- (4) *Auto Configuration with BIOS Defaults*
- (5) *Auto Configuration with Power-On Defaults*
- (6) *Change Password*
- (7) *Hard Disk Utilities*

It is important that all the setup procedures should be completed before operating the system. Otherwise, the system will not run properly with the incorrect setup information. Run the setup again if the configuration is changed.

To enter the setup section, press 'DEL' when the following message is shown during memory test :

Hit if you want to run SETUP

Whenever the system BIOS finds that the configuration of the system is altered, error message will be shown and you may press 'F1' to run setup. Then the following messages are shown on the screen.

SYSTEM BIOS

<i>BIOS SETUP PROGRAM - AMI BIOS SETUP UTILITIES</i>
<i><C> 1990 American Megatrends, Inc. All Rights Reserved</i>
<i>STANDARD CMOS SETUP</i>
<i>ADVANCED CMOS SETUP</i>
<i>ADVANCED CHIPSET SETUP</i>
<i>AUTO CONFIGURATION WITH BIOS DEFAULTS</i>
<i>AUTO CONFIGURATION WITH POWER-ON DEFAULTS</i>
<i>CHANGE PASSWORD</i>
<i>HARD DISK UTILITY</i>
<i>WRITE TO CMOS AND EXIT</i>
<i>DO NOT WRITE TO CMOS AND EXIT</i>
<i>Configure system with Power On Default Values for Chipset and Advanced CMOS</i>



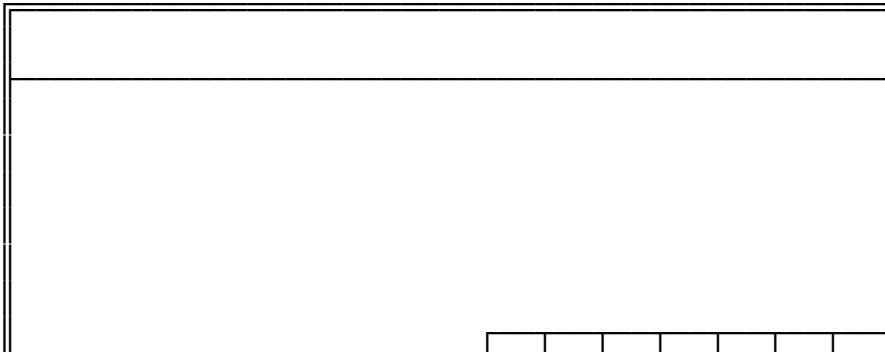
SYSTEM BIOS

(1) CMOS SETUP

The memory size is detected by the BIOS. So you are only required to set those options on the left side of the screen. The system configuration information are shown as follows:

CMOS SETUP (C) Copyright 1985-1990, American Megatrends Inc.,

Date (mn/date/year) :	Sun, Jul 01, 1990	Base memory size :	640 KB
Time (hour/min/sec) :	12 : 05 : 30	Ext. memory size :	7424 KB
Daylight Saving :	Disabled	Cyln Head WPcom LZone Sect	
Size			
Hard Disk C: type :	Not Installed		
Hard Disk D: type :	Not Installed		
Floppy Drive A: :	1.2 MB, 5¼		
Floppy Drive B: :	1.44 MB, 3½		
Primary Display :	VGA or EGA	Sun Mon Tue Wed ThuFri Sat	
Keyboard :	Installed		
		1 2 3 4 5 6 7	
		8 9 10 11 12 13 14	
		15 16 17 18 19 20 21	
Month : Jan, Feb, Dec		22 23 24 25 26 27 28	
Date : 01, 02, 03, 31			
Year : 1901, 1902, 2099	29 30 31 1 2 3 4		
ESC=Exit, ↓→↑←=Select, PgUp/PgDn=Modify	5 6 7 8 9 10 11		



SYSTEM BIOS

SYSTEM BIOS

OPTION 1 TIME AND DATE

Use PgUp and PgDn keys to change the value. The date and time cannot be entered directly. A calendar is displayed on the lower right corner of the screen for your reference.

OPTION 2 FIXED DISK DRIVE

There are 47 types of fixed disks supported by the BIOS. Consult your fixed disk manual to determine its correct type. The parameters such as cylinder number, head number, sector number and pre-compensation must match your fixed disk's parameters.

Use PgUp and PgDn keys to change the fixed disk type. If the type of your fixed disk is not included in the hard disk list, define a new type as type 47. Use left and right arrow keys to move between the parameter fields and enter the parameters. The parameters will be stored in the CMOS RAM and your fixed disk can be used afterwards. Each hard disk can be assigned a different type 47 hard disk. So two hard disks which are not included in the list can be used together in your system.

If the type of fixed disk is wrong, it takes a while before the BIOS can identify the error. After setting the fixed disk type, if the system halts after reboot, please wait for a while. It is most likely that the setting of fixed disk type is incorrect.

When you install a new hard disk, make sure whether it is already formatted. If not, the BIOS has to check for a while before reporting the hard disk error. In fact, the error arises only because the hard disk is not formatted. If the hard disk is formatted, you can run DOS FDISK and DOS FORMAT.

SYSTEM BIOS

Some fixed disks e.g. some SCSI are specially handled and must be set to 'Not Installed'. Consult the fixed disk manual for details.

OPTION 3 FLOPPY DISK DRIVE

Four types of floppy disk drives are supported:

- 1. 5- $\frac{1}{4}$ inch standard drive (360K)*
 - 2. 5- $\frac{1}{4}$ inch high-density drive (1.2M)*
 - 3. 3- $\frac{1}{2}$ inch standard drive (720K)*
 - 4. 3- $\frac{1}{2}$ inch high-density drive (1.44M)*
-

SYSTEM BIOS

The system BIOS supports two floppy disk drives and they are recognized as drive A and B. Select the correct types. Otherwise the drives cannot work properly. If one of them is not installed, select 'Not Installed' for that drive.

The BIOS is able to detect the type of the drives automatically. But remember to check the settings before exit.

OPTION 4 DISPLAY

Four types of display are supported:

- 1. CGA 80 column mode*
- 2. CGA 40 column mode*
- 3. EGA and VGA*
- 4. Monochrome*

If the type of display is incorrect, the BIOS will prompt you and ask you to set up again. But the BIOS is still able to display messages on the display attached to the system. Thus you can enter the setup program.

The jumper JP4 must be set according to this setting. Otherwise, the BIOS will report error after self-test.

SYSTEM BIOS

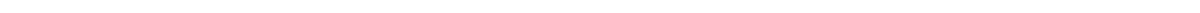
OPTION 5 KEYBOARD

If a keyboard is attached to the system, select 'Installed'. The BIOS will test the keyboard during self-test.

(2) ADVANCED CMOS SETUP

All registers of the chipsets are set to default values by the system BIOS. Usually, there is no need to modify these registers unless the configuration is changed. Since improper settings of these registers may cause the system malfunction, check your settings carefully before exit.

There are two menu to modify the registers of the chipset : ADVANCED CMOS SETUP and ADVANCED CHIPSET SETUP. In ADVANCED CMOS SETUP, the system BIOS allows you to modify some registers which are more likely to be changed if system configuration is modified. ADVANCED CHIPSET SETUP, on the other hand, allow you to modify those registers which are more unlikely to be changed.



SYSTEM BIOS

In ADVANCED CMOS SETUP, the main menu is shown as below:

SYSTEM BIOS

BIOS SETUP PROGRAM - ADVANCED CMOS SETUP
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Typematic Rate Programming	: Enabled	Video ROM Shadow C000,16K	: Disabled
Typematic Rate Delay (Msec)	: 500	Video ROM Shadow C400,16K	: Disabled
Typematic Rate (Chars/Sec)	: 15	Adapter ROM Shadow C800,16K	: Disabled
Above 1MB Memory Test	: Disabled	Adapter ROM Shadow CC00,16K	: Disabled
Memory Test Tick Sound	: Enabled	Adapter ROM Shadow D000,16K	: Disabled
Hit Message Display	: Enabled	Adapter ROM Shadow D400,16K	: Disabled
Hard Disk Type 47 RAM Area	: 0:300	Adapter ROM Shadow D800,16K	: Disabled
System Boot Up Num Lock	: On	Adapter ROM Shadow DC00,16K	: Disabled
Floppy Drive Seek At Boot	: Enabled	Adapter ROM Shadow E000,16K	: Disabled
Weitek Processor	: Absent	System ROM Shadow F000,16K	: Enabled
System Boot Up Sequence	: A:, C:	Cacheable Rom Area	: Video
System Boot Up CPU Speed	: High	Hidden Refresh	: Enabled
External Cache Memory	: Enabled		
Password Check Function	: Enabled		

SYSTEM BIOS



SYSTEM BIOS

After changing the registers' settings, test your system first to make sure that the settings are correct. It is likely that your system becomes unstable and you need to setup the registers again.

In this section, you simply use the up and down arrow keys to move between options and press PgUp/PgDn to scroll bit value. After you finish the Setup, press `Esc' to return to main menu and then select 'WRITE TO CMOS AND EXIT' to save the new setting in the CMOS RAM.

A short description follows for each of the options on the Advanced CMOS Setup Screen. If any problem in some options, press the <F1> Help Key.

Typematic Rate Programming :

By enabling this option, the user can adjust the rate at which a keystroke is repeated. The options "Typematic Rate Delay" and "Typematic Rate" also affect this rate. When a key is pressed and held down, the character appears on the screen and, after a delay set by the Typematic Rate Delay, it keeps on repeating at a rate set by the Typematic Rate Value. When two or more keys are pressed and held down simultaneously, only the last key pressed will be repeated at the typematic rate. This stops when the last key pressed is released, even if other keys are depressed.

SYSTEM BIOS

Above 1MB Memory Test :

If the option is enabled, the memory above 1 MB will be tested.

Memory Test Tick Sound :

This option will turn on or turn off the "ticking" sound during the memory test.

Hit Message Display :

If enabled, the following message will be shown after memory test :

"Hit if you want to run SETUP"

It allows you to enter Setup section.

Hard Disk Type 47 Data Area :

AMI BIOS SETUP features two user-definable hard disk types. Normally, the data for these disk types are stored at 0:300 in lower system RAM. However, if a problem occurs with some software regarding hard disk, try setting to `DOS 1 KB'. 1 KB in the main memory will be allocated for hard disk type storage and the main memory is reduced to 639 KB.

When the system shadow (F000) is enabled, the BIOS will add the user-defined hard disk type to the hard disk type table in the system BIOS. There is no need to store the data for the user-defined hard disk

SYSTEM BIOS

type in the separate area. So this option will be ignored.

Wait for F1 if Any Error :

The system BIOS execute a series of diagnostic tests on the system during boots-up. If non-fatal error has been detected and the system can still work, the BIOS will display appropriate error message followed by the following message :

"Press <F1> to continue"

If this option is disabled, BIOS will only display the appropriate error message but not the above statement for non-fatal error. This eliminate the need for any user intervention to a non-fatal error condition.

SYSTEM BIOS

System Boot Up Num Lock :

The "Num Lock" option on the keyboard is usually turned on after power on. This option allows you to turn the "num lock" off after power on. So you can use the arrow keys on the numeric keypad without pressing the "num lock" key.

Weitek Processor(s) :

These options allow the user to mark the Weitek numeric processor (WTL4167) as present or absent.

Floppy Drive Seek At Boot :

The default for this option is "Enabled". If disabled, it allows a fast boot.

System Boot Up Sequence :

This option allow you to choose which drive the system will boot from first. The default setting is 'A:, C:'. It allows you to boot from device A if necessary. However, it will directly boot from hard disk when selecting 'C:, A:'. The BIOS will not read the floppy disk A unless there is no drive C: installed. Thus it takes less time for boot up.

SYSTEM BIOS

External Cache Memory :

This option controls the secondary cache memory. If the secondary cache memory is installed, select "enable".

Internal Cache Memory :

This option controls the internal cache memory of 80486. Normally, the internal cache memory is enabled.

Password Checking Option :

The system may be configured so that user is required to enter a password every time the system boots, or whenever an attempt is made to enter the SETUP programs. The password function may be disabled, which means that the prompt will not appear under any circumstances.

The password check function is enabled or disabled in Advanced CMOS Setup. The password check function is enabled by choosing either "Always" or "Setup". If "Always" option is selected in Advanced CMOS Setup, user will be prompted for the password each time the system is powered on. If the "Setup" option is selected, user is requested to enter password each time an attempt is made to enter the Setup program.

If the CMOS is corrupted, the default password, if enabled, will be OCEAN.

Password may be changed if you hit <ENTER> at the <Change Password Option> in the main Setup screen. The following screen will then come up

SYSTEM BIOS

*BIOS SETUP PROGRAM - CHANGE PASSWORD
<C> 1990 American Megatrends Inc., All Rights Reserved*

Enter CURRENT Password :

<table border="1"><tr><td></td></tr></table>	

SYSTEM BIOS

You are requested to enter current password. If the current password has been entered correctly, the following screen will appear :

You may enter a password of not exceeding 6 characters in length. You are required to enter the new password twice.

SYSTEM BIOS

*BIOS SETUP PROGRAM - CHANGE PASSWORD
<C> 1990 American Megatrends Inc., All Rights Reserved*

Enter NEW Password :

<table border="1"><tr><td></td></tr></table>	

SYSTEM BIOS

Video,Adapter and System ROM shadow :

There are two options of shadow RAM for video adapter, seven options of shadow RAM for add-on card and one for the system BIOS. For the option System ROM, the content of the system at F000H segment BIOS is copied to the on board memory. For the option Video ROM, the video ROM at C0000H segment or C4000H segment are copied to memory. If you install an add-on card which ROM BIOS is locate at one of the Adapter ROM shadow options, you may select corresponding option to shadow this ROM. If there is any problem after enabling the shadow memory on the add-on card, it recommends to enable the shadow RAM function for system BIOS only.

Cacheable ROM area :

This option allow you to set the video BIOS, system BIOS, or both BIOS are cacheable. The default is disabled. If ROM BIOS is cacheable, the performance is better, but it is likely that the BIOS may be overwritten by software.

Hidden Refresh :

If enabled, the refresh operation of main memory will not suspend the CPU operation and the overall performance is better.

SYSTEM BIOS

(3) ADVANCE CHIPSET SETUP

SYSTEM BIOS

BIOS SETUP PROGRAM - ADVANCED CHIPSET SETUP
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DRAM Wait State : 0 W/S
Non-Cache Size-Block 0 : Disabled
Non-Cache Start-Block 0 : 000000
Cacheable Region : 64MB



SYSTEM BIOS

DRAM wait states :

Select 0 wait state with 70ns or faster DRAM and 1 wait state for 100 ns DRAM.

Check carefully whether your DRAM is suitable for the number of wait states you want to select. Improper setting can make the system malfunction. Since the specification of DRAM from different manufacturers may vary, you would better consult your local dealer for the detail information.

Non-cache Start and Size :

There is one non-cacheable block that can be defined by user. You need to specify the size and start address. The block size may be 64 KB, 128 KB, 256 KB or 512 KB. The start address is where the non-cacheable block will start in the main memory. Press 'PgUp' or 'PgDn' keys to change the address value to an appropriate value.

Cacheable Region :

This option define the upper bound of memory to be cached. You may set this option to a value not less than the size of total DRAM installed into the system.

**(4) AUTO CONFIGURATION WITH BIOS
DEFAULTS**

The Auto configuration with BIOS default is used to set the internal state of the system in option performance with high reliability. Once the Auto Configuration is applied, the user need not enter the ADVANCED CMOS SETUP. You will still need to set those options in the STANDARD CMOS SETUP after the Auto Configuration is used.

SYSTEM BIOS

(5) AUTO CONFIGURATION WITH POWER-ON DEFAULTS

The Auto configuration with Power-On default is used to set the internal state of the system with worst case default values. You may use this option to put the machine back to operation if the system perform erratically because of hardware problem.

(6) CHANGE PASSWORD

Please refer to sub-section of "Password Checking Option" in the "Advanced CMOS Setup" for detail information.

SYSTEM BIOS

(7) HARD DISK UTILITY

Below is the menu for Hard Disk Utility option.

SYSTEM BIOS

BIOS SETUP PROGRAM - HARD DISK UTILITY
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	Cylin	Head	WPcom	LZone	Sect	Size (MB)
Hard Disk C:Type : 47 USER TYPE	1314	7	1314	1314	17	76
Hard Disk D: Type : Not Installed						

Hard Disk Type can be changed from the STANDARD CMOS SETUP option in Main Menu

Hard Disk Format
Auto Interleave
Media Analysis

SYSTEM BIOS

There are three options in the hard disk utility :Hard Disk Format, Auto Interleave and Media Analysis.

For a new hard disk (drive), the manufacturer of the hard drive usually provides a list of "bad tracks" with the hard disk. Your hard disk manual might also include the optimum interleave factor.

In this case, assuming that you have a list of bad tracks and know the interleave factor, it will not be necessary to take the auto interleave and media analysis options. Simply follow the instructions in the Hard Disk Format. If you have a bad track list but have not been provided with the optimum interleave factor, follow the instructions in the Auto Interleave Section.

SYSTEM BIOS

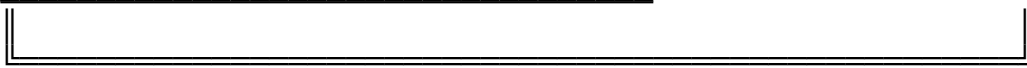
BIOS SETUP PROGRAM - HARD DISK UTILITY
<C> 1990 American Megatrends Inc., All Rights Reserved

	Cylin	Head	WPcom	LZone	Sect	Size (MB)
Hard Disk C:Type :47 USER TYPE	1314	7	1314	1314	17	76
Hard Disk D: Type : Not Installed						

Hard Disk Format

Disk Drive (C/D) ? C
Disk Drive Type ? 47
Interleave (1-16) ? 3
Mark Bad Tracks (Y/N) ?
Proceed (Y/N) ?

SYSTEM BIOS



Option 1 Hard Disk Format Utility

Use the Hard Disk Format option to integrate a new hard disk to the system, or to reformat a used hard disk which has developed some bad tracks. To find these bad patches on a used drive, select the Media Analysis option.

The value for Disk Drive is C for a C: Drive or D for a D: Drive. If two disk drives have been previously entered at the Standard CMOS Setup Screen, then the ID (C/D) will appear to the right of the question mark following the Disk Drive field. Choose which drive you wish to format by selecting the appropriate letter and pressing <ENTER>. If only one drive was selected at the Standard CMOS Setup Screen, the cursor will automatically be placed at the interleave prompt.

The Disk Drive Type is read from the CMOS. The

SYSTEM BIOS

interleave factor can be selected manually, or can be determined with the Auto Interleave feature of the SETUP program.

The hard drive usually provides a list of bad tracks. These tracks should be entered with this option, and they will then be marked as "bad" in order to prevent data from being stored there.

*The default for the Proceed prompt is <N> to prevent accidental formatting of the hard drive and subsequent loss of data. **Once this prompt is changed to <Y> and the <ENTER> key pressed, any data residing on the hard disk will be irrevocably lost.***

Make sure that your hard disk is allowed to be formatted. Some hard disks are formatted in the factory and will be malfunctioned if reformatted. Check your hard disk manual for more information.

Option 2 Auto Interleave Utility

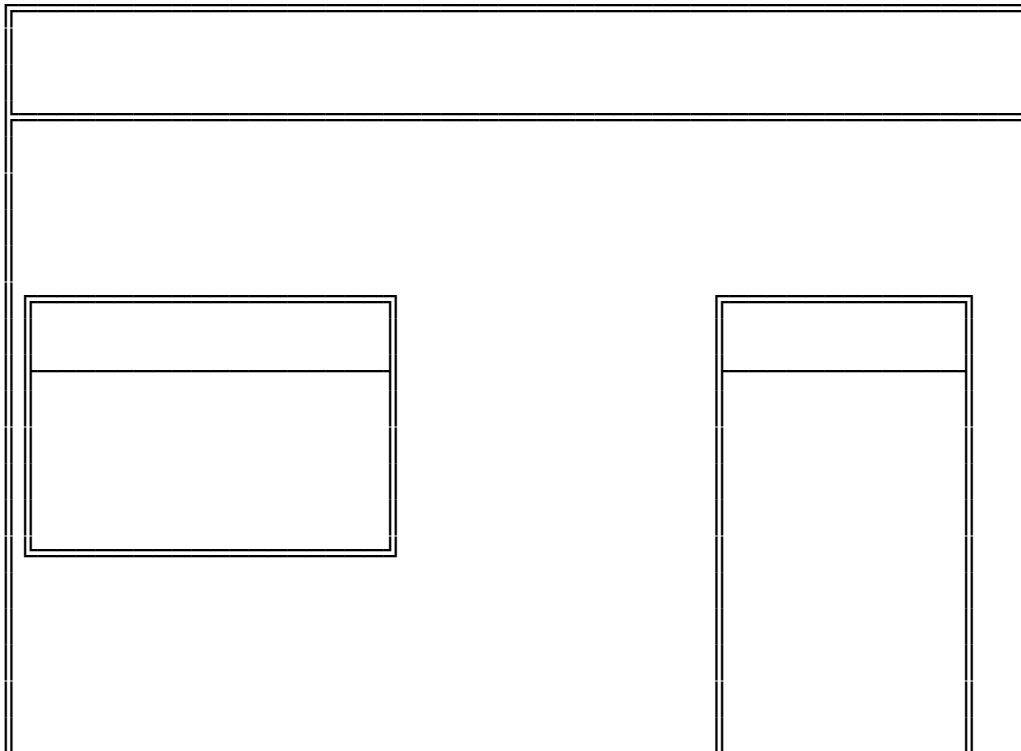
The Auto Interleave Utility determines the optimum interleave value by measuring the transfer rate for four different interleave values. The cylinders, head and sector formatted for each value will be displayed in the active box on the screen

SYSTEM BIOS

BIOS SETUP PROGRAM - HARD DISK UTILITY
<C> 1990 American Megatrends Inc., All Rights Reserved

	Cylin	Head	WPcom	LZone	Sect	Size (MB)
Hard Disk C:Type : 47 USER TYPE	1314	7	1314	1314	17	76
Hard Disk D: Type : Not Installed						

Auto Interleave		Bad Track %		
Disk Drive (C/D)	? C	Ms.	Cyln.	Head
Disk Drive Type	? 47			
Mark Bad Tracks (Y/N)	? N			
Proceed (Y/N)	?			



SYSTEM BIOS



SYSTEM BIOS

Option 3 Media Analysis Utility

The Media Analysis utility performs a series of tests to locate bad tracks on the hard disk. All bad tracks on the hard disk will be listed in the Bad Track List Box. Since this test writes to all cylinders and heads on the hard disk to verify any bad tracks, the test may require several minutes to complete.

SYSTEM BIOS

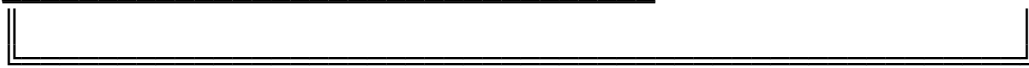
BIOS SETUP PROGRAM - HARD DISK UTILITY
<C> 1990 American Megatrends Inc., All Rights Reserved

	Cylin	Head	WPcom	LZone	Sect	Size (MB)
Hard Disk C:Type : 47 USER TYPE	1314	7	1314	1314	17	76
Hard Disk D: Type : Not Installed						

Media Analysis

Disk Drive (C/D) ? C
Disk Drive Type ? 47
Proceed (Y/N) ?

SYSTEM BIOS



SYSTEM BIOS

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Appendix B

EISA Configuration Utility

EISA SYSTEM CONFIGURATION

One of advantage of EISA over ISA is its ability of automatem system configuration to resolve conflict of resources (such as I/O ports, memory, interrupt lines, DMA channels) among system board and add on cards. This means an EISA system can be designed with no DIP switch and jumpers. Note that DIP switches and jumpers are still allowed on a EISA system.

EISA provide an unique product ID for each motherboard and add on card. During power up, the system BIOS on an EISA motherboard read the product ID from each device (including motherboard and each add on card) and compare with the product ID stored in an EISA Extended CMOS RAM and configure each device according to that specified during last time the EISA configuration utility was successfully run.

EISA CONFIGURATION

ECU FOR THE DRAGON EISA

DRAGON EISA 486 is shipped with a AMI ECU (EISA configuration utility diskette).

An AMI ECU diskette contains the following files :

- * CFG.EXE (the EISA configuration utility)*
- * EISACFG.HLP (AMI ECU Help file)*
- * some overlay files (with .OVR extension) that are re-written by AMI for some EISA product to fix into their overlay files requirements.*
- * several CFG files for OCEAN products.*

As you run the AMI ECU, the following files can be recreated :

- * .ISA files whenever an ISA adapter card is configured.*
 - * .CMS files, generated as a result of configuration process and store the configuration information.*
 - * .INF files, which is used by the "Display / Print" command of the ECU to recall detailed information of a configuration such as switch and jumper settings, software statements, connection statements, and resource allocation.*
-

EISA CONFIGURATION

INSTALLATION OF AMI ECU

1. *Install on hard disk*

- a. *Copy all files from the AMI ECU floppy diskette onto a subdirectory on the hard disk.*
- b. *Copy all CFG files to the same directory.*

2. *Install on floppy diskette*

You may need to run ECU from a floppy if the hard disk controller may be configured with ECU before it can be used. Refer to your hard disk controller manual whether they include a default mode that can be used with configuration.

- a. *Use a back up of you original AMI ECU floppy diskette as a working copy.*
- b. *Copy all CFG files to the working diskette.*

3. *System requirements*

The AMI ECU is able to run in a system that having the following minimum configuration:

- * *MS-DOS 3.2 or later*
 - * *640 KB of main memory*
 - * *a 1.2 MB floppy disk drive*
 - * *a hard disk drive, monitor and keyboard*
-

EISA CONFIGURATION

OPERATION OF AMI ECU

The AMI ECU is a menu driven utility. User may find it easy to use and master the utility without consult to a manual.

AMI ECU is invoked by typing CFG at DOS prompt. CFG accept no parameter nor switch.

Main menu is the first screen that comes up to you.

EISA CONFIGURATION

EISA CONFIGURATION UTILITY, Eval Release 1.4 - <C> 1991 American Megatrends Inc.
File Configure Display/Print Help Quit

F1 = Help = Move Enter = Select Esc = Exit

EISA CONFIGURATION

--

EISA CONFIGURATION

The five options that available from main menu are described one by one as below :

File :

use to load CFG files onto hard disk or back up configuratin information from hard disk onto floppy disk.

Configure :

configure an EISA system, check CFG file syntax, or write configuration information to CMOS RAM.

Display/Print :

display or print information (switch, jumper settings, software statements, connection statements, and resource allocation) about configuration saved.

Help :

about AMI ECU operation details.

Quit :

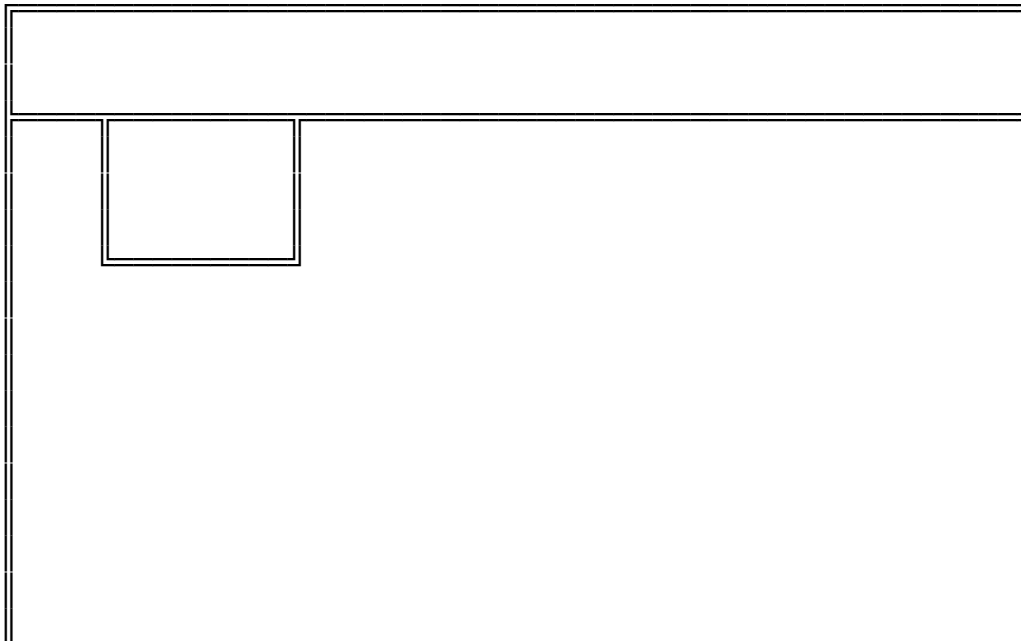
exit the AMI ECU and back to DOS prompt.

EISA CONFIGURATION

EISA CONFIGURATION UTILITY, Eval Release 1.4 - <C> 1991 American Megatrends Inc.
File Configure Display/Print Help Quit

Copy
Backup
About AMI ECU

F1 = Help = Move Enter = Select Esc = Exit
Copy CFG files from diskette



EISA CONFIGURATION

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FILE MENU

Options available from File menu :

- *File copy*
- *Backup*
- *About AMI ECU*

They are described one by one as below.

EISA CONFIGURATION

File Copy :

You may find these option useful if you want to copy CFG files onto ECU sub-directory without leaving the ECU utility. Alternately, you may use DOS COPY command to copy the necessary CFG files to the ECU sub-directory.

You may either use keyboard or a mouse to direct the ECU to copy the necessary CFG files.

Backup Configuration :

Backup configuration option store the CMS files and INF files to a floppy diskette. You may restore an old configuration, for example, after a battery failure, by choosing the Write Extended CMOS option from the configuration menu to write the content of CMS files onto the EISA extended CMOS RAM.

You may also use the back-up option to copy a configuration to another EISA system.

About the AMI ECU :

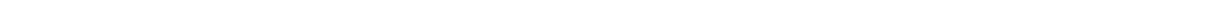
It shows some information about the AMI ECU utility.

CONFIGURATION OPTIONS MENU

There are five option available from the Configuration Option menu :

- *Config Option*
- *Define ISA Board Option*
- *Check CFG File*
- *Write Ext. CMOS*
- *Board ID Map*

They are described one by one as below.

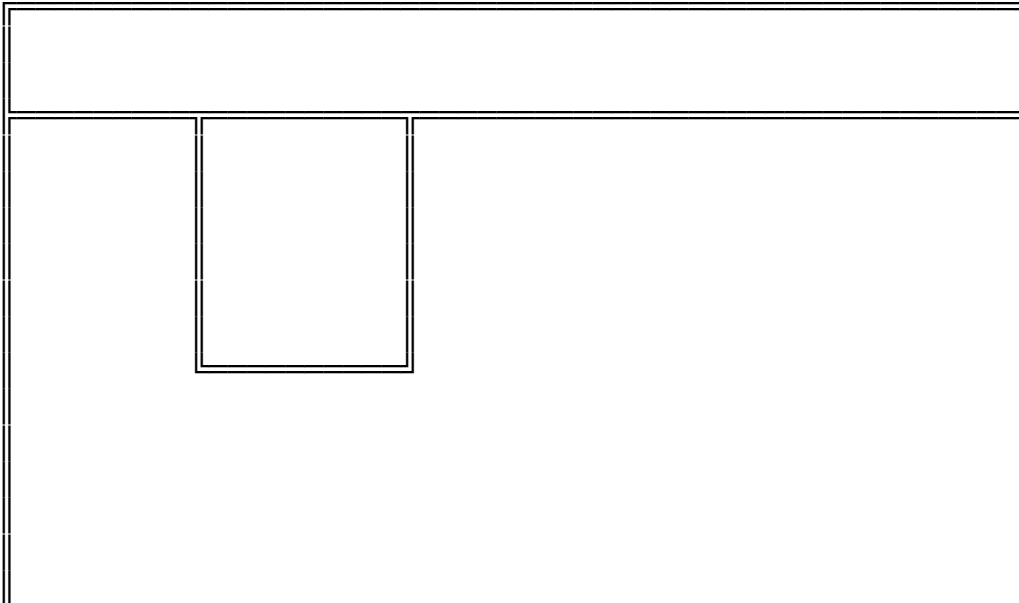


EISA CONFIGURATION

EISA CONFIGURATION UTILITY, Eval Release 1.4 - <C> 1991 American Megatrends Inc.
File Configure Display/Print Help Quit

Configure
Define ISA Board
Check CFG File
Write Ext. CMOS
Board ID Map

F1 = Help = Move Enter = Select Esc = Exit
Create a new configuration or modify an old configuration



EISA CONFIGURATION

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EISA CONFIGURATION

Config Option :

The config Option allow use to choose the three ranges of options for your configuration process.

1. Configuration Type

Configuration type can be

- *Create New Configuration or*
- *Modify Old Configuration.*

Choose "Create New Configuration" if you are going to begin a new configuration session.

Choose "Modify Old Configuration" if you are going to make change to a configuration that you created in some time ago.

2. Configuration Mode

In automatic mode, the ECU ask you a few essential questions and then perform the configuration on its own.

Manual mode allow you to alter the advanced features such as function choice selection, resource allocation editing, add board and remove board.

Local mode allow you to create configuration information for this computer. The configuration information will be stored in EISA extended CMOS RAM, CMS file and INF file.

Remote mode generate configuration information for other computer. The EISA extended CMOS RAM is not modified. The CMS and INF files generated may be moved to other computer via the backup option

EISA CONFIGURATION

in the File menu.

3. Which CFG/CMS Files to Configure

You need to specify which CFG files to be used if "Create New Configuration" is chosen. You may choose from the Configure Option menu to use one of the follow CFG files :

- *Use CFG files for installed boards*
- *Use filenames listed in CFGLIST file*
- *Select files one by one*
- *Use all CFG files in this directory*

You need to specify which CMS file to be modified if "Modify Old Configuration" is chosen. There are two options :

- *Use default CMS name (ECU look for a CMS file having same name as the motherboard)*
- *Select CMS file from directory listing*
- *Enter CMS file name using keyboard.*

After you have chosen all ranges of option in the Configure Option, move the cursor to <OK> and then hit <Enter>. Then the ECU will guide you to go through a series of screen to

- *select a slot for each adapter card it can detect*
- *allow you to add, remove, move adapter card around the slots.*
- *modified the configuration for each adapter card.*
- *save the configuration information generated.*
- *display/print the configuration information.*

Define ISA Board :

Most ISA adapter card does not come with an CFG file. Without a CFG file, the ECU cannot reserve

EISA CONFIGURATION

system resources automatically for ISA adapter cards. ISA cards must be configured manually. Manual mode allow you to edit the configuration settings for all adapter cards in the system and make sure that there is no conflict between EISA and ISA adapter cards.

Check CFG File :

Check syntacx for one or more CFG files and report for any error.

EISA CONFIGURATION

Write Ext CMOS :

Write the content of a CMS file onto the EISA extended CMOS RAM. This will destroy any previous configuration information that is stored in the system's CMOS RAM.

Board ID Map :

This option display a table of all EISA adapter cards in the system.

EISA CONFIGURATION

DISPLAY/PRINT MENU

Display or Print configuration information such as board information, switches & jumpers settings, software statements, connection statements, DMA resources, IRQ resources, port resources, and memory resources allocations. The output may be LPT1, a disk file, or screen.

EISA CONFIGURATION

USING HELP MENU

Help may access the Help function any time by hitting the <F1> function key.

EISA CONFIGURATION

QUIT MENU

Conclude the ECU utility and return to the DOS prompt.

EISA CONFIGURATION

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Appendix C

Operation and Maintenance

STATIC ELECTRICITY

When installing or removing any add-on card, DRAM module or coprocessor, you should discharge the static electricity on your body. Static electricity is dangerous to electronic device and can build-up on your body. When you touch the add-on card or motherboard, it is likely to damage the device. To discharge the static electricity, touch the metal of your computer. When handling the add-on card, don't contact the components on the cards or their "golden finger". Hold the cards by their edges.

KEEPING THE SYSTEM COOL

The motherboard contains many high-speed components and they will generate heat during operation. Other add-on cards and hard disk drive can also produce a lot of heat. The temperature inside the computer system may be very high. In order to keep the system running stably, the temperature must be kept at a low level. A easy way to do this is to keep the cool air circulating inside the case. The power supply contains a fan to blow air out of the case. If you find that the temperature is still very high, it would be better to install another fan inside the case. Using a larger case is recommended if there are a number of add-on cards and disk drives in the system.

CLEANING THE "GOLDEN FINGER"

Whenever inserting an add-on card to the motherboard, make sure that there is no dirt on the "golden finger" of the add-on card. If not, the contact between the "golden finger" and the slot may be poor and thus the add-on card may not work properly. Use a pencil eraser to clean the "golden finger" if dirt is found.

CLEANING THE MOTHERBOARD

The computer system should be kept clean. Dust and dirt is harmful to electronic devices. To prevent dust from accumulating on the mother-board, installing all mounting plates on the rear of the case. Regularly examine your system, and if necessary, vacuum the interior of the system with a miniature vacuum.

Appendix D

Troubleshooting

MAIN MEMORY ERROR

After power up, the monitor remains blank, and there are beep sounds indicating a main memory failure. In this case, turn off the power and remove all SIMM modules. Carefully place the modules back to the sockets and make sure that all the modules are locked by the locking latches firmly.

In some other cases, the total memory found by the BIOS is different from the actual amount of memory on board. (Note that 128K bytes memory is reserved for the shadow RAM function and will not be counted by the BIOS). It is also a memory failure and you can follow the instruction above.

CACHE MEMORY FAILURE

If the system hangs after memory test, it is likely that the cache memory has some problems when the secondary cache memory card is installed. Maybe some of the SRAMs are damaged or the contact of the IC pins is poor. Try to press the SRAM to make sure that the SRAMs are inserted in the sockets, or examine the SRAM to see whether any pins are bent under or out. If the bent pins are found, remove the SRAM, straighten the pin and place the SRAM again. You may also check the BIOS setup of the cache configuration. If the cache controller is enabled, you should select chipset's cache controller. Otherwise, the system will fail.

IMPROPER SETTING OF WAIT STATE

If the system hangs after memory test, another possible cause is the improper setting of the wait state for memory operation. The number of wait state must match the speed of the DRAM. Reset the CMOS RAM and set up the wait state. Try to increase the number of wait state.

Appendix E

System Board Layout
