Alpha PCI 64–275

User's Manual

Order Number: EK–AL275–UM. A01

This manual describes the Alpha PCI 64–275 motherboard, order number EBP30–AN, configured for the Microsoft Windows NT operating system.

Revision/Update Information: This is a new manual.

Digital Equipment Corporation
Maynard, Massachusetts

April 1996

This document was prepared using VAX DOCUMENT, Version 2.1.

Contents

Index

Figures

Tables

About This Manual

This manual describes Digital's Alpha PCI 64–275 motherboards.

Audience

The target audience is the embedded and realtime technical OEM requiring higher performance than is available from PCs using other architectures. This guide is to assist users of the Alpha PCI 64–275 in installing the board and populating it with memory modules and peripheral cards.

Scope

This guide describes the features, configuration, and installation of the Alpha PCI 64–275. This guide does not include bus specifications (for example, PCI or ISA buses). Additional information is available in the appropriate vendor and IEEE specifications. See Appendix B for information about ordering additional documentation.

Content

This guide contains the following chapters and appendixes:

- Chapter 1, Alpha PCI 64–275 Introduction, is an overview of the Alpha PCI 64–275, including its components, uses, and features.
- Chapter 2, Board Jumpers and Connectors, describes the user environment configuration; board connectors and functions; jumper functions; and identifies jumper and connector locations.
- Chapter 3, Starting and Using the Alpha PCI 64–275, lists additional hardware and software requirements, provides information on how to configure the hardware and software, and describes the board startup procedures.
- Chapter 4, Functional Elements, describes some of the functional elements of the Alpha PCI 64–275, such as, interrupt assignments, flash ROM contents, and power distribution.

- Chapter 5, Board Requirements and Parameters, describes the Alpha PCI 64–275 power and environmental requirements, and identifies major board components.
- Appendix A, Components and Associated Literature, lists suggested supporting components that are available from Digital, such as CDROMs, disk, tapes, modems, and so forth.
- Appendix B, Additional Documentation, gives addresses for ordering documentation from other vendors.

Document Conventions

This section provides the conventions used in this document.

Caution: Cautions indicate potential damage to equipment or data.

Note: Notes provide additional information.

Numbering: All numbers are decimal or hexadecimal unless otherwise indicated. In case of ambiguity, a subscript indicates the radix of nondecimal numbers. For example, 19 is a decimal number, but 19_{16} and 19A are hexadecimal numbers.

Extents: Extents are specified by a single number, or a pair of numbers in angle brackets (< >) separated by a colon (:) and are inclusive. For example, bits <7:3> specify an extent including bits 7, 6, 5, 4, and 3. Multiple bit fields are shown as extents.

Register Figures: Register figures have bit and field position numbering starting at the right (low-order) and increasing to the left (high-order).

Signal Names: Signal names in text are printed in boldface lowercase type. For example, " . . . bits **data<127:0>** are delivered to the Bcache SIMM connectors . . . "

1

Alpha PCI 64–275 Introduction

This chapter provides an overview of the Alpha PCI 64–275, its components, features, and uses.

1.1 The Alpha PCI 64–275

The Alpha PCI 64–275 motherboards use the the Alpha 21064A processor chip operating at 275MHz and Digital's 21072 chip set. The boards support the Windows NT operating system (EBP30-NA, with ARC firmware console).

1.2 Board Components and Features

The Alpha PCI 64–275 design uses Digital's Alpha 21064A processor and 21072 chip set combined with industry-standard support chips. The functional block diagram in Figure 1–1 illustrates the functional components of the board. The following sections further define the components.

1.2.1 Memory Subsystem

The Alpha PCI 64–275 memory subsystem supports industry-standard single inline memory modules (SIMMs) with a 128-bit data bus structure. Each SIMM must be 36 bits wide, with 32 data bits, 1 parity bit, and 3 unused bits with an access time of 70ns or less. The Alpha PCI 64–275 can address up to 512MB of memory in two banks of four SIMMs. Figure 1–2 shows the maximum and minimum SIMM bank layouts. The Alpha PCI 64–275 supports the following SIMM sizes:

1M x 36 2M x 36 4M x 36 8M x 36 16M x 36

The memory size required depends on the operating system you use and your application.

1.2 Board Components and Features

Figure 1–1 Alpha PCI 64–275 Functional Block Diagram

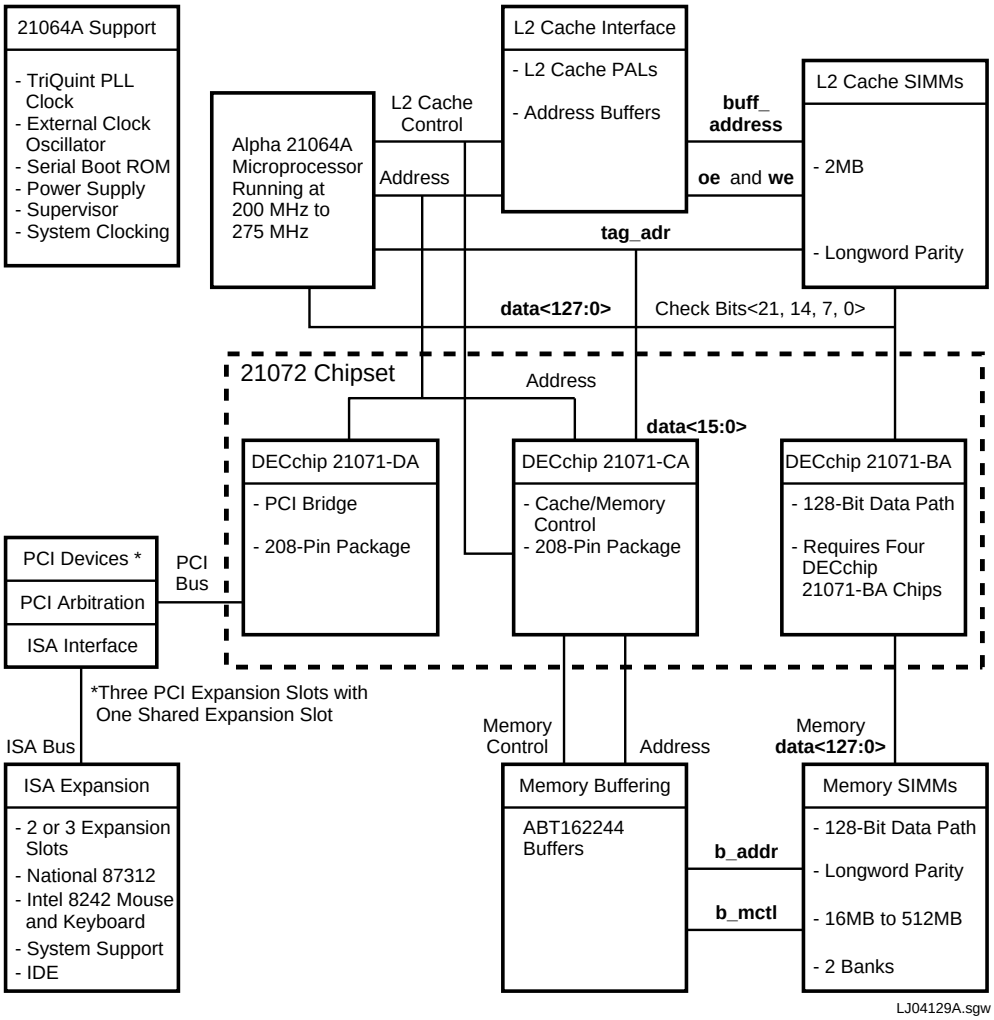
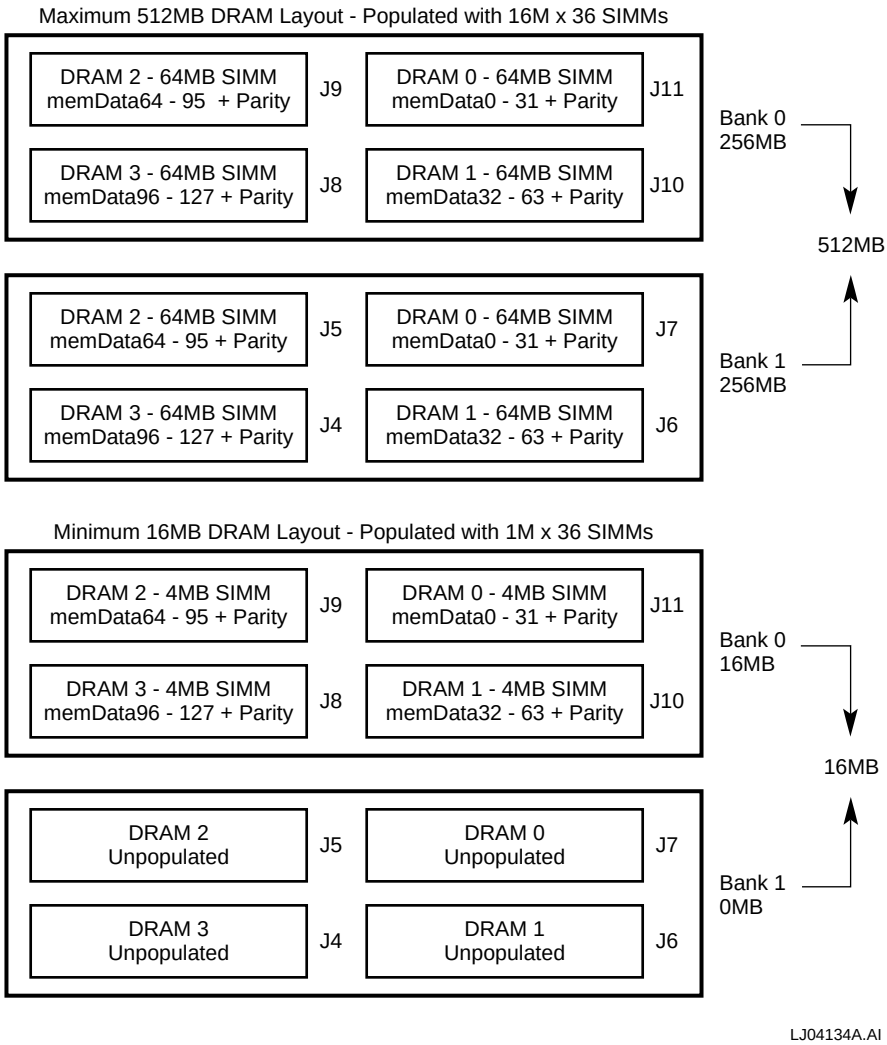


Figure 1–2 Maximum and Minimum SIMM Bank Layouts



1.2.2 DECchip 21072 Support Chipset

The 21064A is supported by a DECchip 21072 ASIC chipset (21072), with a 128-bit memory interface. The chipset consists of the following three chips:

- DECchip 21071-CA (21071-CA) provides the interface from the CPU to cache and main memory, and includes the cache and memory controller.
- DECchip 21071-BA (21071-BA) provides a 32-bit data path from the CPU to memory and I/O. Four chips provide the 128-bit interface.
- DECchip 21071-DA (21071-DA) provides an interface from the CPU to the peripheral component interconnect (PCI) bus.

The chipset includes the majority of functions required for a high-performance PC or workstation, requiring minimum discrete logic on the Alpha PCI 64–275. The chipset provides flexible and generic functions to allow its use in a wide range of applications.

For more information on the DECchip 21072 chipset, see the *DECchip 21071 and DECchip 21072 Core Logic Chipsets Data Sheet*.

1.2.3 PAL Control Set

The Alpha PCI 64–275 contains a 4-PAL control set and includes the following:

- Two 16V8-5 PALs provide L2 cache output-enable and write-enable functions.
- One 22V10-25 PAL provides interrupt address decode functions and utility bus (Ubus) control.
- One MACH210-20 PAL provides the PCI and ISA interrupts.

1.2.4 Level 2 Cache Subsystem Overview

Alpha PCI 64–275 motherboards are sold with the external level 2 (L2) cache subsystem configured with 2MB cache memory using two 1MB dual inline memory modules (DIMMs) with an access time of 12ns. You can increase or decrease the L2 cache size by replacing the DIMMs with other sizes and changing onboard hardware and software jumpers. Your application's cache hit rate may improve with faster or more cache. Contact your Digital Field Application Engineer (FAE) or your local sales representative for assistance.

Table 1–1 L2 Cache SIMM Sizes

L2 Cache Size	Static RAM Access Times
512KB	6 ns, 8 ns, 10 ns, 12 ns, 15 ns
2MB[1]	6 ns, 8 ns, 10 ns, **12 ns**[1], 15 ns
8MB	6 ns, 8 ns, 10 ns, 12 ns, 15 ns

[1]Default as shipped

1.2.5 Clock Subsystem Overview

The clock subsystem provides clocks to the 21072 chipset and PCI devices. Two oscillators provide clocks for the ISA and combination chip functions.

1.2.6 PCI Interface Overview

There are four 32-bit PCI slots available, with three slots dedicated to PCI and one shared PCI/ISA slot (see Table 2–3). The PCI bus interface operates at 30.5MHz, which is defined by the 21064A processor's clock speed.

1.2.7 ISA Interface Overview

The ISA interface provides an expansion bus and the following board support functions:

- Mouse and keyboard controller functions provided through an Intel 8242 chip
- A National 87312 chip used as the combination chip providing a diskette controller; two universal asynchronous receiver–transmitters (UARTs); an integrated device electronics (IDE) interface; a bidirectional parallel port; and an interface to the utility bus (Ubus) for ISA interrupts and jumper status
- A time-of-year (TOY) function provided by a Dallas Semiconductor DS1287 chip
- A 1MB flash ROM memory using the Intel 28F008SA chip

The ISA bus has two dedicated expansion slots and one shared expansion slot with the PCI bus. (See Table 2–3.)

1.2.8 Software Support

The Alpha PCI 64–275 supports the Windows NT operating system through an ARC firmware console. This console is resident on the module in 1MB of flash ROM. In addition to supporting the operating system, the console provides code for power-up testing, initializing, and a debug monitor. Section 4.4 describes the flash ROM in more detail.

The basic debug monitor supports the following functions:

- Download files through serial port, I/O diskette, and optional Ethernet port.
- Load data from the flash ROM through the debug monitor to selected cache locations.
- Examine and deposit the Alpha PCI 64–275 system register, 21064A internal processor registers (IPRs), and I/O mapped registers.
- Examine and modify DRAM and I/O mapped memory.
- Disassemble CPU instructions in memory.
- Transfer control to programs in memory.
- Perform native debugging, including breakpoints and single stepping.
- Perform full source-level debugging, using DECladebug running on a host communicating through an Ethernet connection.

A serial ROM (SROM) contains the 21064A initialization code. When **reset** is deasserted, the contents of the SROM are read into the 21064A internal cache (Icache) and are executed to perform initialization. After initialization, code is loaded from the flash ROM to memory, then control is transferred to the code in memory.

1.2.9 Component Layout

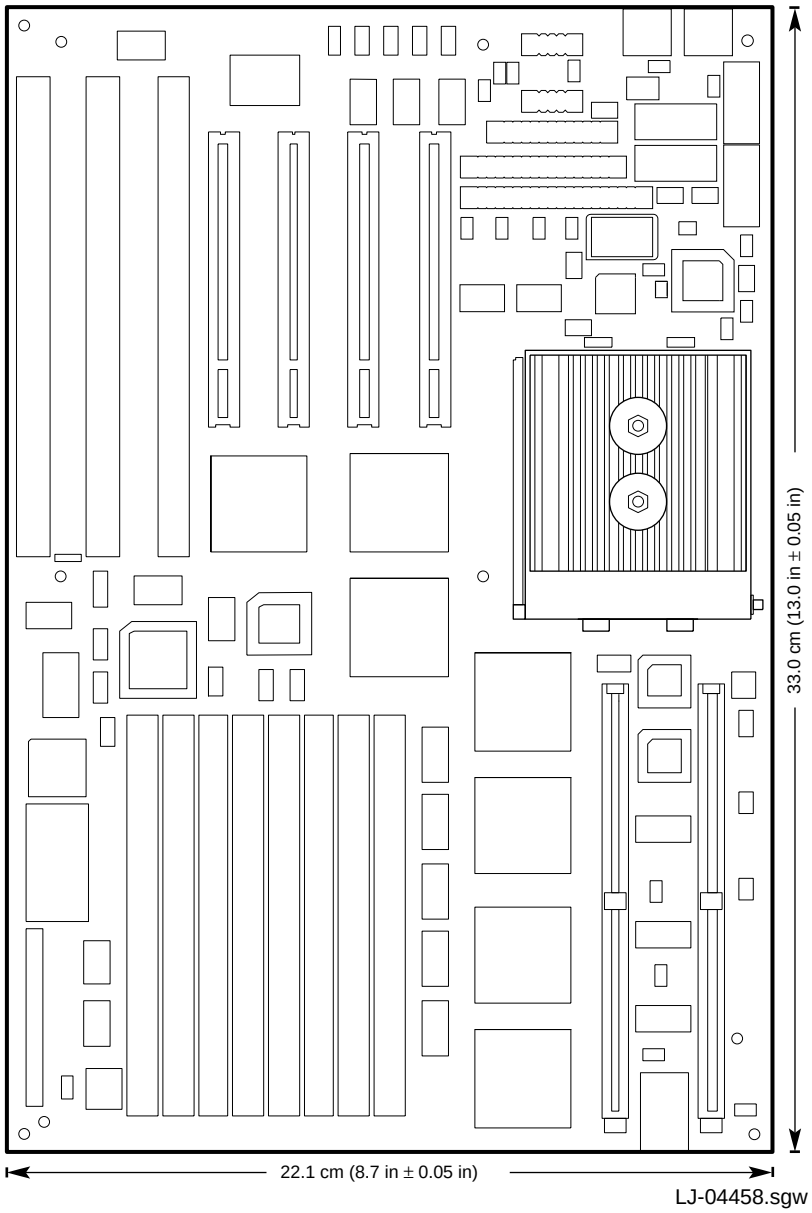
Figure 1–3 shows the Alpha PCI 64–275 board component layout and dimensions.

1.2.10 Board Summary

Table 1–2 lists the physical, performance, and operating characteristics of the Alpha PCI 64–275.

1.2 Board Components and Features

Figure 1–3 Alpha PCI 64–275 Component Layout and Board Dimensions



1.2 Board Components and Features

Table 1–2 Alpha PCI 64–275 Summary

Characteristic	Description		
Operating Systems			
Supported operating systems	Microsoft Windows NT		
Board Characteristics			
CPU and clock speed	Alpha 21064A at 275 MHz		
Instruction issue	Up to 2 instructions issued per clock cycle		
Word size	64 bits		
Address size	34-bit physical address, 43-bit virtual address		
Floating-point format	VAX (F and G) and IEEE (S and T) data types		
Memory (DRAM)[1]	Minimum DRAM 16MB plus parity Maximum DRAM 512MB plus parity		
Memory (ROM)	1MB flash ROM		
External L2 cache	Configurable for 512KB, **2MB** (default), 8MB (128-bit data)		
Memory bus width	128 bits plus parity		
Performance metrics			
	Cache	**SPECint92**	**SPECfp92**
	512KB @15 ns	176	217
	2MB @12 ns (default)	**193**	**259**
	2MB @8 ns	205	272

[1]Minimum DRAM required:
16MB for Microsoft Windows NT
32MB for Digital UNIX

(continued on next page)

Table 1–2 (Cont.) Alpha PCI 64–275 Summary

Graphics	
Graphics options	The Alpha PCI 64–275 supports a wide variety of PCI- and ISA-based graphics options, such as those listed in Appendix A. Look at the Microsoft Windows NT hardware compatibility listing for detailed option support information.
Input/Output	
Input device interfaces	PS/2 style keyboard and mouse
Serial	Two RS423-compatible (9-position) serial communications ports
Parallel	One parallel (Centronics compatible) communications port
Bus options	Total of 6 option slots
PCI bus	Supports four 5-V/32-bit PCI option slots at 30.5 MHz maximum–one long and three short cards
ISA bus	Supports three 16-bit ISA option slots plus one shared PCI /ISA slot
IDE	One IDE interface supporting up to 2 drives
Diskette	One 82077-compatible diskette controller supporting up to 2 drives with 1.44MB and 2.88MB formats
Physical Characteristics	
Form factor	Baby-AT-size board
Width/depth	22.1 cm (8.7 in) × 33.0 cm (13.0 in)
Weight	840 grams (1.85 lb) with high-profile heat sink

(continued on next page)

1.2 Board Components and Features

Table 1–2 (Cont.) Alpha PCI 64–275 Summary
Environmental Characteristics (Operating)

Temperature	10°C to 40°C (50°F to 104°F) ambient on the board
Temperature change rate (maximum)	20°C/hr (36°F/hr)
Relative humidity Maximum wet bulb Minimum dew point	10%–90% noncondensing 32°C (90°F) 2°C (36°F)
EMC compliance	Compliance certification is the responsibility of the system integrator. The Alpha PCI 64–275 was tested in industry-representative enclosures to prove feasibility of emissions compliance.
CE compliance	The Alpha PCI 64–275 carries CE certification. The module has a certification label.
Shock and vibration	Passing of shock and vibration tests is dependent on the method used to mount the Alpha PCI 64–275 board, the design of the enclosure, and how the enclosure is supported. Testing is the responsibility of the system integrator.

2

Board Jumpers and Connectors

The Alpha PCI 64–275 uses jumpers to implement variations in clock frequency and L2 cache size and speed. These jumpers must be configured for the user's environment. Onboard connectors are provided for the I/O, memory SIMMs, serial and parallel peripherals, integrated device electronics (IDE) devices, and L2 cache SIMMs.

2.1 Configuration Jumpers

The software and hardware configuration jumpers are identified in Figures 2–1 and 2–2, and are described in Tables 2–1 and 2–2.

2.1.1 Software Configuration Jumpers

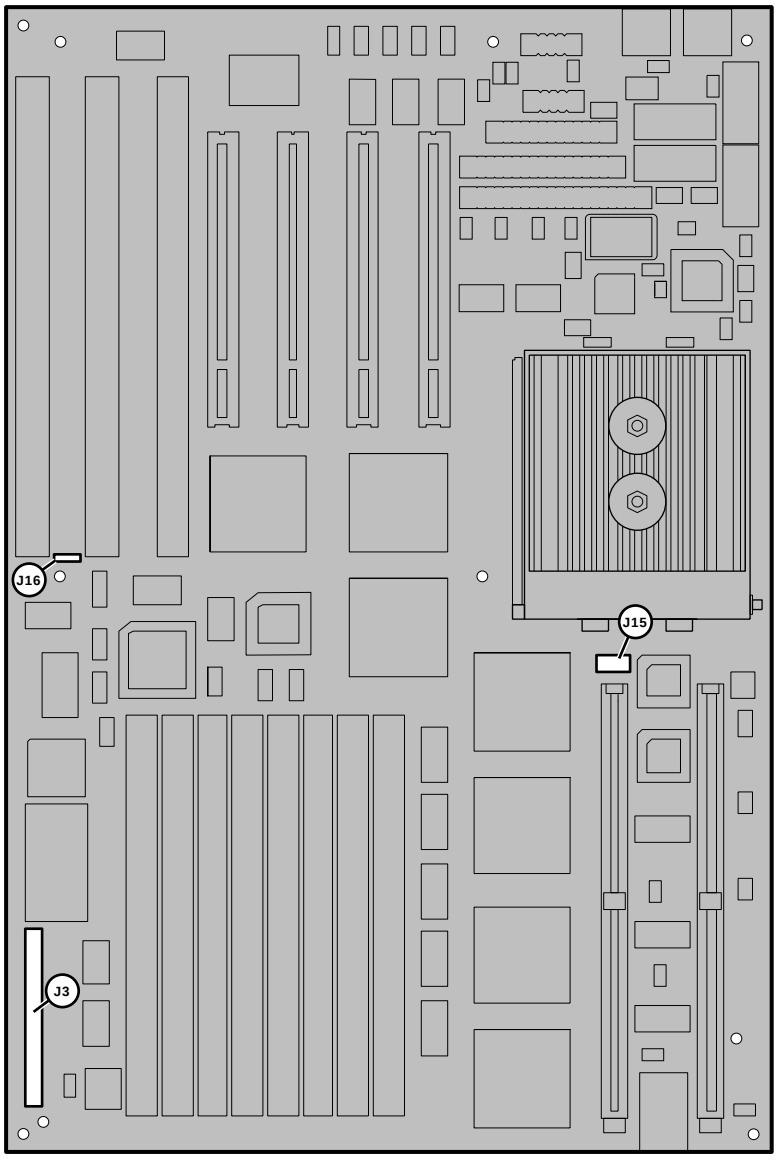
The software configuration jumpers are completely programmable. Each jumper position is described in Table 2–1.

The SROM code defines the software configuration jumpers **sp_bit<7:0>**, as shown in Figure 2–2 (see also Chapter 4).

The board ships with the jumpers listed in Tables 2–1 and 2–2 in the default position.

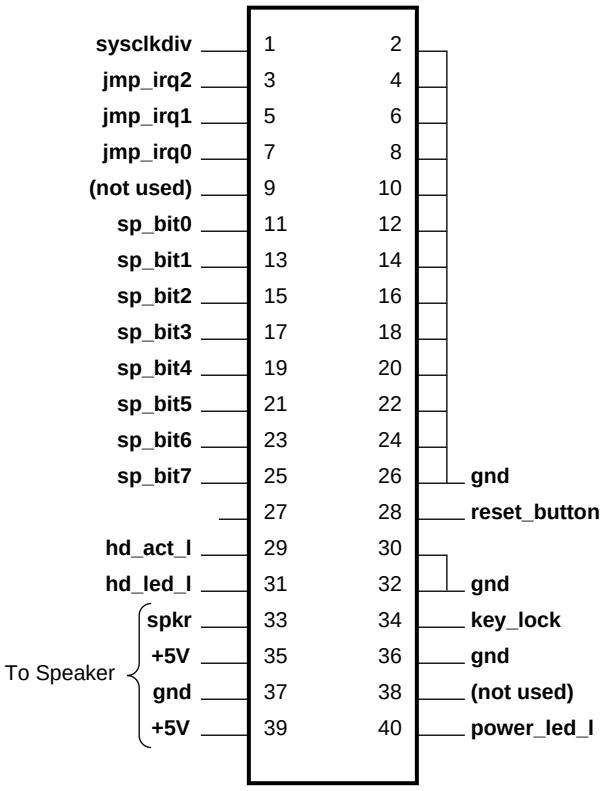
2.1 Configuration Jumpers

Figure 2–1 Alpha PCI 64–275 Board Jumpers



LJ-04459.AI5

Figure 2–2 J3 Jumpers/Connectors



LJ-04132.SW

2.1 Configuration Jumpers

Table 2–1 Jumper Position Descriptions

Select Bit	Register Bit Name	Function
sp_bit7	BOOT_OPTION	Jumper out—Boot first image in flash ROM. Jumper in (**default**)—Boot one of several alternate images in flash ROM as specified by NVRAM location 3F in TOY RAM.
sp_bit6	MINI_DEBUG	Jumper out (**default**)—Boot selected image in flash ROM. Jumper in—Trap to SROM debug port (J2).
sp_bit<5:3>	BC_SPEED<2:0>	L2 cache speed selection is shown here.

BC_SPEED <2> J3-21	BC_SPEED <1> J3-19	BC_SPEED <0> J3-17	L2 Cache Access Time
In	In	In	Reserved
In	In	Out	6 ns
In	Out	In	8 ns
In	Out	Out	10 ns
Out	In	In	**12 ns** (default)
Out	In	Out	15 ns
Out	Out	In	Reserved
Out	Out	Out	Reserved

(continued on next page)

Table 2–1 (Cont.) Jumper Position Descriptions

Select Bit	Register Bit Name	Function
sp_bit<2:0>	BC_SIZE<2:0>	L2 cache size selection is shown here.

BC_SIZE <2> J3-15	<1> J3-13	<0> J3-11	L2 Cache Size
In	In	In	Disables L2 cache
In	In	Out	512KB
In	Out	In	1MB
In	Out	Out	**2MB** (default)
Out	In	In	4MB
Out	In	Out	8MB
Out	Out	In	Reserved
Out	Out	Out	Reserved

2.1.2 Hardware Configuration Jumpers

Hardware configuration jumpers are shown in Figure 2–1 and are described in Table 2–2.

Table 2–2 Alpha PCI 64–275 Board Jumpers

Connector	Pins	Description
		L2 Cache Address Lines
J15	4	**Adr<22:19>** L2 cache; pins 22:19 are identified on the board. Pin 19 corresponds to J15-1, and so forth.

J15-1 Adr19	J15-2 Adr20	J15-3 Adr21	J15-4 Adr22	Size
Out	Out	Out	Out	512KB
In	Out	Out	Out	1MB
In	In	Out	Out	**2MB** (default)
In	In	In	Out	4MB
In	In	In	In	8MB

		Flash ROM
J16	3	Flash ROM update enable/disable connector. Pin 1 of J16 is identified on the board as pin 7; pin 3 is identified as pin 9. Pin 2 is center. Jumper from pin 1 to pin 2 disables flash ROM update. Jumper from pin 2 to pin 3 enables flash ROM update (**default**).

(continued on next page)

Table 2–2 (Cont.) Alpha PCI 64–275 Board Jumpers

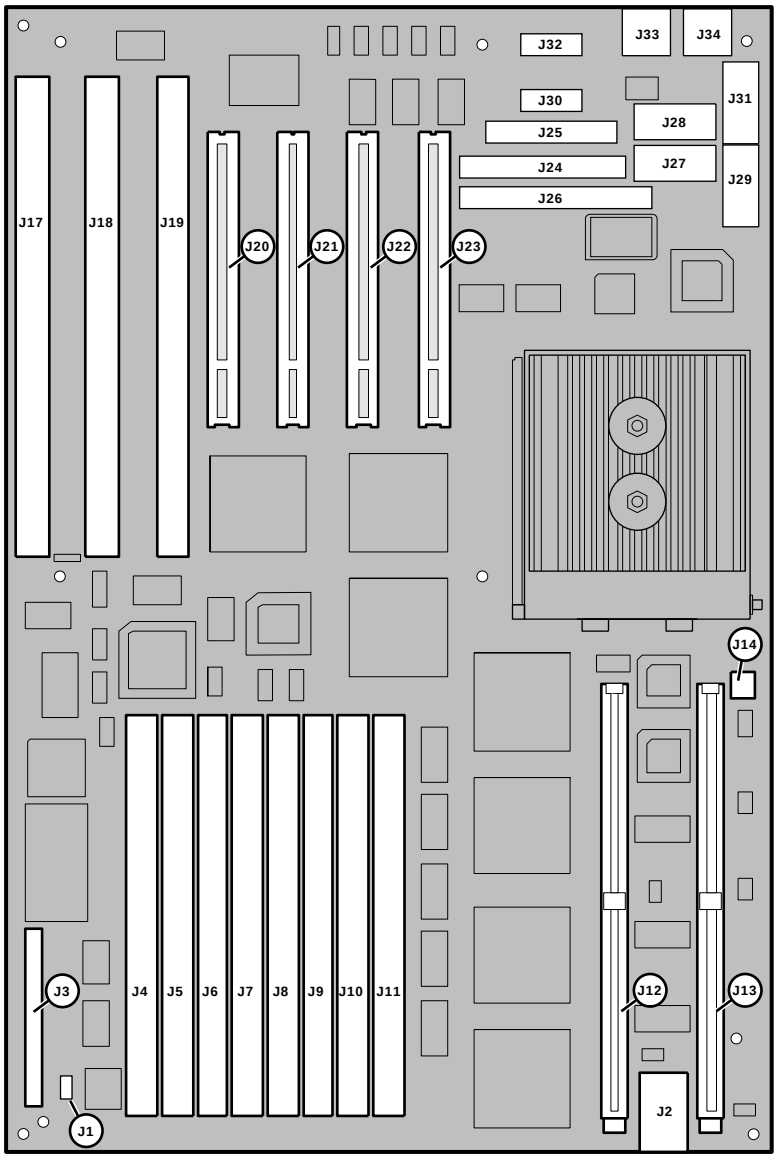
Connector	Pins	Description				
		Board Clock Functions				
J3	4	**21064A** CPU clock divisor selection.				
		J3-1 sysclkdiv	**J3-3 jmp_irq2**	**J3-5 jmp_irq1**	**J3-7 jmp_irq0**	**Divisor**
		In	In	In	In	2
		In	In	In	Out	3
		In	In	Out	In	4
		In	In	Out	Out	5
		In	Out	In	In	6
		In	Out	In	Out	7
		In	Out	Out	In	8
		In	Out	Out	Out	9
		Divisor 9 is used for 275 MHz (default).				
		Out	In	In	In	10
		Out	In	In	Out	11
		Out	In	Out	In	12
		Out	In	Out	Out	13
		Out	Out	In	In	14
		Out	Out	In	Out	15
		Out	Out	Out	In	16
		Out	Out	Out	Out	17

2.2 Alpha PCI 64–275 Board Connectors

The module connectors are shown in Figure 2–3 and are described in Table 2–3.

2.2 Alpha PCI 64–275 Board Connectors

Figure 2–3 Alpha PCI 64–275 Board Connectors



LJ-04457.AI5

2.2 Alpha PCI 64–275 Board Connectors

Table 2–3 Module Connector Descriptions (See Figure 2–3)

Connector	Pins	Description
		PCI Slots
J23	124	PCI expansion slot 3
J22	124	PCI expansion slot 2
J21	124	PCI expansion slot 1
J20	124	PCI expansion slot 0 (shared slot)
		ISA Slots
J19	98	ISA expansion slot 2 (shared slot)
J18	98	ISA expansion slot 1
J17	98	ISA expansion slot 0
		L2 Cache SIMM Slots
J13	160	L2 cache SIMM slot 1, **data<127:64>**
J12	160	L2 cache SIMM slot 0, **data<63:00>**
		Keyboard Connector
J33	6	Keyboard connector
		Mouse Connector
J34	6	Mouse connector

(continued on next page)

2.2 Alpha PCI 64–275 Board Connectors

Table 2–3 (Cont.) Module Connector Descriptions (See Figure 2–3)

Connector	Pins	Description
		Memory SIMMs
J11	72	Bank 0, DRAM 0 SIMM
J10	72	Bank 0, DRAM 1 SIMM
J9	72	Bank 0, DRAM 2 SIMM
J8	72	Bank 0, DRAM 3 SIMM
J7	72	Bank 1, DRAM 0 SIMM
J6	72	Bank 1, DRAM 1 SIMM
J5	72	Bank 1, DRAM 2 SIMM
J4	72	Bank 1, DRAM 3 SIMM
		SROM Test
J2	6	SROM test data serial port input/output connector **Note:** This connector can be used as a terminal port for the Mini-Debugger.
		National 87312 Connectors
J25	26	Combination chip parallel port connector. Pin 1 is identified on the board with a **v** symbol.
J26	40	IDE supports two devices. Pin 1 is identified on the board with a **v** symbol.
J32	10	Combination chip serial communication port 1 (COM1) connector. Pin 1 is identified on the board with a **v** symbol. **Note:** This connector can be used as a terminal port for the Debug Monitor.
J30	10	Combination chip serial communication port 2 (COM2) connector. Pin 1 is identified on the board with a **v** symbol.
J24	34	Combination chip diskette drive connector. Pin 1 is identified on the board with a **v** symbol.

(continued on next page)

Table 2–3 (Cont.) Module Connector Descriptions (See Figure 2–3)

Connector	Pins	Description
		Power Connectors
J27	6	Module power connector (GND, +3.3 V)

Pin	Voltage/Signal
1	Ground
2	Ground
3	Ground
4	+3.3 V
5	+3.3 V
6	+3.3 V

J28 6 Module power connector (+3.3 V, GND)

Pin	Voltage/Signal
1	+3.3 V
2	+3.3 V
3	+3.3 V
4	Ground
5	Ground
6	Ground

(continued on next page)

2.2 Alpha PCI 64–275 Board Connectors

Table 2–3 (Cont.) Module Connector Descriptions (See Figure 2–3)

Connector	Pins	Description
J29	6	Module power connector (GND, –5 V, +5 V)

Pin	Voltage/Signal
1	Ground
2	Ground
3	–5 V
4	+5 V
5	+5 V
6	+5 V

Connector	Pins	Description
J31	6	Module power connector (GND, +12 V, –12 V, +5 V, **p_dcok**)

Pin	Voltage/Signal
1	**p_dcok**
2	+5 V
3	+12 V
4	–12 V
5	Ground
6	Ground

Note: Power for the Alpha PCI 64–275 is provided by a user-supplied, standard PC power supply that includes 3.3 Vdc. Digital does not provide this power supply.

Connector	Pins	Description
J14	3	CPU fan power and sensor. Pin 1 is +12 V. Pin 2 is sensor; low = fan on. Pine 3 is ground.

Caution: Fan sensor required

The fan *must* have a built-in sensor that drives a signal if the airflow stops. The sensor is connected to J14. The fan supplied with the Alpha PCI 64–275 includes an airflow sensor.

(continued on next page)

Table 2–3 (Cont.) Module Connector Descriptions (See Figure 2–3)

Connector	Pins	Description
		Enclosure Fan
J1	3	Enclosure fan connector. Pins 1 and 3 are ground. Pin 2 is +12 V.
		Power LED
J3 Pins 38, 40	2	Power LED connector. Pin 38 is +5 V with a built-in 150-ohm resistor. Pin 40 is ground.
		Disk Access LED
J3 Pins 29, 31	2	IDE disk access LED connector. Pin 29 is grounded on access. Pin 31 is +5 V with a built-in 150-ohm resistor.
		Key Lock
J3 Pins 32, 34	2	Key lock connector. Pin 32 is ground. Pin 34 is open (high) when unlocked.
		Board Reset
J3 (Pins 28, 30)	2	Board reset switch connector. 28 open or high to run, ground to 30 to reset.
		Speaker Connector
J3 (Pins 33, 35, 37, 39)	4	Connect speaker to 33 (signal) and 37 (ground).

3

Starting and Using the Alpha PCI 64–275

This chapter lists hardware, software, and accessories you must obtain to completely set up a functioning computer system. The chapter then describes how to configure the hardware and software. Finally, the chapter describes how to start and use the Alpha PCI 64–275.

3.1 Hardware Requirements

Before turning on the power to your Alpha PCI 64–275, you must provide the following components (if required by your applicattion) in addition to those supplied with your board. The components listed here round out the complement of parts needed to run the Microsoft Windows NT operating system on the Alpha PCI 64–275.

The required peripherals are available from Digital. See Appendix A for a list of part numbers.

- Four or eight, 72-pin, 36-bit, 5-V, DRAM SIMM memory modules (connectors J4 through J11). SIMMs must be installed in groups of four consisting of identical devices.

  To minimize the possibility of memory timing conflicts, Digital recommends the use of the same memory type. For best results, use a single vendor's part number for all modules.
- An industry-standard PC power supply, rated at a minimum of 275 W, that includes a 3.3-Vdc output.
- A PS/2 compatible 101-key keyboard.
- A PS/2 compatible mouse.
- A supported PCI or ISA bus graphics card, cables, and a compatible monitor.
- A supported PCI bus SCSI controller card and cables, if you plan to use one or more SCSI devices.
- An IDE or SCSI CD–ROM drive.

3.1 Hardware Requirements

- An IDE or SCSI hard drive.
- A 3.5-in diskette drive and cable.
- A 10-pin serial line cable.
- A terminal or a serial line connection to a host system with appropriate cables.

For more information about hardware requirements and for the location of board connectors and jumpers, see Chapter 2.

3.2 Software Requirements

3.2.1 Windows NT

Windows NT is distributed either on CDROM (recommended) or 3.5" diskettes. Your system must have either a CDROM drive or 3.5" diskette drive to install Windows NT. Refer to the *Alpha PCI 64–275 Microsoft Windows NT Installation Guide* for installation instructions.

3.3 Hardware Configuration

Once you have acquired the necessary hardware, it must be assembled into a system. This section lists the necessary steps. The system does not have to be assembled in the order presented.

Caution: Static-Sensitive Component

Digital strongly recommends the use of antistatic mats, ESD-approved workstations, and exercising other good ESD practices when handling the Alpha PCI 64–275 and any associated components.

1. Install either four or eight system memory DRAM SIMMs. Refer to Section 1.2.1 for configuration information and Table 2–3 for socket locations.
   a. **Observe antistatic precautions.** Handle SIMMs at the edges only to prevent damage.
   b. SIMMs must be installed in groups of four consisting of identical devices.
   c. Hold the SIMM at an angle with the notch facing the key in the socket.
   d. Firmly push the module into the connector and stand the module upright.

e. Make sure that the SIMM snaps into the metal locking clips on both ends.

2. Connect a power supply to the Alpha PCI 64–275 motherboard, as shown in Figure 3–1, with standard power to J29 and J31 and with +3.3Vdc power to J27 and J28. If you use Digital's recommended power supply, connect P8—J31, P9—J29, P11—J27, and P12—J28. J29 and J31 are mounted inline to appear as a single 12-pin connector on the board, but accept two 6-pin plugs.

Caution

The four power connectors are not keyed, so pay particular attention to Figure 3–1 when installing them.

3. If you are using an enclosure, mount the 3.5-in diskette drive, hard drive, and CD–ROM drive. Refer to the manufacturer's instructions for installing these devices.

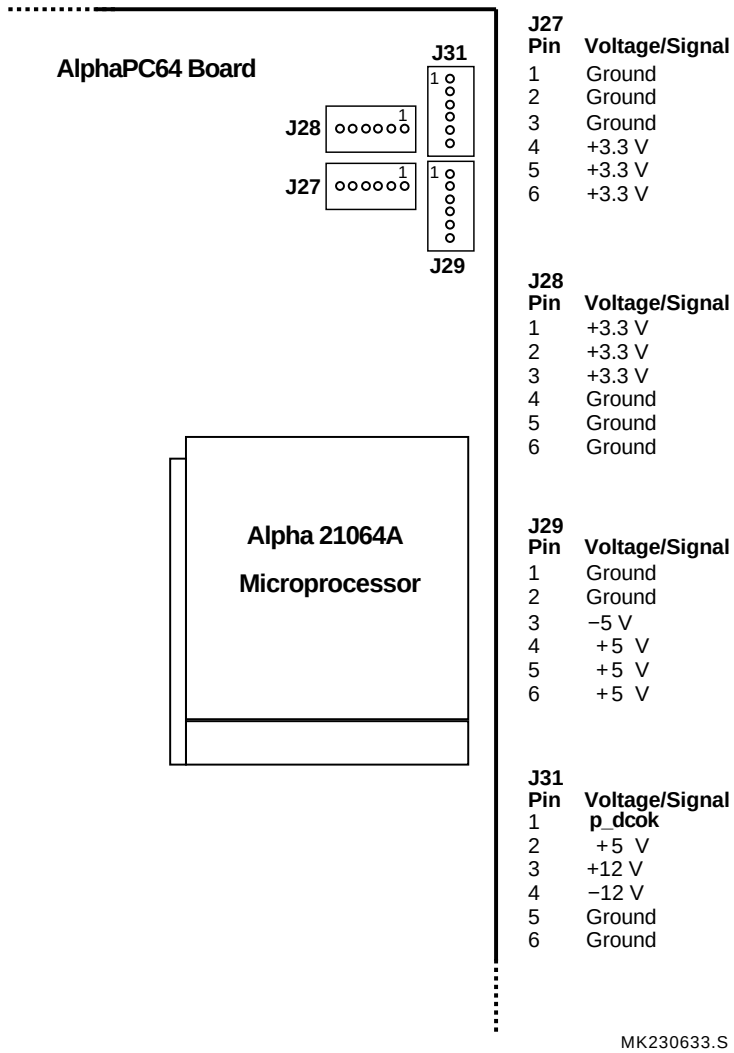
4. Connect the 3.5-in diskette drive. The 34-pin diskette drive cable goes from connector J24 on your Alpha PCI 64–275 to the diskette drive. The drive should be connected at the very end of the cable closest to the twist in the cable. Make sure to insert the connector in the proper orientation so that pin 1 on the cable matches pin 1 on the board header (as indicated on the board). Pin 1 is identified on the board with a **v** symbol. Attach a power connector to the drive.

5. If you will be using any SCSI devices, such as a SCSI CD-ROM drive or hard disk, install the SCSI controller in any free PCI or ISA slot. Then connect the drives, being sure *only* the last drive connected to the cable is terminated, or use a cable terminator if the last drive does not have SCSI bus termination capability. Follow the drive manufacturer's installation instructions to set each drive on the bus to a unique ID number and each drive except the last to non-terminated. The primary drive on the bus shold be a hard drive.

6. If you will be using one or more IDE CD-ROMs, hard drives, or other IDE devices, attach your IDE cable to connector J26 in the proper orientation. An IDE hard drive should be configured as the primary device on the IDE bus. Refer to the manufacturer's instructions for setting up the hard drive.

3.3 Hardware Configuration

Figure 3–1 Alpha PCI 64–275 Power Connectors



7. Install the graphics card into either a PCI or ISA connector, depending on the card you are using. Connect the graphics card to a compatible monitor, following the graphics card manufacturer's instructions.
8. Connect the keyboard cable to connector J33.

9. Connect the mouse cable to connector J34.
10. Connect a 9-pin serial port adapter cable to the COM1 connector at J32. Insert the connector in the proper orientation, so that pin 1 on the cable matches pin 1 on the board header (as indicated on the board). Pin 1 is identified on the board with a **v** symbol.
11. Connect your host system or terminal to the COM1 port by using an appropriate cable arrangement. Set the host system communications port or terminal to 9600 baud, 8 data bits, 1 stop bit, no parity.
12. Connect miscellaneous items such as, enclosure fans, reset button, speaker, power indicator, hard drive active indicator (if using an IDE drive), keyboard lock switch, and so forth. Refer to Figure 2–2 and Table 2–3 for the connection points.

3.4 Software Configuration

Refer to the software configuration compatibility sheet shipped with your motherboard for compatible firmware and operating system revisions.

3.4.1 Starting Windows NT ARC Firmware

Start the Windows NT ARC firmware using the following procedure:

1. Verify that the jumper from J16–2 to J16–3 is inserted, allowing the flash ROM to be written. See connector J16 in Table 2–3. If the Windows NT ARC firmware is unable to write to flash ROM, it prints the `device error` message and stops.
2. Verify that the jumper from J3–25/26 is installed (see SP7 on the board). The presence of the jumper at J3–25/26 forces the serial ROM firmware to load the alternate image selected by the value in the nonvolatile TOY RAM. The absence of this jumper overrides the value stored in the TOY RAM and causes the first image, the debug monitor, to be loaded.
3. Turn on the power to the Alpha PCI 64–275. After the power-up diagnostics are run, the ARC console boot menu appears on the graphics display. The diagnostics take several seconds to complete, so there will be some delay before the boot menu appears.

   If the ARC console boot menu does not appear, check the output of COM1 for error messages and review your hardware configuration.

You are ready for software installation. Refer to the *Alpha PCI 64–275 Microsoft Windows NT Installation Guide* for instructions.

3.4.2 Going to the Debug Monitor from Windows NT ARC Firmware

If a problem occurs requiring the use of the debug monitor, you can use one of the following methods to access the debug monitor from the Windows NT ARC firmware:

A. Use the ARC firmware menus to choose the debug monitor.

1. At the Boot menu, choose **Supplementary menu...**.
2. At the Supplementary menu, choose **Setup the system...**.
3. At the Setup the system menu, choose **Machine specific setup...**.
4. At the Machine specific setup menu, choose **Debug Monitor**.
5. Turn off the power to the Alpha PCI 64–275, and then turn the power back on.

Or:

B. Turn off the power to the Alpha PCI 64–275, remove the jumper from J3-25/26 (SP7 on the board), and then turn on the power to the Alpha PCI 64–275.

3.4.3 Returning to Windows NT ARC Firmware from the Debug Monitor

You can use one of the following methods to return to the Windows NT ARC firmware from the debug monitor:

A. If you used item A in Section 3.4.2 to enter the debug monitor, then use this procedure to return to Windows NT ARC firmware.

The firmware contained in the the serial ROM on your Alpha PCI 64–275 determines which firmware image is loaded from the flash ROM at power-up. The serial ROM firmware uses a value stored in the nonvolatile RAM of the real-time clock to determine which firmware image to load. At this point, you want the serial ROM to load the Windows NT ARC firmware.

1. Use the following debug monitor commands to select Windows NT ARC firmware, by writing the value 1 to the TOY RAM, and to verify the selection:[1]

[1] The Alpha PCI 64–275 uses the same firmware as the AlphaPC64, so the firmware prompts may appear as `AlphaPC64>`.

```
AlphaPC64>  bootopt nt

O/S type selected: "The Windows NT Operating System"
....Firmware type: "Windows NT Firmware"

AlphaPC64> bootopt

Predefined bootoptions are...
  "0" "Alpha Evaluation Board Debug Monitor" "DBM"
  "1" "The Windows NT Operating System" "NT"
  "2" "OpenVMS" "VMS"
  "3" "Digital UNIX" "UNIX"

O/S type selected: "The Windows NT Operating System"
....Firmware type: "Windows NT Firmware"

AlphaPC64>
```

(Support for other operating systems requires the purchase of the proper software license.)

2. Turn off the power to the Alpha PCI 64–275. Verify the presence of a jumper at J3-25/26 (see SP7 on the board).
3. Turn on the power to the Alpha PCI 64–275. After the power-up diagnostics run (10–15 seconds), the ARC console boot menu appears on the graphics display.

B. If you used item B in Section 3.4.2 to enter the debug monitor, then use this procedure to return to Windows NT ARC firmware:

1. Turn off the power to the Alpha PCI 64–275 and install the jumper at J3-25/26 (see SP7 on the board).
2. Turn on the power to the Alpha PCI 64–275. After the power-up diagnostics are run, the ARC console boot menu appears on the graphics display.

   If the ARC console boot menu does not appear, check the output of COM1 for error messages and review your hardware configuration.

4
Functional Elements

This chapter describes some of the functional elements of the Alpha PCI 64–275. Information, such as bus timing and protocol, found in other specifications, data sheets, and reference documentation is not duplicated. Appendix B provides a list of supporting documents and order numbers.

Note

For a detailed description of the Alpha 21064A, refer to the *Alpha 21064 and Alpha 21064A Microprocessors Hardware Reference Manual*.

For detailed descriptions of chipset logic, operations, and transactions, refer to the *DECchip 21071 and DECchip 21072 Core Logic Chipsets Data Sheet*.

For details of the PCI interface, refer to the *PCI System Design Guide* and the *PCI Local Bus Specification*, available from the PCI Special Interest Group (see Appendix B for address).

4.1 PCI Interrupts and Arbitration

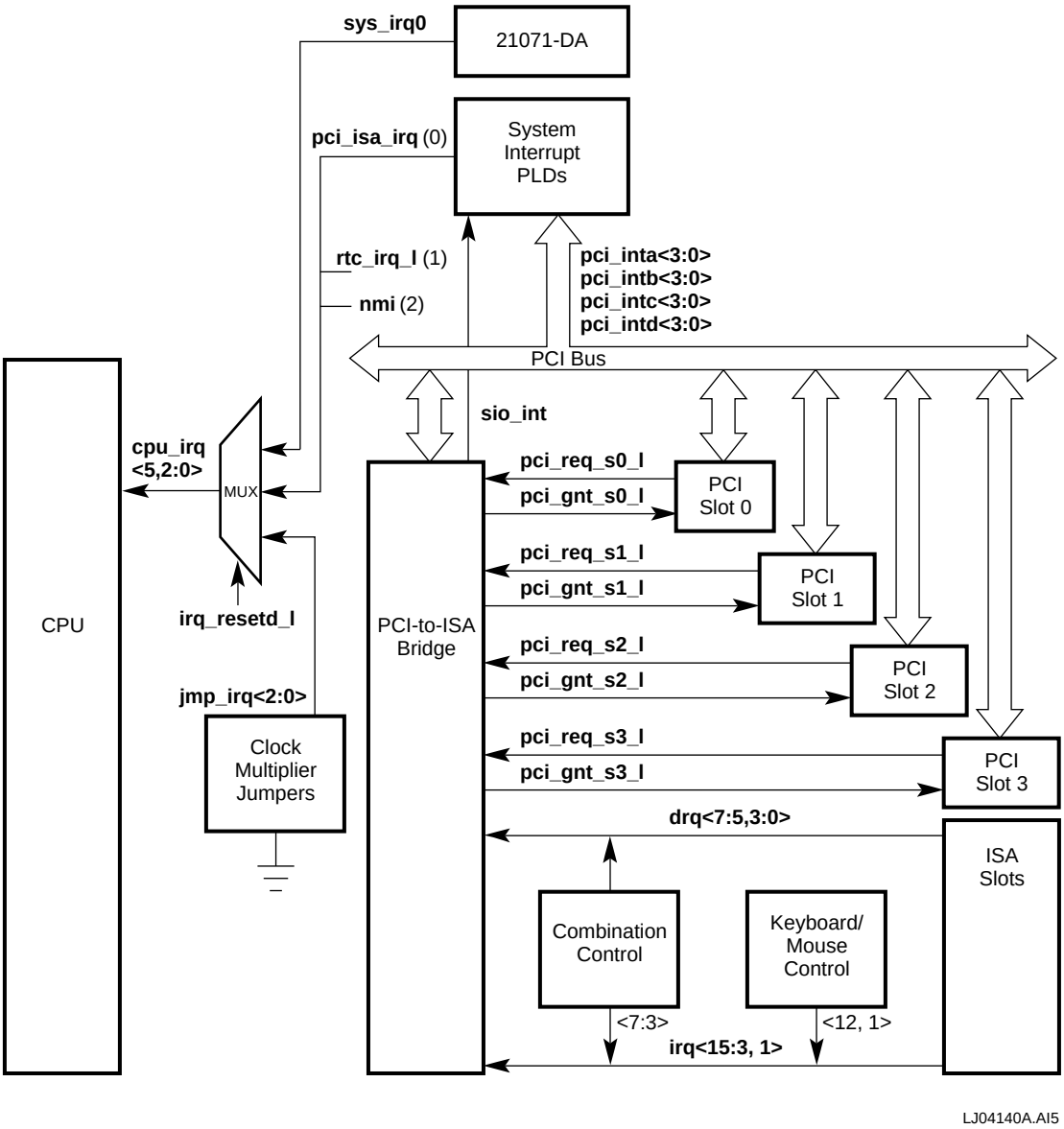
The following subsections describe the PCI interrupt and arbitration (arbiter) logic.

4.1.1 Board Interrupts

Figure 4–1 shows the Alpha PCI 64–275 interrupt logic. Interrupt logic is implemented in two programmable logic devices (PLDs), MACH210–20 and 22V10–25. The PLDs allow each PCI and PCI-to-ISA bridge chip interrupt to be individually masked. The PLDs also allow the current state of the interrupt lines to be read.

4.1 PCI Interrupts and Arbitration

Figure 4–1 Interrupt Control and PCI Arbitration



The Alpha PCI 64–275 interrupt controller has 17 interrupts: four from each of the four PCI slots (16) and one from the SIO bridge.

4.1 PCI Interrupts and Arbitration

All PCI interrupts are combined in the PLD and drive a single output signal, **pci_isa_irq**. This signal drives CPU input **cpu_irq0** through a multiplexer. There is also a memory controller error interrupt and an I/O controller error interrupt within the CPU.

Table 4–1 lists the CPU interrupt assignment during normal operation.

Table 4–1 CPU Interrupt Assignment

Interrupt Source	CPU Interrupt	Description
pci_isa_irq	**cpu_irq0**	Combined output of the interrupt PLD
rtc_irq_l	**cpu_irq1**	Real-time clock interrupt from DS1287
nmi	**cpu_irq2**	Nonmaskable interrupt from the SIO bridge
—	**cpu_irq3**, **cpu_irq4**	Not used; tied to ground
sys_irq0	**cpu_irq5**	Hardware interrupt from the PCI host bridge (21071-CA)

Three jumpers (J3-3, J3-5, and J3-7) connect to one side of the multiplexer. The jumper configuration sets the CPU clock multiplier value through the **cpu_irq***n* inputs during reset.

The ISA bus interrupt signals (**irq0** through **irq8** and **irq12** through **irq14**) are all nested through the SIO and then into the CPU. The interrupt assignment is configurable but is normally used as follows:

Interrupt Level	Interrupt Source
IRQ0	Interval timer
IRQ1	Keyboard
IRQ2	Chains interrupt from slave peripheral interrupt controller (PIC)
IRQ3	8-bit ISA from serial port COM2
IRQ4	8-bit ISA from serial port COM1
IRQ5	8-bit ISA from parallel port (or **irq7**)
IRQ6	8-bit ISA from diskette controller
IRQ7	8-bit ISA from parallel port (or **irq5**)
IRQ8	Reserved (real-time clock internal to the SIO)

4.1 PCI Interrupts and Arbitration

Interrupt Level	Interrupt Source
IRQ9, IRQ10, IRQ11	16-bit ISA
IRQ12	Mouse
IRQ13	16-bit ISA
IRQ14	IDE
IRQ15	16-bit ISA

The Alpha PCI 64–275 timer interrupt is generated by the real-time clock by means of **cpu_irq1**, rather than by the timer within the SIO, which would route the interrupt through the ISA bus interrupts.

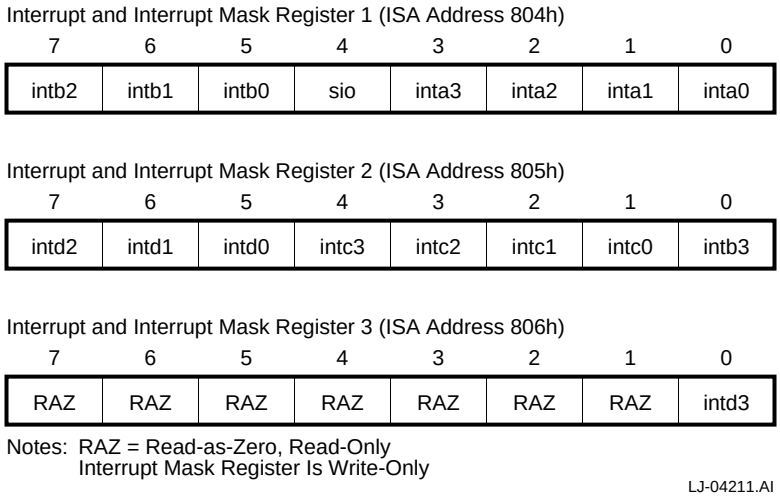
Interrupt PLDs Function

The MACH210 PLD acts as an 8-bit I/O slave on the ISA bus at addresses 804h, 805h, and 806h. This is accomplished by a decode of the three ISA address bits **sa<2:0>** and the three **ecas_addr<2:0>** bits.

Each interrupt can be individually masked by setting the appropriate bit in the mask register. An interrupt is disabled by writing a 1 to the desired position in the mask register. An interrupt is enabled by writing a 0. For example, bit <7> set in interrupt mask register 1 indicates that the INTB2 interrupt is disabled. There are three mask registers located at ISA addresses 804h, 805h, and 806h.

An I/O read transaction at ISA addresses 804h, 805h, and 806h returns the state of the 17 PCI interrupts rather than the state of the masked interrupts. On read transactions, a 1 means that the interrupt source shown in Figure 4–2 has asserted its interrupt. The mask register can be updated by writing addresses 804h, 805h, or 806h. The mask register is write-only.

Figure 4–2 Interrupt and Interrupt Mask Registers



4.1.2 PCI/ISA Arbitration

Arbitration logic is implemented in the Intel 82378ZB Saturn IO (SIO) chip. The arbitration scheme is flexible and software programmable. Refer to the Intel *82420/82430 PCIset ISA and EISA Bridges* document for more information about programmable arbitration.

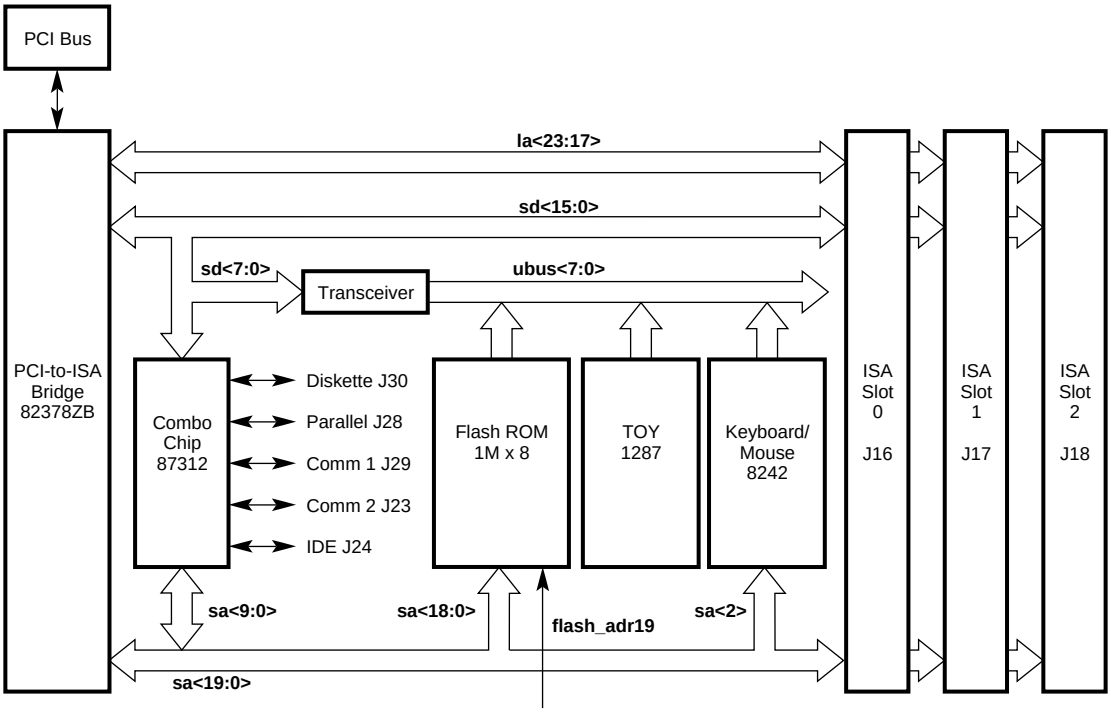
4.2 ISA Devices

Figure 4–3 shows the Alpha PCI 64–275 ISA bus implementation with peripheral devices and connectors. Also shown is the utility bus (Ubus) with system support devices.

4.3 dc Power Distribution

The Alpha PCI 64–275 derives its power from a user-supplied, industry-standard PC power supply. The power supply must provide ±12 Vdc, ±5 Vdc, and +3.3 Vdc. The dc power is supplied through power connectors J27, J28, J29, and J31 (see Figure 4–4). Power is distributed to the board logic through dedicated power planes within the 6-layer board structure.

Figure 4–3 ISA Devices



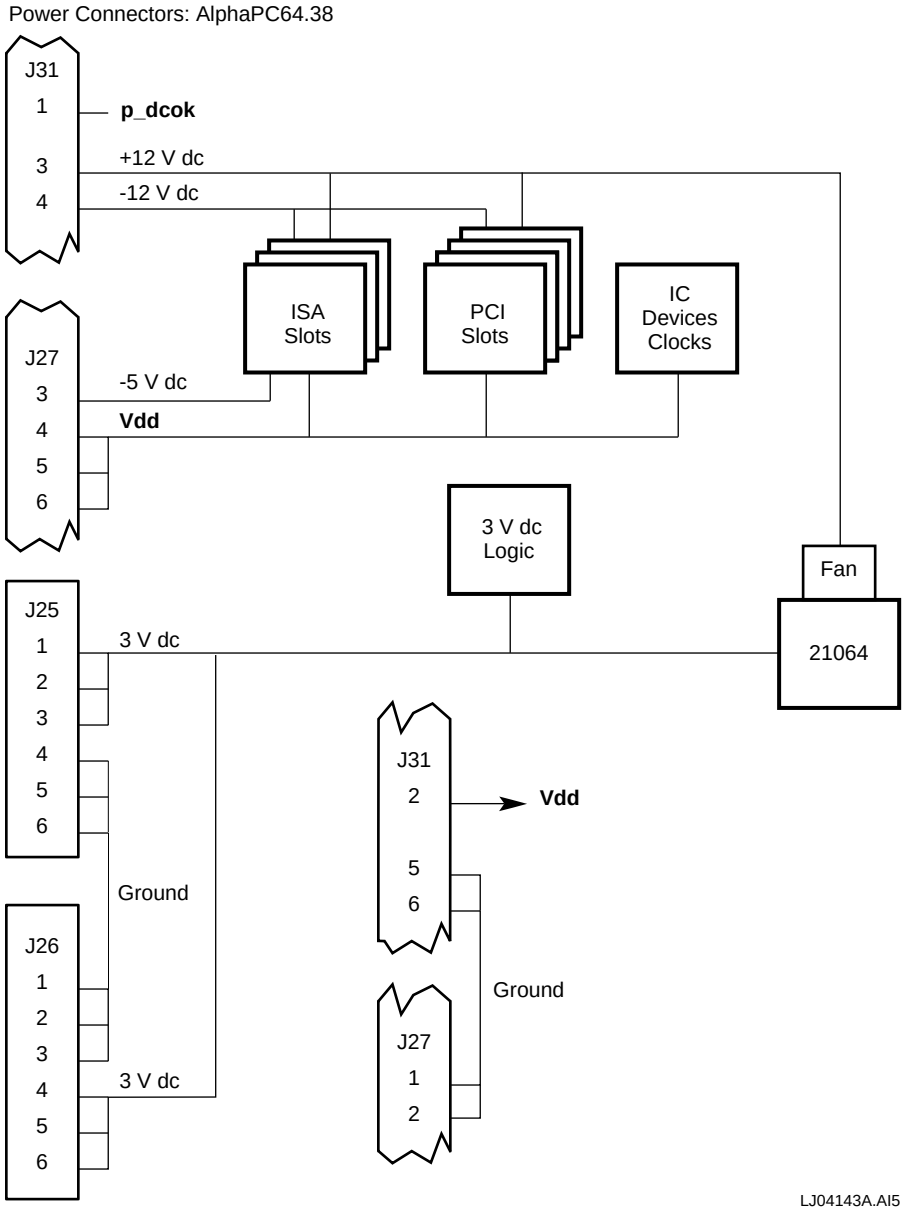
4.4 Flash ROM (System ROM)

The flash ROM, sometimes called the system ROM, is a 1MB, nonvolatile, writable ROM. After the SROM code initializes the Alpha PCI 64–275 board, flash ROM code prepares the board for booting. The flash ROM headers, structure, and access methods are described here.

4.4.1 Special Flash ROM Headers

The header informs the SROM where to load the image, and whether or not it has been compressed. The SROM allows the flash ROM to contain several different ROM images, each with its own header. The header is optional for flash ROM containing a single image. If the header does not exist, the 1MB flash ROM is loaded and executed at physical address zero. Figure 4–5 shows the header content.

Figure 4–4 dc Power Distribution



4.4 Flash ROM (System ROM)

Figure 4–5 Special Header Content

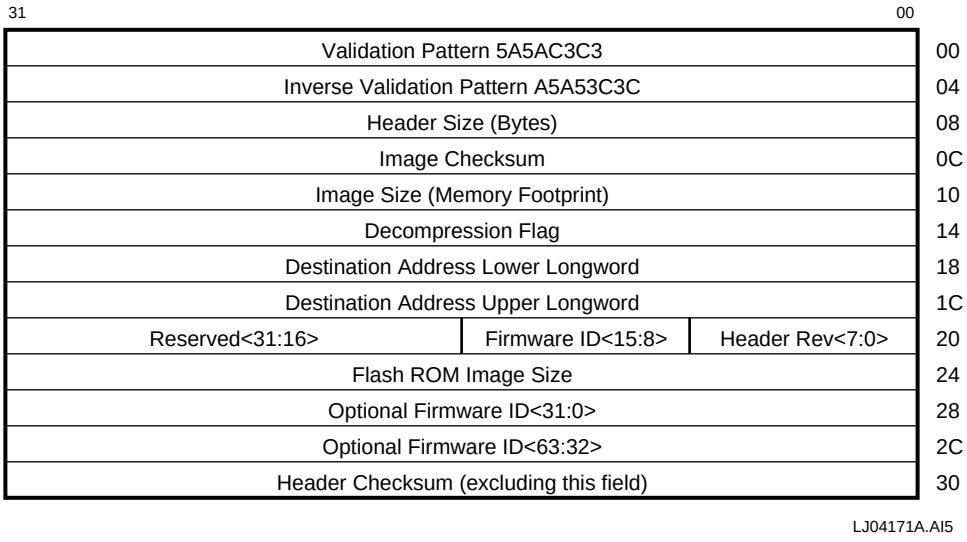


Table 4–2 describes each entry in the special header.

Table 4–2 Special Header Entry Descriptions

Entry	Description
Validation and inverse validation pattern	This quadword contains a special signature pattern used to validate that the special ROM header has been located. The pattern is 5A5AC3C3A5A53C3C.
Header size (bytes)	This longword contains the size of the header block, which varies among versions of the header specification. When the header is located, SROM code determines where the image begins based on the header size. Additional data added to the header will be ignored by older SROM code. A header size of 32 bytes implies version 0 of the header specifications.
Image checksum	This longword is used to verify the integrity of the ROM.
Image size (memory footprint)	The image size is used by the SROM code to determine how much of the flash ROM should be loaded.

(continued on next page)

Table 4–2 (Cont.) Special Header Entry Descriptions

Entry	Description
Decompression flag	The decompression flag informs the SROM code whether the the ROM image was compressed. The SROM code contains routines that execute the decompression algorithm. Other compression and decompression schemes, which work independently from this scheme, may be employed.
Destination address	This quadword contains the destination address for the image. The SROM code will load the image at this address and begin execution.
Firmware ID	The firmware ID is a byte that specifies the firmware type. This information facilitates image boot options necessary to boot different operating systems.

Firmware Name	Firmware Type	Firmware Description
Debug monitor	0	Alpha evaluation board debug monitor
Windows NT	1	Windows NT firmware
Alpha SRM	2	Alpha System Reference Manual console

Header revision	The revision of the header specifications used in this header. This is necessary to provide for changes to the header specification. Version 0 headers are identified by the size of the header (32 bytes).
Flash ROM image size	The flash ROM image size reflects the size of the image as it is contained in the flash ROM.
Optional firmware ID	This optional field can be used to provide additional firmware information such as firmware revision or a character descriptive string up to 8 characters.
Header checksum	The checksum of the header. This is used to validate the presence of a header beyond the validation provided by the validation pattern.

4.4.2 Flash ROM Structure

The Alpha PCI 64–275 loads and boots the first image (the debug monitor) during the power-up and initialization sequence if the BOOT_OPTION jumper J3-25/26 is not installed.

4.4 Flash ROM (System ROM)

If jumper J3-25/26 is installed, the Alpha PCI 64–275 reads the value at location 3F of the TOY NVRAM. The Alpha PCI 64–275 uses the value found there to determine which image will be selected (see Table 4–3). The selected image is loaded and executed.

Table 4–3 Higher 512KB Flash ROM Image Selection

TOY RAM Value[1]	Firmware ID[2]	Image Description
00	0	Evaluation board debug monitor firmware
01	1	Windows NT ARC firmware
02	2	Alpha SRM firmware (OpenVMS)[3]
03	2	Alpha SRM firmware (Digital UNIX)[3]
8*n*	Not applicable	SROM code will load the *n*th image from flash ROM. If *n*=0, the SROM code loads the entire flash ROM contents. If *n*=1, 2, ..., the SROM code loads the first image, second image, and so on.

[1]Operating system type. Found at TOY RAM address 3F.

[2]Found in image header.

[3]Support for this operating sytem requires the purchase of the proper software license.

If an image is specified and is not found, the Alpha PCI 64–275 loads the first image in the flash ROM with a valid header. If no valid header is found, the entire 1MB flash image is loaded at address 0000 0000.

The following sequence of steps describes how to change the value stored in TOY RAM location 3F by using either the basic debug monitor commands or the debug monitor `bootopt` command.

Changing TOY RAM Location 3F—Debug Monitor `bootopt` Command

Use the debug monitor `bootopt` command to change the value in location 3F. In the example shown here, the `bootopt` command is used to change the value in location 3F from 0 to 1:[1]

[1] The Alpha PCI 64–275 uses the same firmware as the AlphaPC64, so the firmware prompts may appear as `AlphaPC64>`.

```
AlphaPC64> bootopt ❶

Predefined bootoptions are...
  "0" "Alpha Evaluation Board Debug Monitor" "DBM"
  "1" "The Windows NT Operating System" "NT"
  "2" "OpenVMS" "VMS"
  "3" "Digital UNIX" "UNIX"

O/S type selected: "Alpha Evaluation Board Debug Monitor"
....Firmware type: "DBM Firmware"

AlphaPC64> bootopt nt ❷

O/S type selected: "The Windows NT Operating System"
....Firmware type: "Windows NT Firmware"

AlphaPC64> bootopt ❸

Predefined bootoptions are...
  "0" "Alpha Evaluation Board Debug Monitor" "DBM"
  "1" "The Windows NT Operating System" "NT"
  "2" "OpenVMS" "VMS"
  "3" "Digital UNIX" "UNIX"

O/S type selected: "The Windows NT Operating System"
....Firmware type: "Windows NT Firmware"

AlphaPC64>
```

Support for other operating systems requires the purchase of the proper software license.)

❶ Use the debug monitor `bootopt` command to see the image choices and note which image is selected.

❷ Use the debug monitor `bootopt nt` command to change the selected image from 0 to 1.

❸ Use the debug monitor `bootopt` command to verify that the selected image has changed from 0 to 1.

4.4.3 Flash ROM Access

The flash ROM can be viewed as two banks of 512KB each. At power-up, the lower 512KB bank is accessed using the address range 3 FFF8 0000 to 3 FFFF FFFF.

Setting address bit 19 will allow you to access the higher 512KB of flash ROM. Write a 1 to the register at address 800 to set address bit 19. Manually deposit a 1 to address 1 C001 0000 or enter the following command from the debug monitor:

```
 > wb 800 1
```

4.4 Flash ROM (System ROM)

The address range for the higher bank is 3 FFF8 0000 to 3 FFFF FFFF, the same as for the lower bank. Access is now to the higher bank and will continue until the Alpha PCI 64–275 is reset or a 0 is written to the register at address 800.

Note

The update-enable jumper must be installed from pin J16-2 to pin J16-3 to enable writing to the flash ROM. See connector J16 in Table 2–3.

5

Board Requirements and Parameters

This chapter describes the Alpha PCI 64–275 power and environmental requirements and physical board parameters.

5.1 Power Requirements

The Alpha PCI 64–275 derives its dc power from a user-supplied, industry-standard PC power supply. The board has a total power dissipation of 96.2 W, excluding PCI and ISA devices. Table 5–1 lists the power requirements of each dc supply voltage.

The power supply must supply signal **p_dcok** to the board reset logic.

Table 5–1 Power Supply dc Current Requirements for Motherboard (275 MHz) Without I/O

Voltage	Current
+5 Vdc	10 A (maximum)
+3.3 Vdc	10 A (maximum)
–5 Vdc	0 A
+12 Vdc	1 A (maximum)
–12 Vdc	0.1 A (maximum)

These values do not include power requirements for peripherals such as disks and tapes. You must increase the power supply capacity to meet the requirements of any peripherals you add.

Caution: Fan Sensor Required

The cooling fan supplied with the Alpha PCI 64–275 has a built-in sensor, connected to J14, that drives a signal low while the fan spins.

5.1 Power Requirements

If the fan stops, the loss of the sensor signal puts the Alpha PCI 64–275 into a low power standby mode. This protects the Alpha PCI 64–275 under fan-failure conditions.

5.2 Environmental Characteristics

The Alpha PCI 64–275 board environmental characteristics are:

- Operating temperature range of 10°C to 40°C (50°F to 104°F)
- Storage temperature range of –55°C to 125°C (–67°F to 257°F)

5.3 Physical Board Parameters

The Alpha PCI 64–275 board consists of a 6-layer printed-wiring board. The board is populated with integrated circuit packages together with supporting active and passive components. The Alpha PCI 64–275 is a baby-AT-size board with the following dimensions:

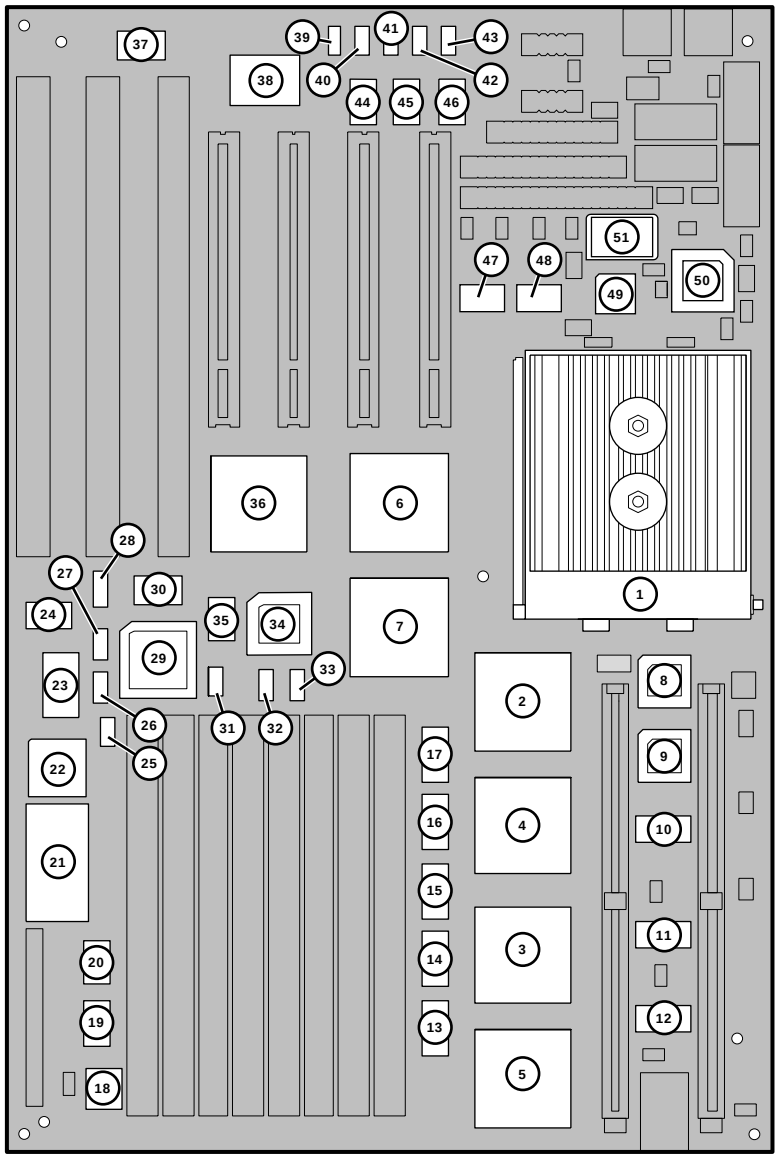
- Width: 22.1 cm (8.7 in)
- Length: 33.0 cm (13.0 in)

The board can be used in enclosures that have adequate clearance for the 21064A heat sink. All ISA and PCI expansion slots are usable in standard desktop or deskside enclosures.

Figure 5–1 shows the board and major component outlines and identifies key components. The components are described in Table 5–2. Refer to Chapter 2 for jumper and connector locations.

5.3 Physical Board Parameters

Figure 5–1 Board Component Layout



LJ-04460.AI5

5.3 Physical Board Parameters

Table 5–2 Board Component Descriptions

Number	Device	Component Description
1	U36	Alpha 21064A–275 microprocessor—431 PGA, 275 MHz
2	U24	DECchip 21071–BA0, 208-pin PQFP, ASIC
3	U8	DECchip 21071–BA1, 208-pin PQFP, ASIC
4	U13	DECchip 21071–BA2, 208-pin PQFP, ASIC
5	U2	DECchip 21071–BA3, 208-pin PQFP, ASIC
6	U35	DECchip 21071–DA, 208-pin PQFP, ASIC
7	U31	DECchip 21071–CA, 208-pin PQFP, ASIC
8, 9	U25, 17	PALCE16V8–5, 5-ns, 125-mA, 20-pin PLCC
10, 11, 12	U14, U9, U5	74FCT162244ETPV—48 SSOP
13, 14, 15, 16, 17	U4, U7, U11, U12, U16	74ABT162244—48-pin SSOP, 16-bit buffer/driver
18	U1	64K × 1 CMOS OTP serial ROM (initialization code)
19, 20	U3, U6	74F244 buffer/line driver
21	U10	Dallas Semiconductor DS1287—24-pin DIP, real-time clock and 50-byte RAM with crystal
22	U15	Intel N8242PC/PHOENIX/1991 mouse and keyboard controller, 44-pin PLCC
23	U19	E28F008SA–120, 40-pin TSOP, 1MX8 CMOS flash ROM, 120 ns
24	U28	74F245 transceiver
25	U18	74LS05 inverter gate
26	U20	74F14 trigger, SOIC
27	U26	74F02D NOR gate
28	U32	74F257 data selector/multiplexer
29	U27	PLD, MACH210–20, 20-ns, 180-mA, 44-pin PLCC, interrupt controller
30	U33	14.3-MHz crystal oscillator, PCI-to-ISA bridge (SIO) oscillator
31	U21	74F04 hex inverter

(continued on next page)

Table 5–2 (Cont.) Board Component Descriptions

Number	Device	Component Description
32, 33	U22, U23	74F08 AND gate
34	U30	PALCE22V10H–25JC, 28-pin PLCC, 25 ns
35	U29	74ACT244
36	U34	S82378ZB—208-pin PQFP, PCI-to-ISA bridge chip
37	U47	24-MHz crystal oscillator
38	U43	PC87312VF combination diskette controller chip—100-pin PQFP
39, 41, 43	U48, U50, U52	SN75189 receiver
40, 42	U49, U51	SN75188 driver
44, 45	U44, U45	74F245 transceiver
46	U46	74F244 buffer/line driver
47, 48	U37, U38	IDC FCT805CT—20-pin SOIC
49	U39	AMCC S4402 PLL—28-pin PLCC
50	U40	TriQuint TQ2061—28-pin PLCC, PLL 500-MHz to 700-MHz output
51	U41	27.50-MHz crystal oscillator

A

Components and Associated Literature

A.1 Components and Peripherals Available from Digital

The following table lists some of the components and peripherals available from Digital that you can use with the Alpha PCI 64–275.

Peripheral	Digital Indentifying Number
SCSI Adapters	KZPAA (PCI SCSI 2)
CD-ROM Drives	RRD43, RRD45
Disks	RZ28, RZ28B
Diskettes	RX23, RX33, RX26
Tapes	TZK11, TLZ07
Network Adapters	DE435, DE450 (PCI Tulip Ethernet) DE203, 205, 205 (ISA Ethernet) PBXNP (PCI Token Ring)
Keyboards	PCXAL-XX
Graphics Subsystems	PBXGA (ZLXp-E)
Mouse	PCXAS-AA

A.1 Components and Peripherals Available from Digital

Peripheral	Digital Indentifying Number	
Printers		
	LA75	LJ250
	LA75 TURBO	LJ252
	LA100	LN03
	LA120	LN03R
	LA210	DEClaser 1100/1500[1]
	LA324	DEClaser 2100/2150[1]
	LCG01	DEClaser 2200/2250[1]
	LF01R	DEClaser 3200/3250[1]
		DEClaser 5100[1]
Monitors	VRC16-HA, PCXBV-PC, VRC21-H4	
Modems	DF02, DF296, DF03 PCXDF[3]	

[1]Support for these printers is at DEC ANSI level 1.

[3]Modem support only - no FAX available.

A.2 Windows NT Qualified Peripherals List

To obtain the latest Microsoft Windows NT Hardware Compatability List, contact Microsoft's Customer Service representatives at 1-800-426-9400 or, access CompuServe Information Systems in Library 1 of the WINNT forum (GO WINNT) or Library 17 of the MSWIN32 forum (GO MSWIN32).

B

Additional Documentation

B.1 Ordering Third-Party Documentation

You can order the following documentation directly from the vendor:

Documentation	Order Number
82420/82430 PCIset ISA and EISA Bridges (includes 82378ZB SIO)	Intel No 290483
PC87311/PC87312 (Super I/O™ II/III) Floppy Disk Controller with Dual UARTs, Parallel Port, and IDE Interface	National Semiconductor No 11362
UPI-41AH/42AH Universal Peripheral Interface 8-Bit Slave Microcontroller	Intel No 210393
Peripheral Components	Intel No 296467
Flash Memory	Intel No 210830
PCI Local Bus Specification, Rev 2.0	Contact PCI Special Interest Group
PCI System Design Guide	Contact PCI Special Interest Group

B.1 Ordering Third-Party Documentation

Vendor Addresses

Intel Corporation
2200 Mission College Boulevard
PO Box 58119
Santa Clara CA 95052–8119
1–800–548–4725
http://www.intel.com

National Semiconductor
2900 Semiconductor Drive
PO Box 58090
Santa Clara CA 95052–8090
1–800–272–9959
http://www.national.com

PCI Special Interest Group
M/S HF3-15A
5200 NE Elam Young Parkway
Hillsboro OR 97124–6497
1–503–696–2000
www.teleport.com/~pc2/pcisigindex.html

C

Technical Support

C.1 Technical Support

If you need technical support with your Alpha PCI Motherboard, contact your local Digital representative. Please provide your local representative with the model number and if possible a brief description of the problem you are encountering.

Additional technical documentation is available from Digital on the major Digital semiconductor components used on your PCI Motherboard. A complete list of these documents can be obtained from your local representative.

And be sure to visit Digital Equipment's home page at UIC:

```
http://www.digital.com
```

Select the Semiconductor InfoCenter for pointers to relevant technical documentation.

Index

D

E

F

H

I

J

K

L

M

O

P

R

S

U

W