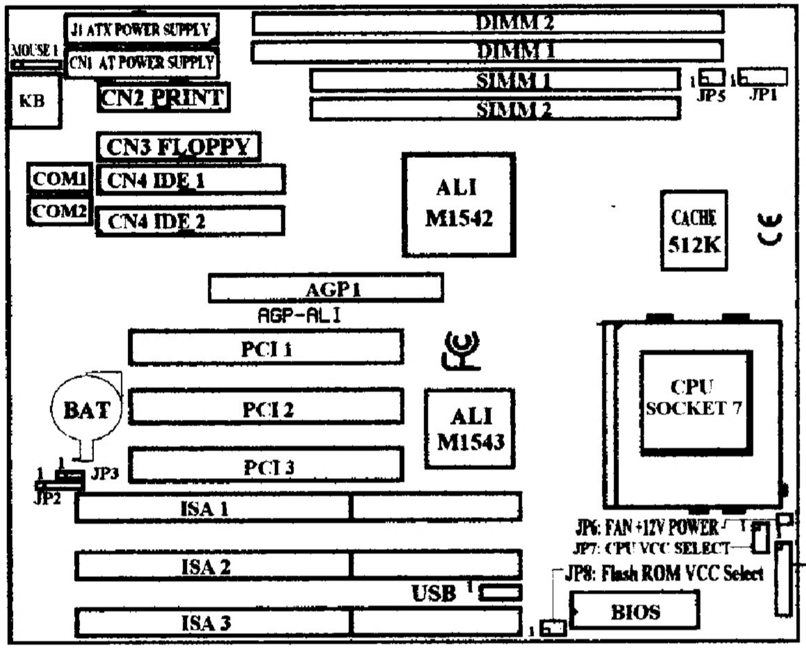
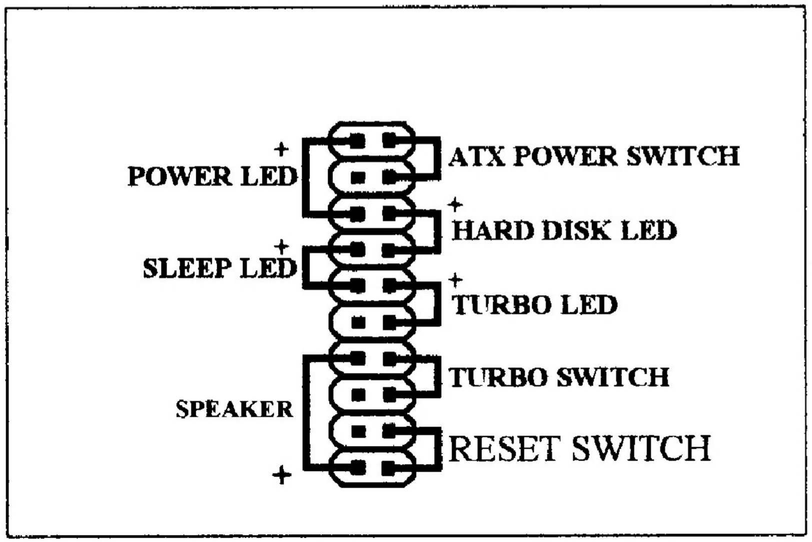




Посетите нашу страничку в интернете
http://pcvesti.null.ru
E-mail: pcvesti@null.ru

JP1: CPU CLK SELECT. Please refer section 2-4 relating

JP2: IR connect.

PINOUT	ASSIGNMENTS
1	VCC
2	FIRRX Signal
3	IRRX2 Signal
4	GND
5	IRTX2 Signal

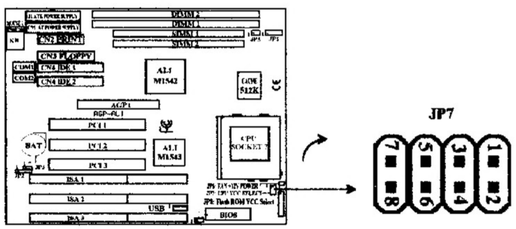
JP3: COMS CLEAR SETTING

JP3	Function
1-2	NORMAL
2-3	CMOS CLEAR

JP5: FOR 168 PIN SDRAM (Synchronous DRAM)
OR FPM/EDO DRAM Voltage SELECT

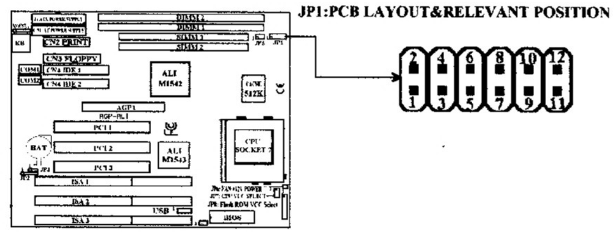
JP5	Function
1-2,1-2	+5V EDO/FPM
2-3,2-3	+3.3V SDRAM

2.3 Set CPU Voltage



CPU POWER MODE	JP7	EXAMPLE
ONLY 3.52V		AMD-K5 CYRIX M1
ONLY 3.3V		INTEL PENTIUM
DUAL 3.2V & 3.3V		AMD-K6 PR-233MHZ
DUAL 3.1V & 3.3V		FOR FUTURE CPU
DUAL 2.9V & 3.3V		IBM 6X86MX AMD-K6 & CYRIX M2
DUAL 2.8V & 3.3V		IBM 6X86L INTEL PENTIUM MMX
DUAL 2.5VV & 3.3V		FOR FUTURE CPU
DUAL 2.2V & 3.3V DUAL 2.2V & 3.45V		AMD-K6 266/300MHZ
DUAL 2.1V & 3.3V		FOR FUTURE CPU
DUAL 2.0V & 3.3V		FOR FUTURE CPU

2.6 CPU Multi Ratio & BUS CLK. AGP CLK & PCI CLK



CPU RATIO	JP1 (1-6 PIN)
1.5X	
2.0X	
2.5X	
3.0X	
3.5X	
4.0X	
4.5X	
5.0	
5.5X	

BUS CLK	AGP CLK	PCI CLK	JP1(7-12PIN)
60MHZ	60MHZ	30MHZ	
66MHZ	66MHZ	33MHZ	
75MHZ	60MHZ	30MHZ	
83MHZ	66MHZ	33MHZ	
95MHZ	63MHZ	32MHZ	
100MHZ	66MHZ	33MHZ	