

# Intel APAC Lakeport CRB Schematic

Version: 1.4

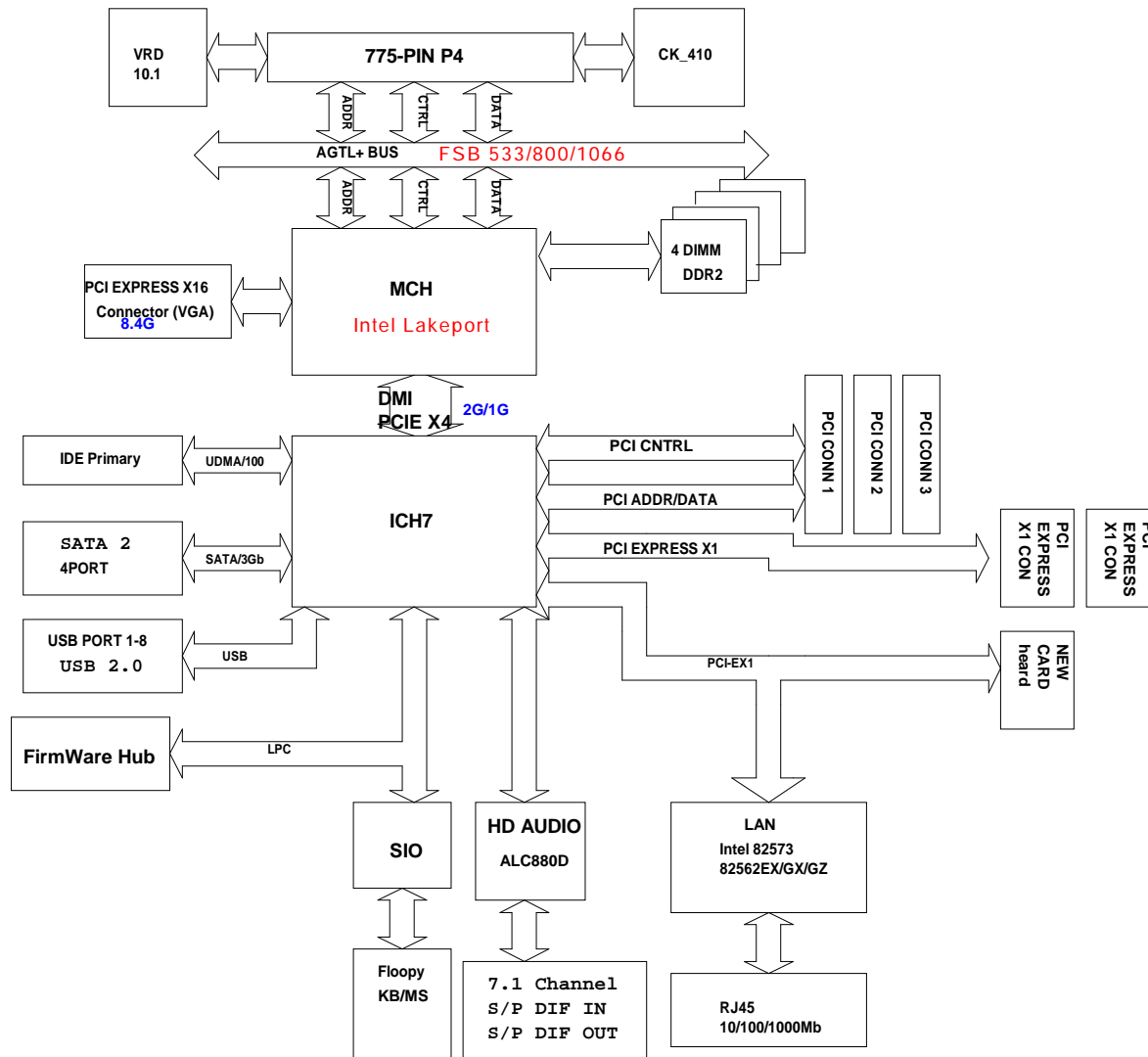
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# BLOCK DIAGRAM



## ICH7 GPIO SETTING

PINNAME	WELL	USAGE	I/O	NOTE
GPI0	MAIN	P_REQA	I	
GPI1	MAIN	P_REQ5	I	
GPI2	MAIN	P_REQE	I	
GPI3	MAIN	P_REQF	I	
GPI4	MAIN	P_REQQ	I	
GPI5	MAIN	P_REQH	I	
GPI6	MAIN	N/A	I	
GPI7	MAIN	N/A	I	
GPI8	RESUME	LPC_PME	I	
GPI9	RESUME	66DET	I	
GPI10	RESUME	FWH_WP	I	
GPI11	RESUME	SMB_ALERT	I	
GPI12	RESUME	ACZ_DET	I	
GPI13	RESUME	N/A	I	
GPI14	RESUME	N/A	I	
GPI15	RESUME	N/A	I	
GPO16	MAIN	N/A	O	
GPO17	MAIN	N/A	O	
GPO18	MAIN	N/A	O	
GPO19	MAIN	N/A	O	
GPO20	MAIN	N/A	O	
GPO21	MAIN	N/A	O	
GPO22	MAIN	N/A	OD	
GPO23	MAIN	LDQR1#	O	
GPO24	RESUME	LAN_DISABLE	I/O	
GPO25	RESUME	N/A	I/O	
GPO27	RESUME	N/A	I/O	
GPO28	RESUME	N/A	I/O	
GPO32	MAIN	N/A	I/O	
GPO33	MAIN	N/A	I/O	
GPO34	MAIN	N/A	I/O	

## PCI DEVICE SETTING

DEVICE	PCI1	PCI2	PCI3
IRQ	F	G	F
	G	F	E
	H	E	H
	E	H	G
ID	21	22	23
REQ/GNT	0	1	2

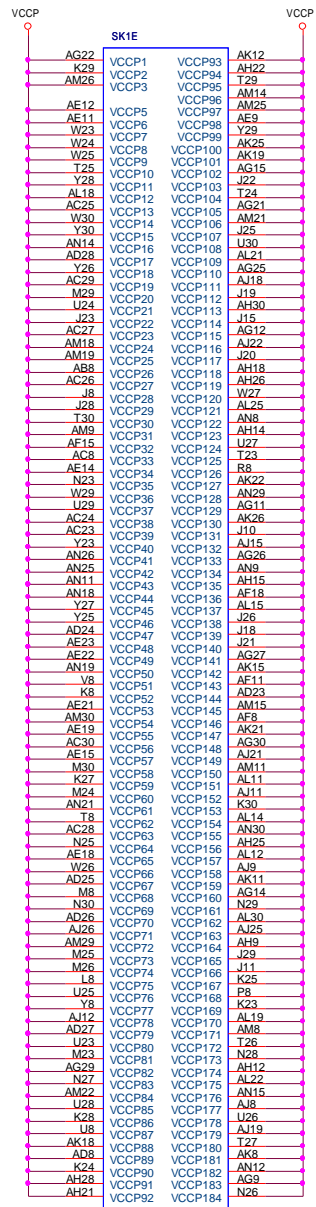
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Title: **BLOCK DIAGRAM & SETTING**

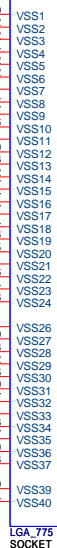
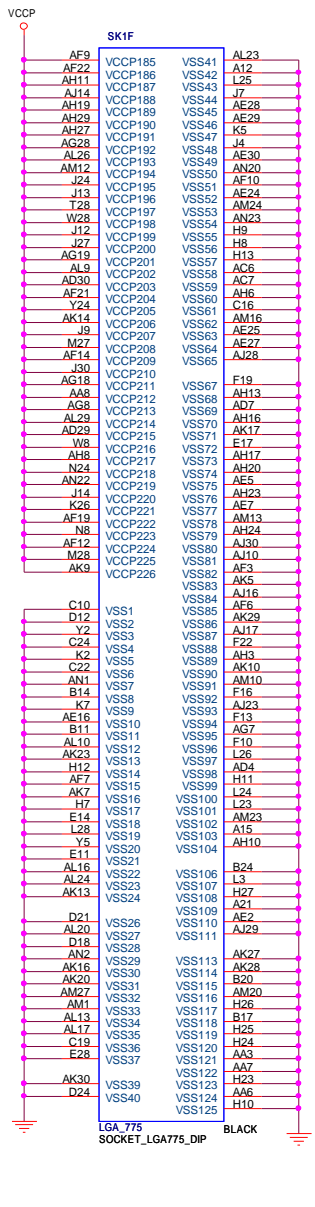
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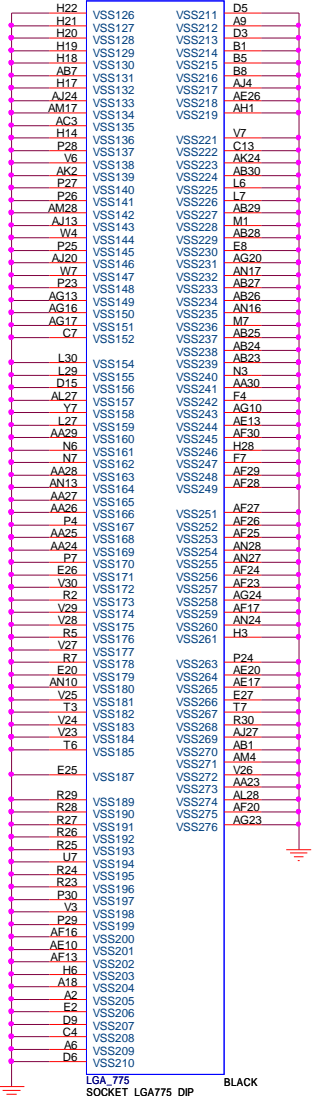




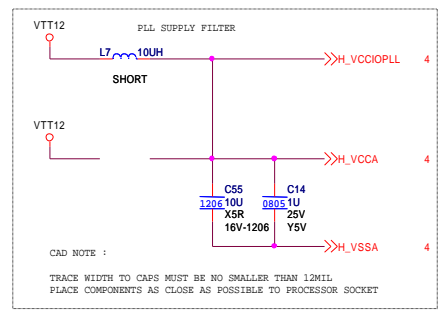
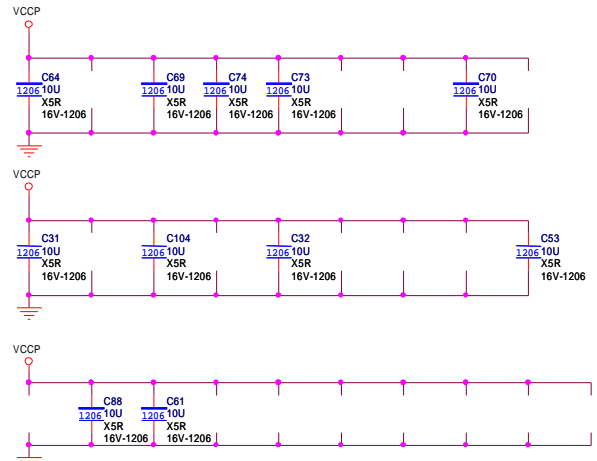
LGA 775 SOCKET\_LGA775\_DIP BLACK



LGA 775 SOCKET\_LGA775\_DIP BLACK



LGA 775 SOCKET\_LGA775\_DIP BLACK



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File: **P4-775 PART B**

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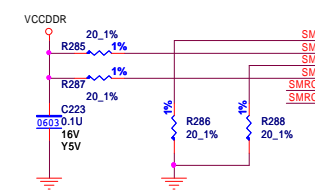
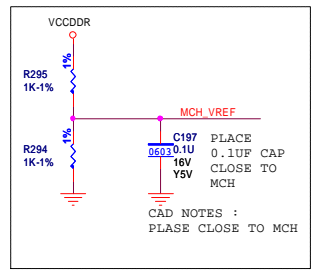


M_MAA_A0	BA31	SMA_A0	SDQS_A0	AU4	M_DOS_P_A0
M_MAA_A1	BB25	SMA_A1	SDQS_A0#	AR3	M_DOS_N_B0
M_MAA_A2	BA26	SMA_A2	SDM_A0	AR2	M_DQM_A0
M_MAA_A3	BA25	SMA_A3			
M_MAA_A4	AY25	SMA_A4	SDQ_A0	AR5	M_DATA_A0
M_MAA_A5	BA23	SMA_A5	SDQ_A1	AR4	M_DATA_A1
M_MAA_A6	AY24	SMA_A6	SDQ_A2	AR3	M_DATA_A2
M_MAA_A7	AY23	SMA_A7	SDQ_A3	AV2	M_DATA_A3
M_MAA_A8	BB23	SMA_A8	SDQ_A4	AP2	M_DATA_A4
M_MAA_A9	BA22	SMA_A9	SDQ_A5	AP2	M_DATA_A5
M_MAA_A10	AY33	SMA_A10	SDQ_A6	AU1	M_DATA_A6
M_MAA_A11	BB22	SMA_A11	SDQ_A7	AV4	M_DATA_A7
M_MAA_A12	AW21	SMA_A12			
M_MAA_A13	AY38	SMA_A13	SDQS_A1	BB3	M_DOS_P_A1
M_MAA_A14	BA21	SMA_A14	SDQS_A1#	BA4	M_DOS_N_A1
			SDM_A1	BA2	M_DQM_A1
9.11 M_WE_A	BB34C	SWE_A#			
9.11 M_CAS_A	AY35	SCAS_A#	SDQ_A8	AY2	M_DATA_A8
9.11 M_RAS_A	BB33C	SRAS_A#	SDQ_A9	AY3	M_DATA_A9
			SDQ_A10	BB5	M_DATA_A10
9.11 M_SBA_A0	BA33	SBS_A0	SDQ_A11	AY6	M_DATA_A11
9.11 M_SBA_A1	AW32	SBS_A1	SDQ_A12	AW2	M_DATA_A12
9.11 M_SBA_A2	BB21	SBS_A2	SDQ_A13	AW3	M_DATA_A13
			SDQ_A14	BA5	M_DATA_A14
9.11 M_SCS_A0	AW35C	SCS_A0#	SDQ_A15	BB4	M_DATA_A15
9.11 M_SCS_A1	BA35C	SCS_A1#			
9.11 M_SCS_A2	BA34C	RESERVED_11	SDQS_A2	BB9	M_DOS_P_A2
9.11 M_SCS_A3	BB38C	RESERVED_12	SDQS_A2#	BA9	M_DOS_N_A2
			SDM_A2	AY9	M_DQM_A2
9.11 M_SCKE_A0	BC20	SCKE_A0	SDQ_A16	AY7	M_DATA_A16
9.11 M_SCKE_A1	AY20	SCKE_A1	SDQ_A17	BC7	M_DATA_A17
9.11 M_SCKE_A2	AY21	RESERVED_9	SDQ_A18	AW11	M_DATA_A18
9.11 M_SCKE_A3	BA19	RESERVED_10	SDQ_A19	AY11	M_DATA_A19
9.11 M_SODT_A0	AY37	SODT_A0	SDQ_A20	BB6	M_DATA_A20
9.11 M_SODT_A1	BA38	SODT_A1	SDQ_A21	BA6	M_DATA_A21
9.11 M_SODT_A2	BB35	RESERVED_2	SDQ_A22	BA10	M_DATA_A22
9.11 M_SODT_A3	BA39	RESERVED_1	SDQ_A23	BB10	M_DATA_A23
9 CK_M_DDR_P_A0	AU31	SCLK_A0	SDQS_A3	AT20	M_DOS_P_A3
9 CK_M_DDR_N_A0	AR31C	SCLK_A0#	SDQS_A3#	AU18	M_DOS_N_A3
9 CK_M_DDR_P_A1	AP27	SCLK_A1	SDM_A3	AN18	M_DQM_A3
9 CK_M_DDR_N_A1	AN27C	SCLK_A1#			
9 CK_M_DDR_P_A2	AV33	SCLK_A2	SDQ_A24	AT18	M_DATA_A24
9 CK_M_DDR_N_A2	AW32C	SCLK_A2#	SDQ_A25	AR18	M_DATA_A25
CK_M_DDR_P_A3	AP29	RESERVED_3	SDQ_A26	AU21	M_DATA_A26
CK_M_DDR_N_A3	AM26	RESERVED_4	SDQ_A27	AT21	M_DATA_A27
CK_M_DDR_P_A4	AM27	RESERVED_5	SDQ_A28	AP17	M_DATA_A28
CK_M_DDR_N_A4	AT33	RESERVED_6	SDQ_A29	AN17	M_DATA_A29
CK_M_DDR_P_A5	AU33C	RESERVED_7	SDQ_A30	AP20	M_DATA_A30
CK_M_DDR_N_A5		RESERVED_8	SDQ_A31	AV20	M_DATA_A31
SDQS_A4			SDQS_A4	AR41	M_DOS_P_A4
SDQS_A4#			SDM_A4	AR40	M_DOS_N_A4
SDM_A4				AU43	M_DQM_A4
SDQ_A32			SDQ_A32	AV42	M_DATA_A32
SDQ_A33			SDQ_A33	AU40	M_DATA_A33
SDQ_A34			SDQ_A34	AP42	M_DATA_A34
SDQ_A35			SDQ_A35	AN39	M_DATA_A35
SDQ_A36			SDQ_A36	AV40	M_DATA_A36
SDQ_A37			SDQ_A37	AV41	M_DATA_A37
SDQ_A38			SDQ_A38	AR42	M_DATA_A38
SDQ_A39			SDQ_A39	AP41	M_DATA_A39
SDQS_A5			SDQS_A5	AL41	M_DOS_P_A5
SDQS_A5#			SDM_A5	AL40	M_DOS_N_A5
SDM_A5				AM43	M_DQM_A5
SDQ_A40			SDQ_A40	AN41	M_DATA_A40
SDQ_A41			SDQ_A41	AM39	M_DATA_A41
SDQ_A42			SDQ_A42	AK42	M_DATA_A42
SDQ_A43			SDQ_A43	AK41	M_DATA_A43
SDQ_A44			SDQ_A44	AN40	M_DATA_A44
SDQ_A45			SDQ_A45	AN42	M_DATA_A45
SDQ_A46			SDQ_A46	AL42	M_DATA_A46
SDQ_A47			SDQ_A47	AL39	M_DATA_A47
SDQS_A6			SDQS_A6	AG42	M_DOS_P_A6
SDQS_A6#			SDM_A6	AG41	M_DOS_N_A6
SDM_A6				AG40	M_DQM_A6
SDQ_A48			SDQ_A48	AJ40	M_DATA_A48
SDQ_A49			SDQ_A49	AH43	M_DATA_A49
SDQ_A50			SDQ_A50	AF39	M_DATA_A50
SDQ_A51			SDQ_A51	AE40	M_DATA_A51
SDQ_A52			SDQ_A52	AJ42	M_DATA_A52
SDQ_A53			SDQ_A53	AJ41	M_DATA_A53
SDQ_A54			SDQ_A54	AE41	M_DATA_A54
SDQ_A55			SDQ_A55	AF42	M_DATA_A55
SDQS_A7			SDQS_A7	AC42	M_DOS_P_A7
SDQS_A7#			SDM_A7	AC41	M_DOS_N_A7
SDM_A7				AC40	M_DQM_A7
SDQ_A56			SDQ_A56	AD40	M_DATA_A56
SDQ_A57			SDQ_A57	AD43	M_DATA_A57
SDQ_A58			SDQ_A58	AE41	M_DATA_A58
SDQ_A59			SDQ_A59	AA40	M_DATA_A59
SDQ_A60			SDQ_A60	AE42	M_DATA_A60
SDQ_A61			SDQ_A61	AE41	M_DATA_A61
SDQ_A62			SDQ_A62	AC39	M_DATA_A62
SDQ_A63			SDQ_A63	AB42	M_DATA_A63

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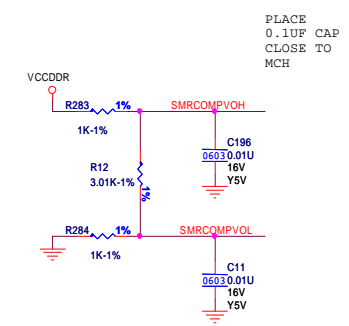
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946GZ(PL)



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**MCH LAKEPORT PART B**

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Channel A DIMM1

M_DQS_N_A0	6	DDR2-A1A	DQS0(B)	236	M_DATA_A63
M_DQS_P_A0	7		DQS0(B)	235	M_DATA_A62
M_DQS_N_A1	15		DQS1(B)	230	M_DATA_A61
M_DQS_P_A1	16		DQS1(B)	229	M_DATA_A60
M_DQS_N_A2	27		DQS2(B)	117	M_DATA_A59
M_DQS_P_A2	28		DQS2(B)	116	M_DATA_A58
M_DQS_N_A3	36		DQS3(B)	110	M_DATA_A57
M_DQS_P_A3	37		DQS3(B)	109	M_DATA_A56
M_DQS_N_A4	83		DQS4(B)	227	M_DATA_A55
M_DQS_P_A4	84		DQS4(B)	226	M_DATA_A54
M_DQS_N_A5	92		DQS5(B)	218	M_DATA_A53
M_DQS_P_A5	93		DQS5(B)	217	M_DATA_A52
M_DQS_N_A6	104		DQS6(B)	108	M_DATA_A51
M_DQS_P_A6	105		DQS6(B)	107	M_DATA_A50
M_DQS_N_A7	113		DQS7(B)	99	M_DATA_A49
M_DQS_P_A7	114		DQS7(B)	98	M_DATA_A48
			DQS8(B)	214	M_DATA_A47
			DQS8(B)	215	M_DATA_A46
M_DOM_A0	45		DQ46(B)	209	M_DATA_A45
			DQ46(B)	208	M_DATA_A44
M_DOM_A1	126		DQ44(B)	208	M_DATA_A44
			DQ44(B)	207	M_DATA_A43
M_DOM_A2	134		DQ43(B)	96	M_DATA_A42
			DQ43(B)	95	M_DATA_A41
M_DOM_A3	147		DQ42(B)	90	M_DATA_A40
			DQ42(B)	89	M_DATA_A39
M_DOM_A4	155		DQ41(B)	89	M_DATA_A39
			DQ41(B)	88	M_DATA_A38
M_DOM_A5	203		DQ39(B)	206	M_DATA_A38
			DQ39(B)	205	M_DATA_A37
M_DOM_A6	211		DQ38(B)	200	M_DATA_A37
			DQ38(B)	199	M_DATA_A36
M_DOM_A7	212		DQ37(B)	199	M_DATA_A36
			DQ37(B)	198	M_DATA_A35
			DQ36(B)	87	M_DATA_A35
			DQ35(B)	87	M_DATA_A34
			DQ35(B)	86	M_DATA_A34
			DQ34(B)	81	M_DATA_A33
			DQ34(B)	80	M_DATA_A32
			DQ33(B)	80	M_DATA_A32
			DQ32(B)	159	M_DATA_A31
			DQ31(B)	158	M_DATA_A30
			DQ30(B)	153	M_DATA_A29
			DQ29(B)	152	M_DATA_A28
			DQ28(B)	40	M_DATA_A27
			DQ27(B)	39	M_DATA_A26
			DQ26(B)	34	M_DATA_A25
			DQ25(B)	33	M_DATA_A24
			DQ24(B)	150	M_DATA_A23
			DQ23(B)	149	M_DATA_A22
			DQ22(B)	144	M_DATA_A21
			DQ21(B)	143	M_DATA_A20
			DQ20(B)	31	M_DATA_A19
			DQ19(B)	30	M_DATA_A18
			DQ18(B)	25	M_DATA_A17
			DQ17(B)	24	M_DATA_A16
			DQ16(B)	141	M_DATA_A15
			DQ15(B)	140	M_DATA_A14
			DQ14(B)	132	M_DATA_A13
			DQ13(B)	131	M_DATA_A12
			DQ12(B)	22	M_DATA_A11
			DQ11(B)	21	M_DATA_A10
			DQ10(B)	13	M_DATA_A9
			DQ9(B)	12	M_DATA_A8
			DQ8(B)	129	M_DATA_A7
			DQ7(B)	67	M_DATA_A6
			DQ6(B)	64	M_DATA_A5
			DQ5(B)	122	M_DATA_A4
			DQ4(B)	10	M_DATA_A3
			DQ3(B)	9	M_DATA_A2
			DQ2(B)	4	M_DATA_A1
			DQ1(B)	3	M_DATA_A0
			DQ0(B)	19	
			NC1(B)	102	
			NC2(B)	102	
			NC3(B)	68	
M_SBA_A2	54		A16(I)	238	

SK-D240P  
DDRII DIMM ADDRESS=000



7,11	M_SCKE_A0	52
7,11	M_SCKE_A1	171
7,11	M_SBA_A0	71
7,11	M_SBA_A1	190
7,11	M_WE_A	18
7,11	M_RAS_A	192
7,11	M_CAS_A	74
7,11	M_SCS_A0	193
7,11	M_SCS_A1	76
7,11	M_SODT_A0	195
7,11	M_SODT_A1	77
7	CK_M_DDR_P_A1	137
7	CK_M_DDR_N_A1	138
7	CK_M_DDR_P_A0	185
7	CK_M_DDR_N_A0	186
7	CK_M_DDR_P_A2	220
7	CK_M_DDR_N_A2	221

DDRII DIMM

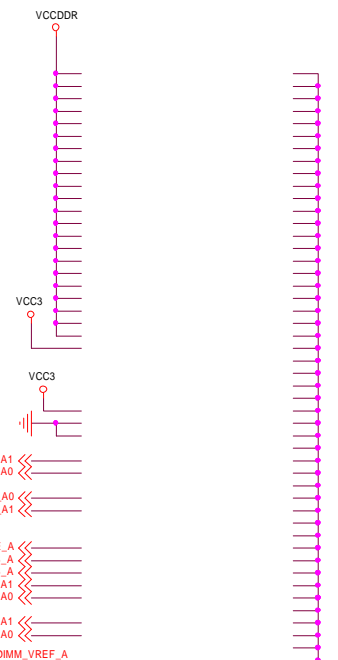
Channel A DIMM2

M_DQS_N_A0	6	M_DATA_A63
M_DQS_P_A0	7	M_DATA_A62
M_DQS_N_A1	15	M_DATA_A61
M_DQS_P_A1	16	M_DATA_A60
M_DQS_N_A2	27	M_DATA_A59
M_DQS_P_A2	28	M_DATA_A58
M_DQS_N_A3	36	M_DATA_A57
M_DQS_P_A3	37	M_DATA_A56
M_DQS_N_A4	83	M_DATA_A55
M_DQS_P_A4	84	M_DATA_A54
M_DQS_N_A5	92	M_DATA_A53
M_DQS_P_A5	93	M_DATA_A52
M_DQS_N_A6	104	M_DATA_A51
M_DQS_P_A6	105	M_DATA_A50
M_DQS_N_A7	113	M_DATA_A49
M_DQS_P_A7	114	M_DATA_A48
		M_DATA_A47
		M_DATA_A46
		M_DATA_A45
		M_DATA_A44
		M_DATA_A43
		M_DATA_A42
		M_DATA_A41
		M_DATA_A40
		M_DATA_A39
		M_DATA_A38
		M_DATA_A37
		M_DATA_A36
		M_DATA_A35
		M_DATA_A34
		M_DATA_A33
		M_DATA_A32
		M_DATA_A31
		M_DATA_A30
		M_DATA_A29
		M_DATA_A28
		M_DATA_A27
		M_DATA_A26
		M_DATA_A25
		M_DATA_A24
		M_DATA_A23
		M_DATA_A22
		M_DATA_A21
		M_DATA_A20
		M_DATA_A19
		M_DATA_A18
		M_DATA_A17
		M_DATA_A16
		M_DATA_A15
		M_DATA_A14
		M_DATA_A13
		M_DATA_A12
		M_DATA_A11
		M_DATA_A10
		M_DATA_A9
		M_DATA_A8
		M_DATA_A7
		M_DATA_A6
		M_DATA_A5
		M_DATA_A4
		M_DATA_A3
		M_DATA_A2
		M_DATA_A1
		M_DATA_A0
M_SBA_A2		

ADDRESS=001

M_MAA_A[0..14]	<<M_MAA_A[0..14]	7,11
M_DQS_P_A[0..7]	<<M_DQS_P_A[0..7]	7
M_DQS_N_A[0..7]	<<M_DQS_N_A[0..7]	7
M_DOM_A[0..7]	<<M_DOM_A[0..7]	7
M_DATA_A[0..63]	<<M_DATA_A[0..63]	7

M_SBA_A2	>>M_SBA_A2	7,11
SMBDATA	>>SMBDATA	3,10,12,15,17,18,19,23
SMBCLK	>>SMBCLK	3,10,12,15,17,18,19,23



7,11	M_SCKE_A1	
7,11	M_SCKE_A0	
7,11	M_SBA_A0	
7,11	M_SBA_A1	
7,11	M_WE_A	
7,11	M_RAS_A	
7,11	M_CAS_A	
7,11	M_SCS_A1	
7,11	M_SCS_A0	
7,11	M_SODT_A1	
7,11	M_SODT_A0	
7	CK_M_DDR_P_A1	
7	CK_M_DDR_N_A1	
7	CK_M_DDR_P_A0	
7	CK_M_DDR_N_A0	
7	CK_M_DDR_P_A2	
7	CK_M_DDR_N_A2	

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Title: **DDR II CHANNEL A**

Size: Custom Document Number: Lakeport CRB

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Rev 1.4

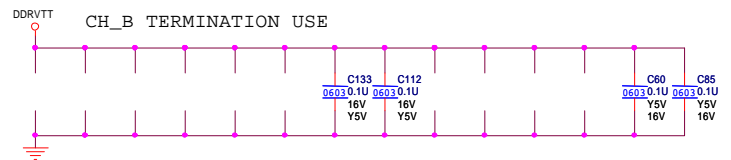
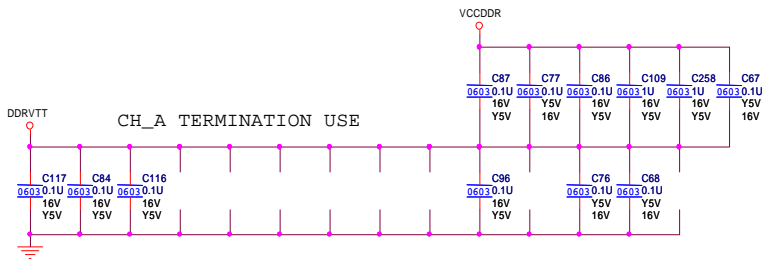
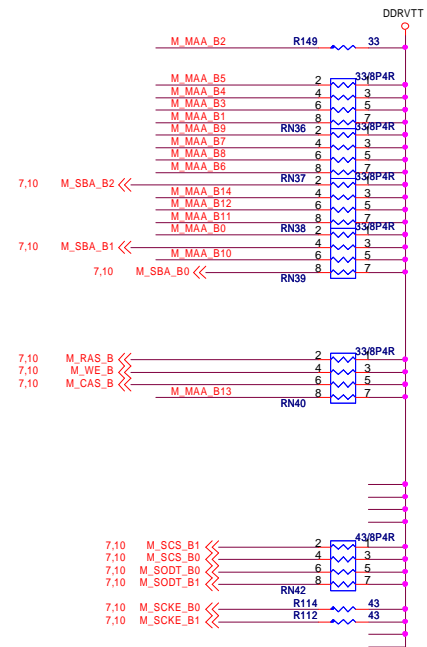
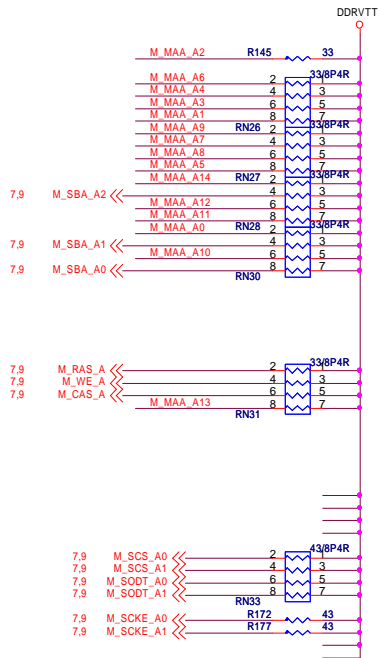
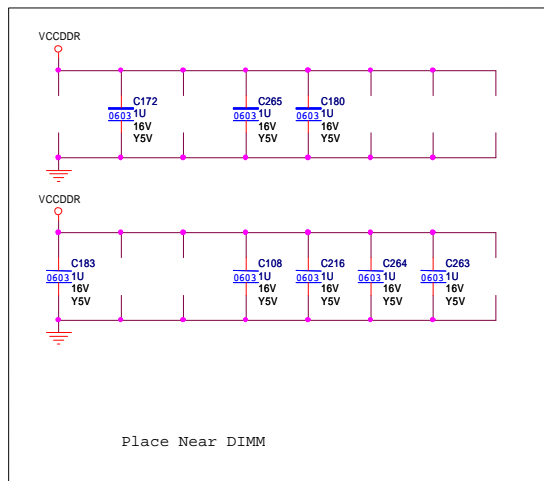
Channel B DIMM1

Channel B DIMM2

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M_DQS_N_B1	15	DDRS1-(B)	230	M_DATA_B61
M_DQS_P_B1	16	DDRS1+(B)	229	M_DATA_B60
M_DQS_N_B2	27	DDRS2-(B)	117	M_DATA_B59
M_DQS_P_B2	28	DDRS2+(B)	116	M_DATA_B58
M_DQS_N_B3	36	DDRS3-(B)	111	M_DATA_B57
M_DQS_P_B3	37	DDRS3+(B)	110	M_DATA_B56
M_DQS_N_B4	83	DDRS3-(B)	227	M_DATA_B55
M_DQS_P_B4	84	DDRS4-(B)	226	M_DATA_B54
M_DQS_N_B5	92	DDRS4+(B)	218	M_DATA_B53
M_DQS_P_B5	93	DDRS5-(B)	217	M_DATA_B52
M_DQS_N_B6	104	DDRS5+(B)	108	M_DATA_B51
M_DQS_P_B6	105	DDRS6-(B)	107	M_DATA_B50
M_DQS_N_B7	113	DDRS6+(B)	99	M_DATA_B49
M_DQS_P_B7	114	DDRS7-(B)	98	M_DATA_B48
		DDRS7+(B)	215	M_DATA_B47
		DDRS8-(B)	214	M_DATA_B46
		DDRS8+(B)	209	M_DATA_B45
M_DQM_B0	125	DDRS9-(B)	208	M_DATA_B44
M_DQM_B1	134	DDRS10-(B)	95	M_DATA_B42
M_DQM_B2	135	DDRS10+(B)	90	M_DATA_B41
M_DQM_B3	147	DDRS11-(B)	89	M_DATA_B40
M_DQM_B4	155	DDRS12-(B)	206	M_DATA_B39
M_DQM_B5	156	DDRS12+(B)	205	M_DATA_B37
M_DQM_B6	203	DDRS13-(B)	199	M_DATA_B36
M_DQM_B7	211	DDRS13+(B)	87	M_DATA_B35
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		DDRS22+(B)	30	M_DATA_B18
		DDRS23-(B)	25	M_DATA_B17
		DDRS23+(B)	24	M_DATA_B16
		DDRS24-(B)	141	M_DATA_B15
		DDRS24+(B)	140	M_DATA_B14
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		DDRS26+(B)	21	M_DATA_B10
		DDRS27-(B)	13	M_DATA_B9
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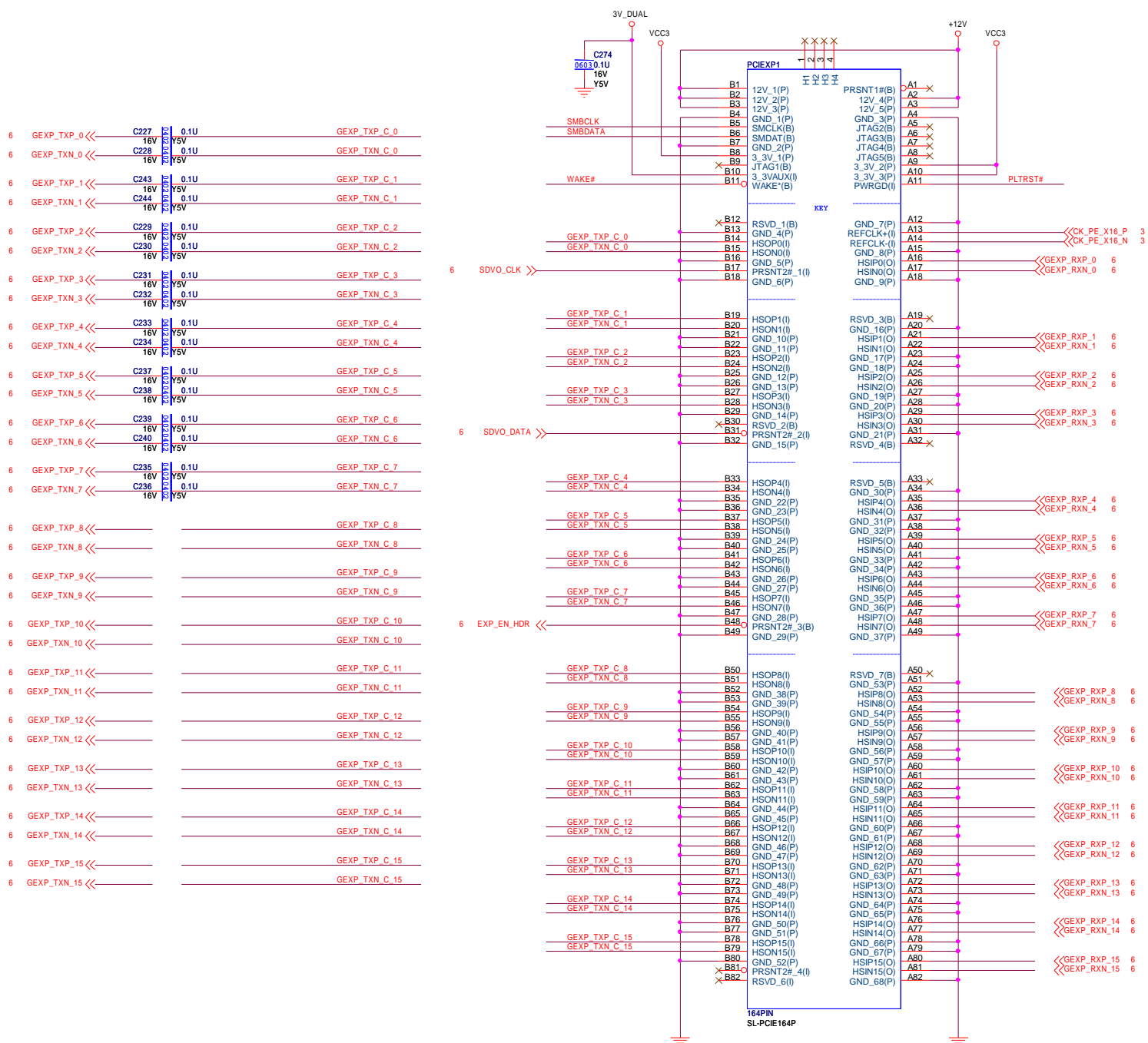
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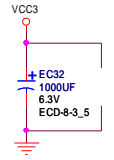
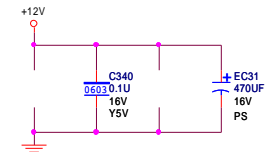
place at left and right ends of VTT island

Channel B Address / Control stitching Caps

place at left and right ends of VTT island



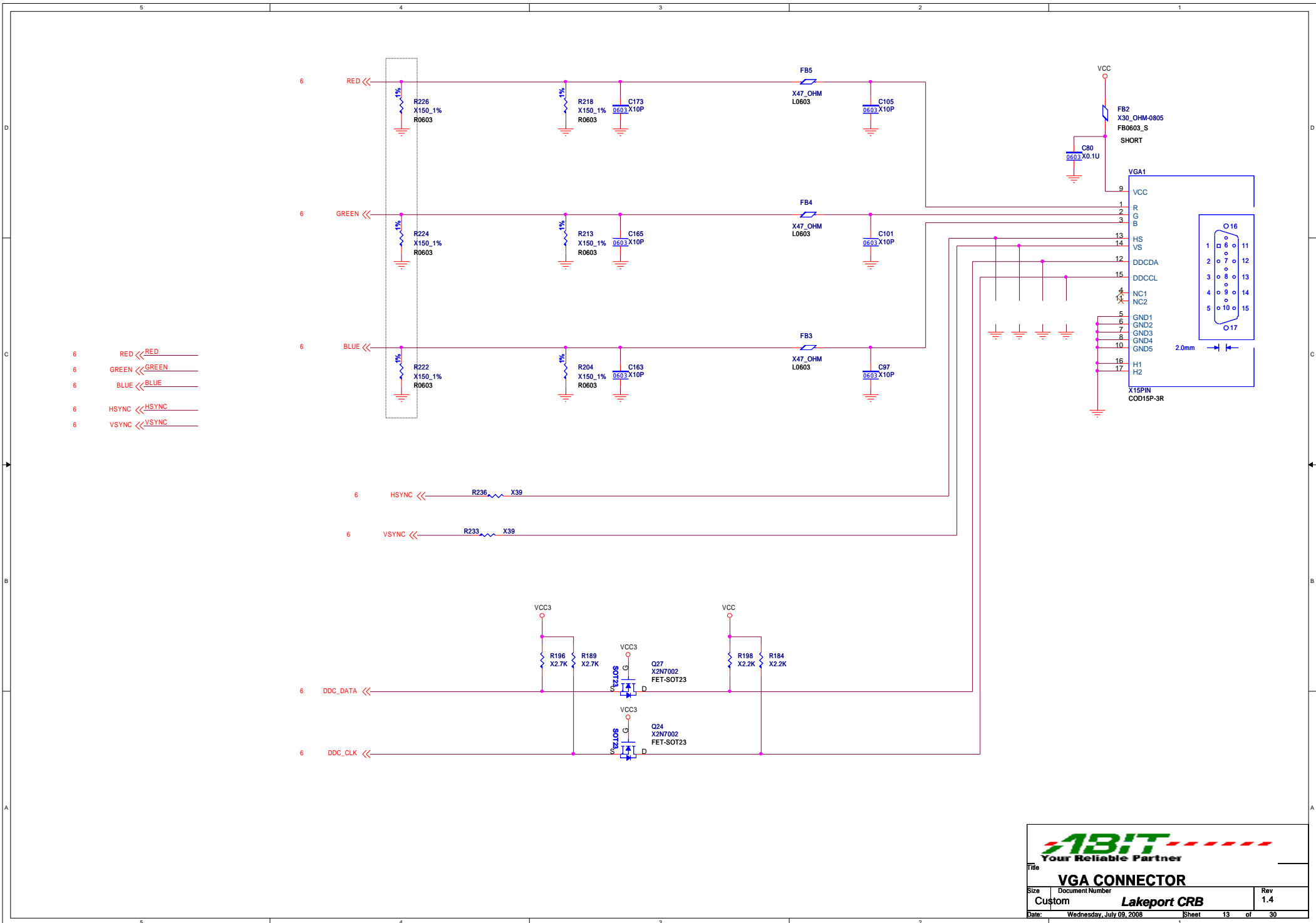
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SMBCLK	<<SMBCLK	3,9,10,15,17,18,19,23



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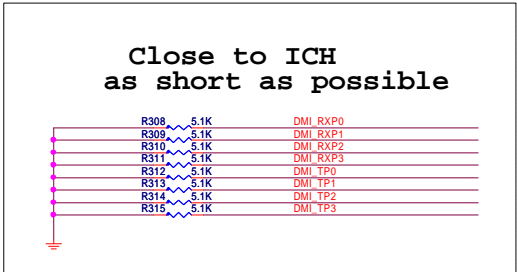
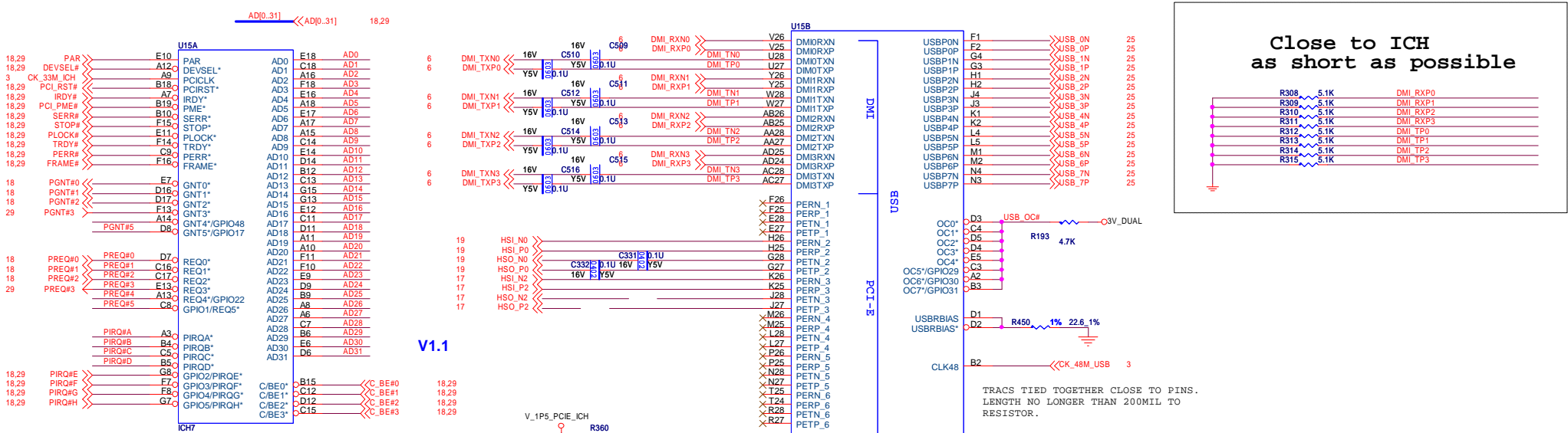
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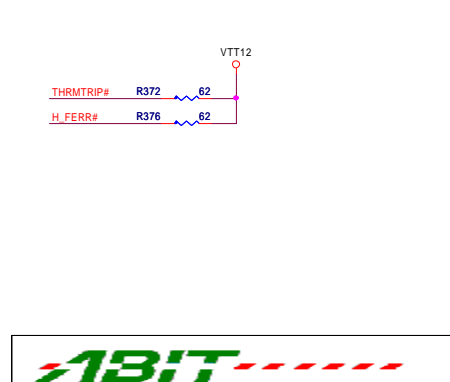
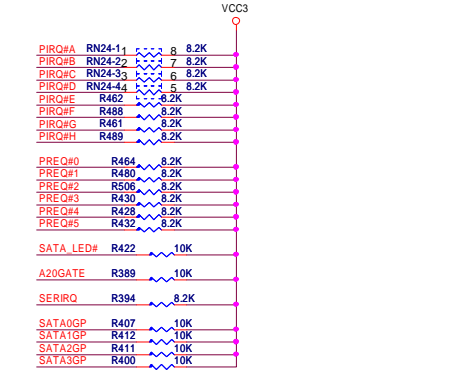
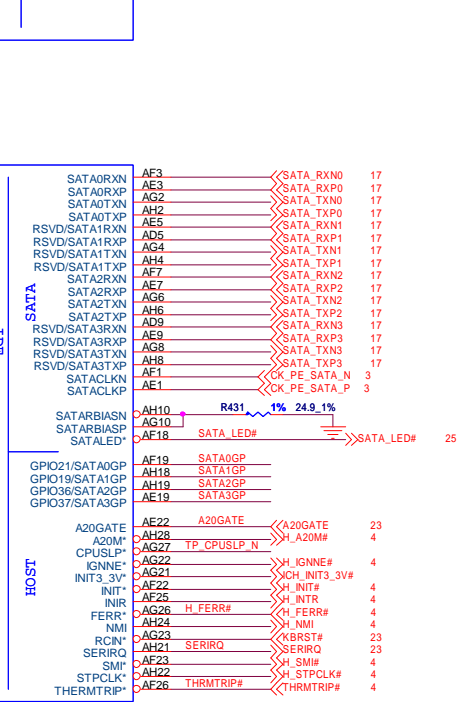
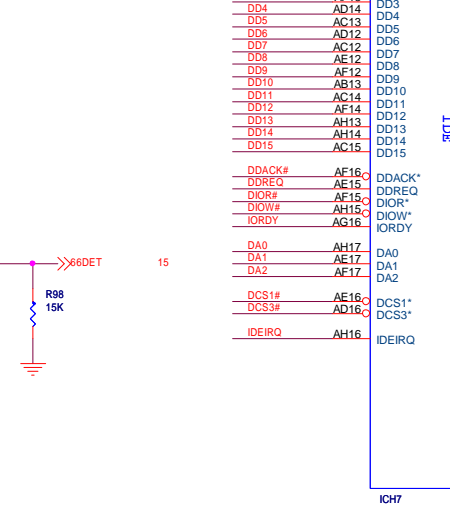
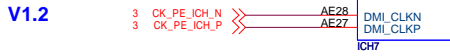
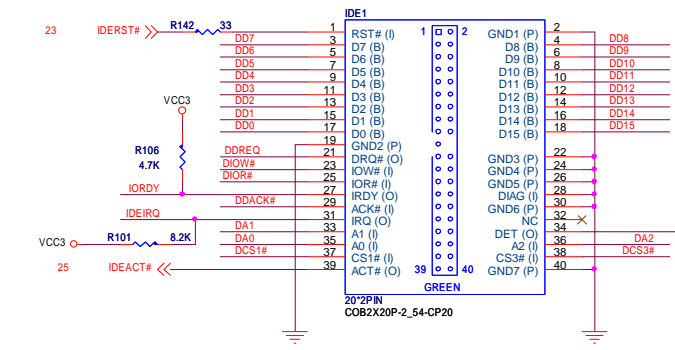
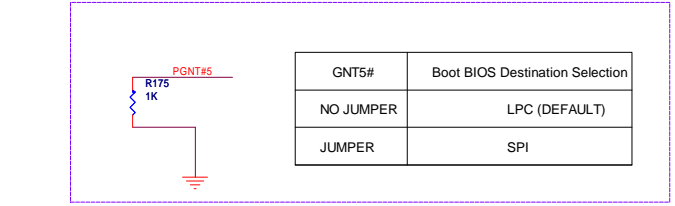


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<b>Title</b> VGA CONNECTOR		
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		JUMPER	SPI

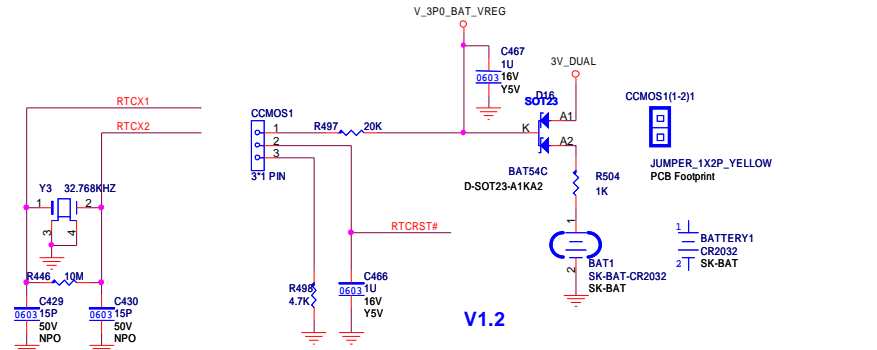
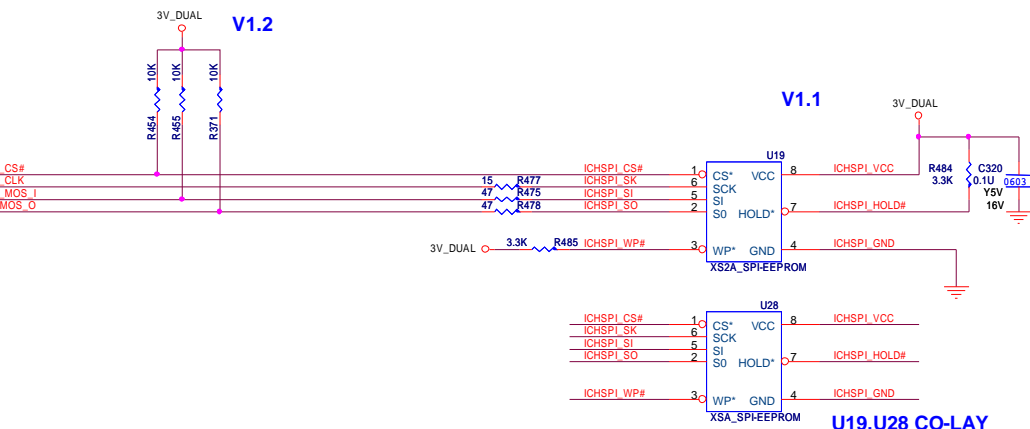
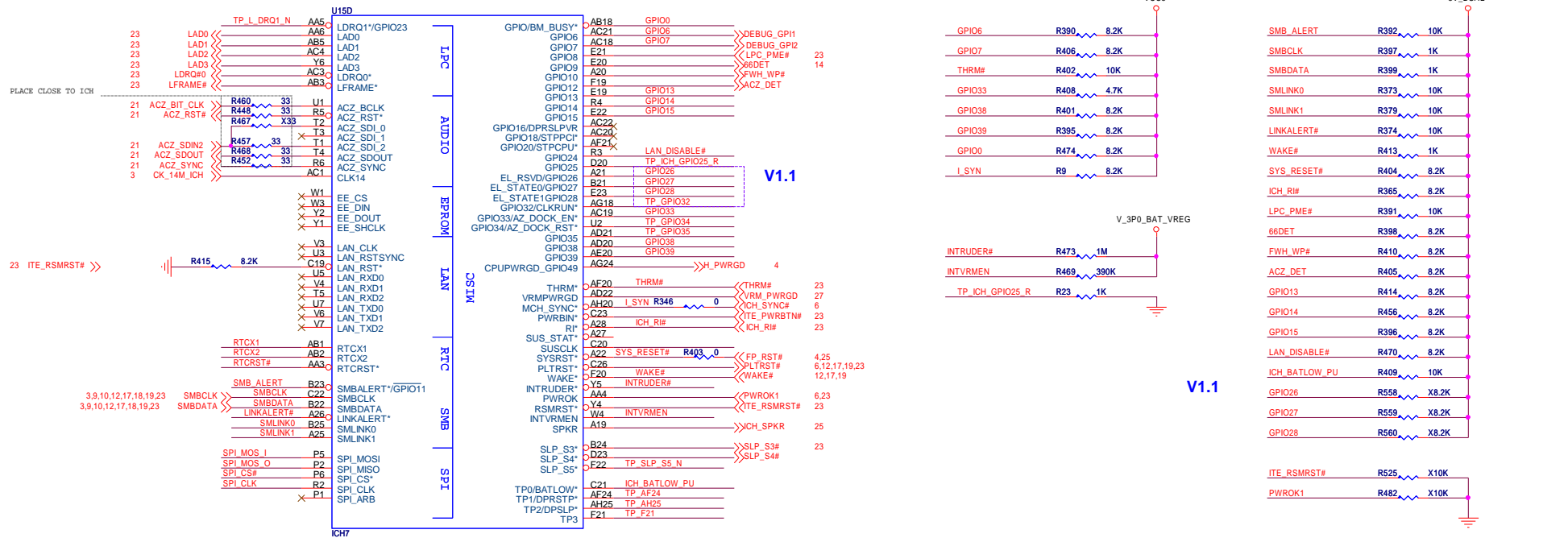


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Title: **ICH7 PART A**

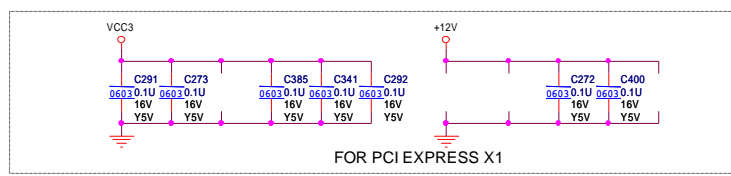
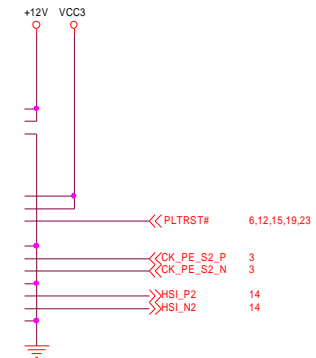
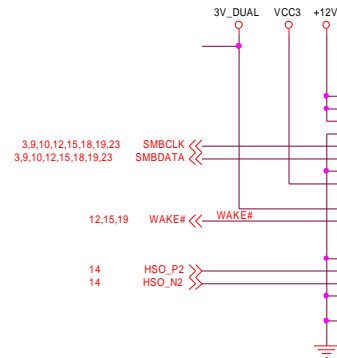
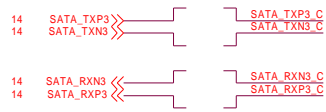
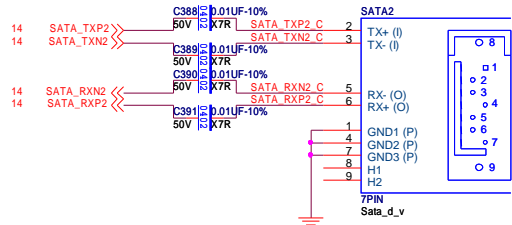
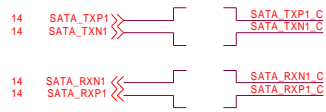
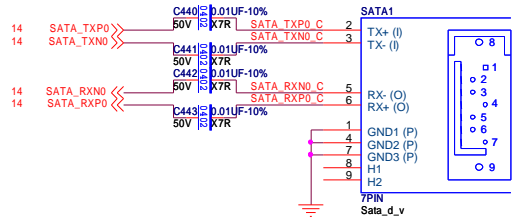
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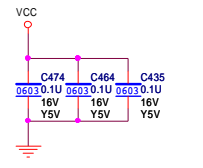
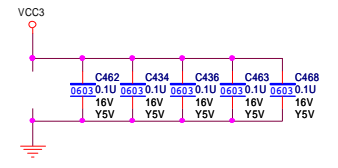
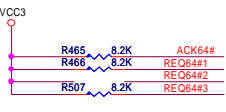
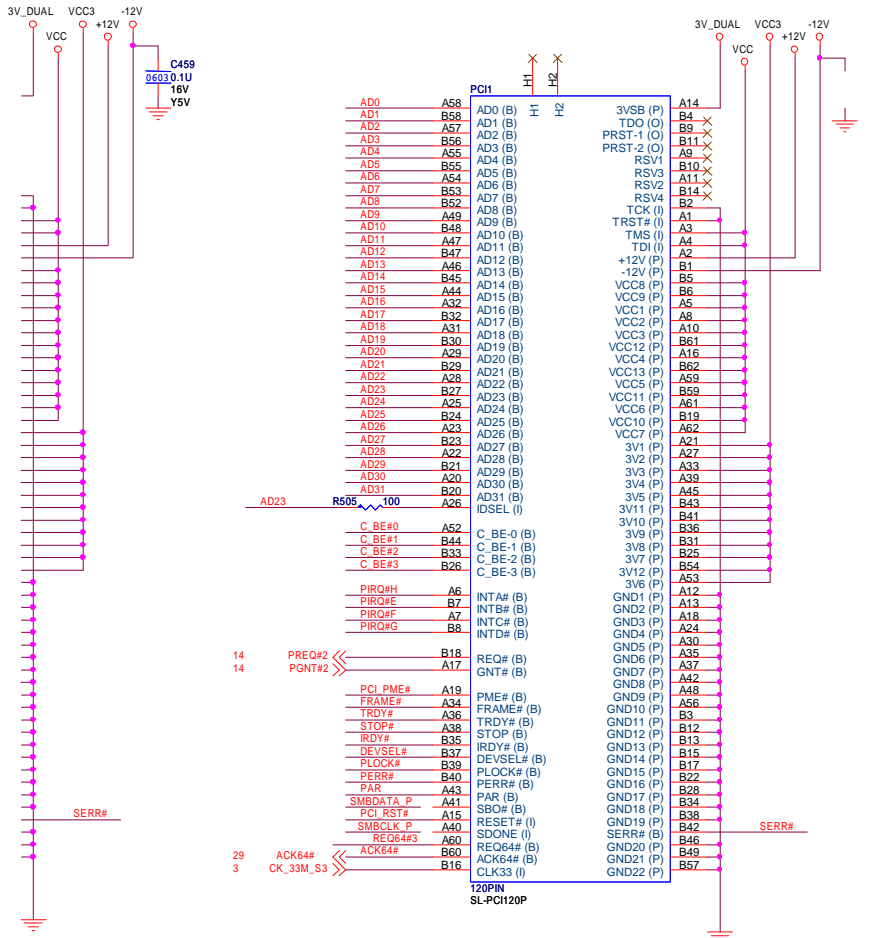


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14.29 AD[0..31] <<



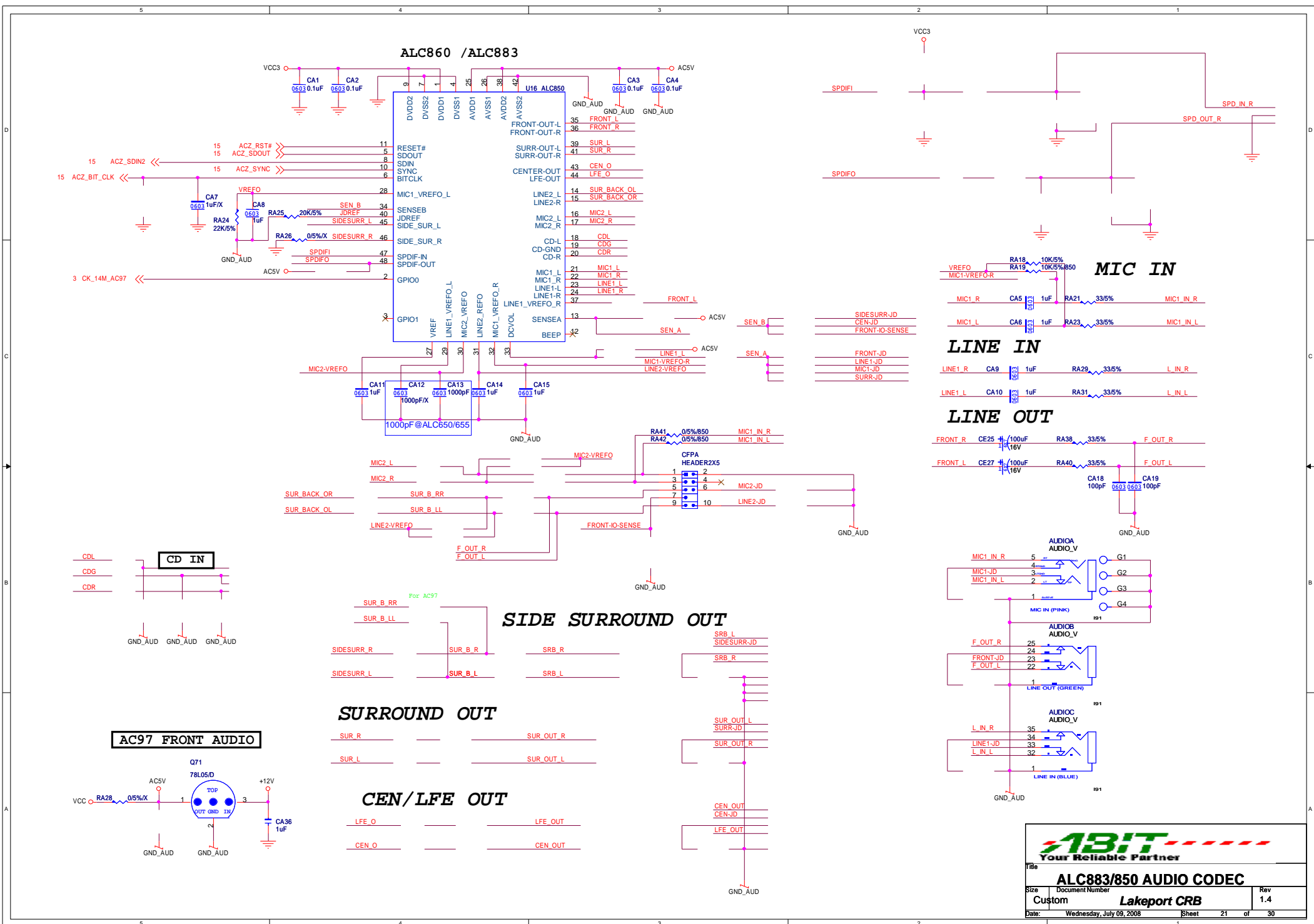
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Title: **PCI 1 & 2 & 3**

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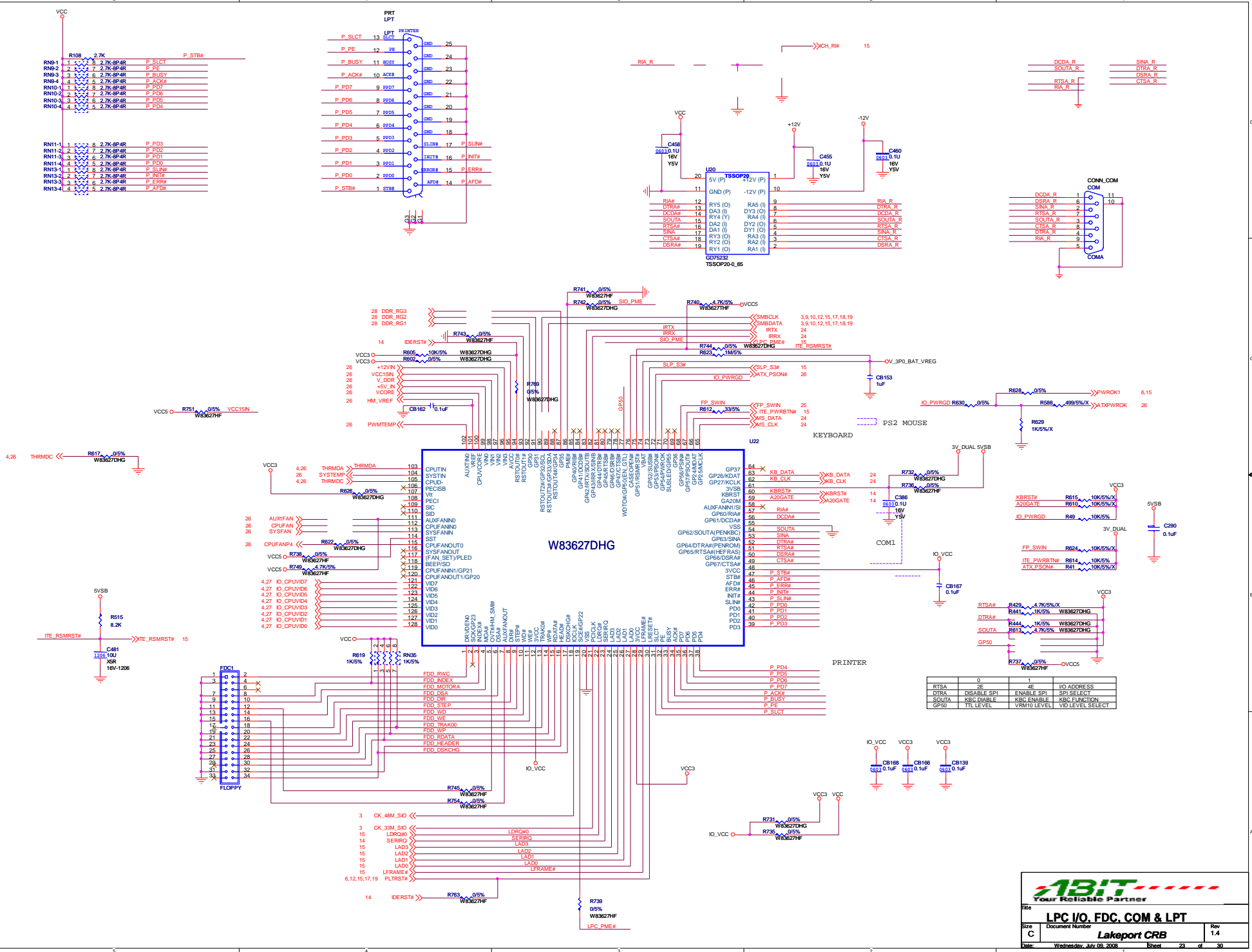


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Title: **ALC883/850 AUDIO CODEC**

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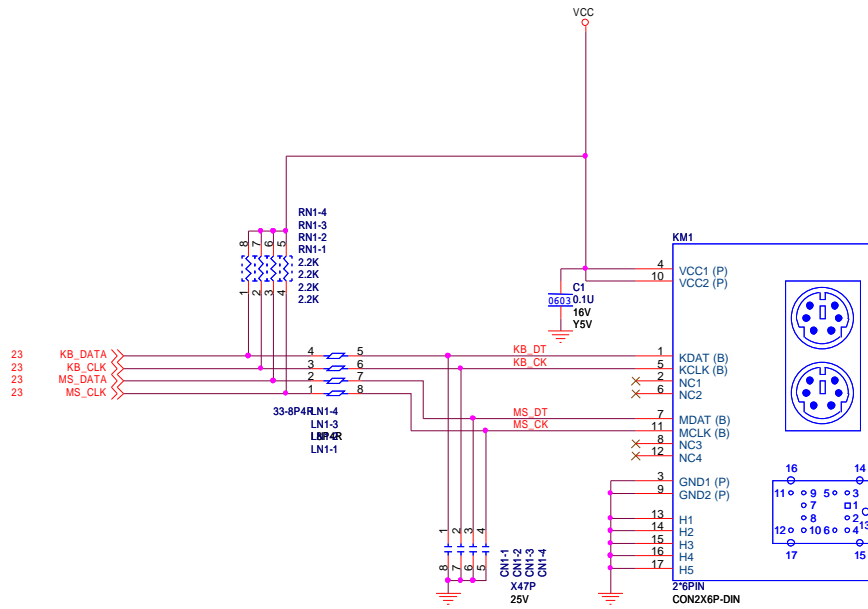
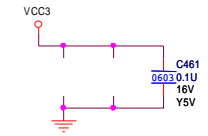
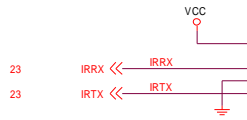


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File: **LPC I/O, FDC, COM & LPT**

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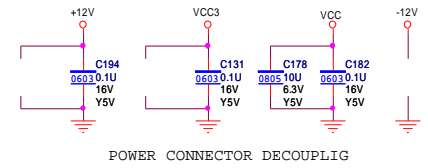
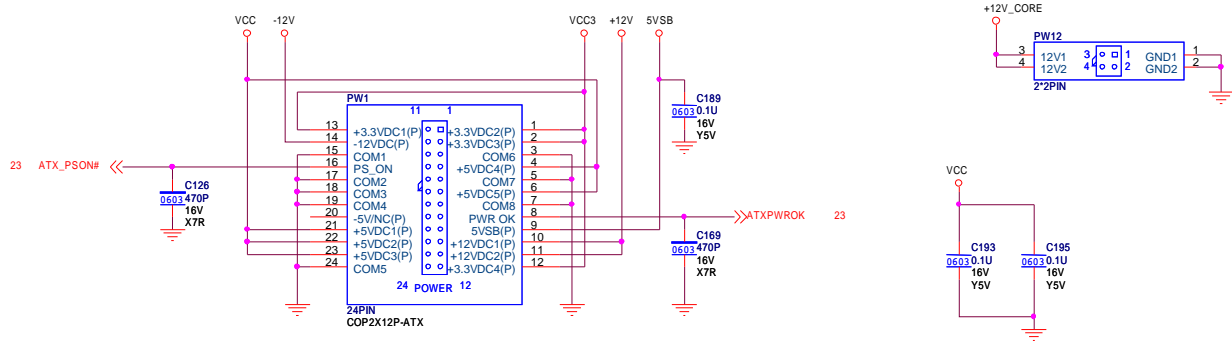
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Size: Custom      Document Number: **Lakeport CRB**      Rev: 1.4

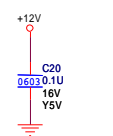
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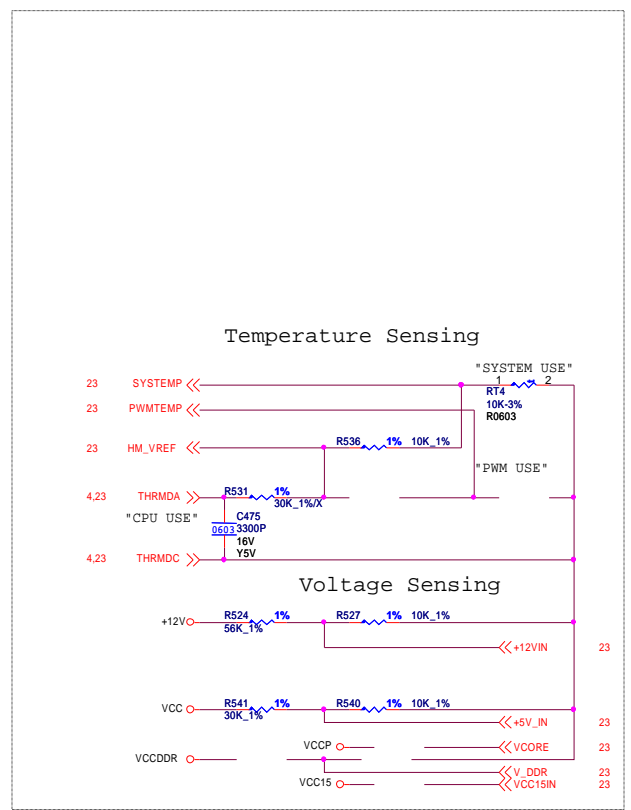
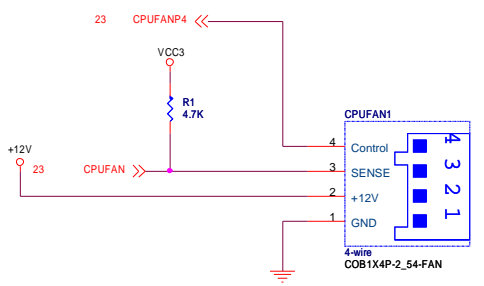
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"FOR LM358 / +12V"



**CPU FAN**

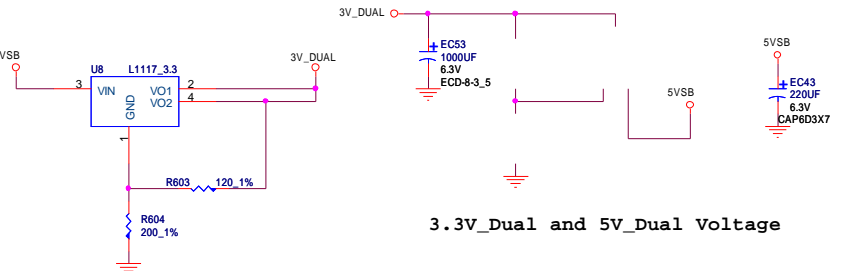
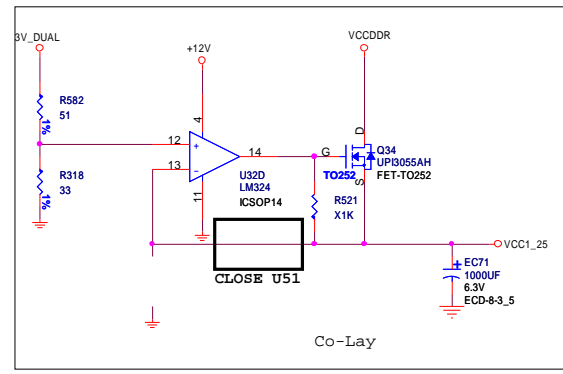
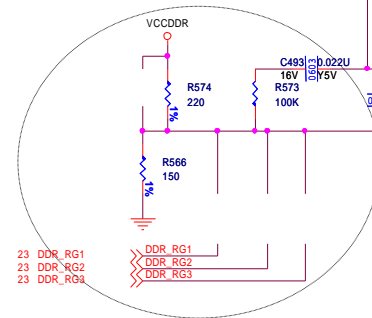
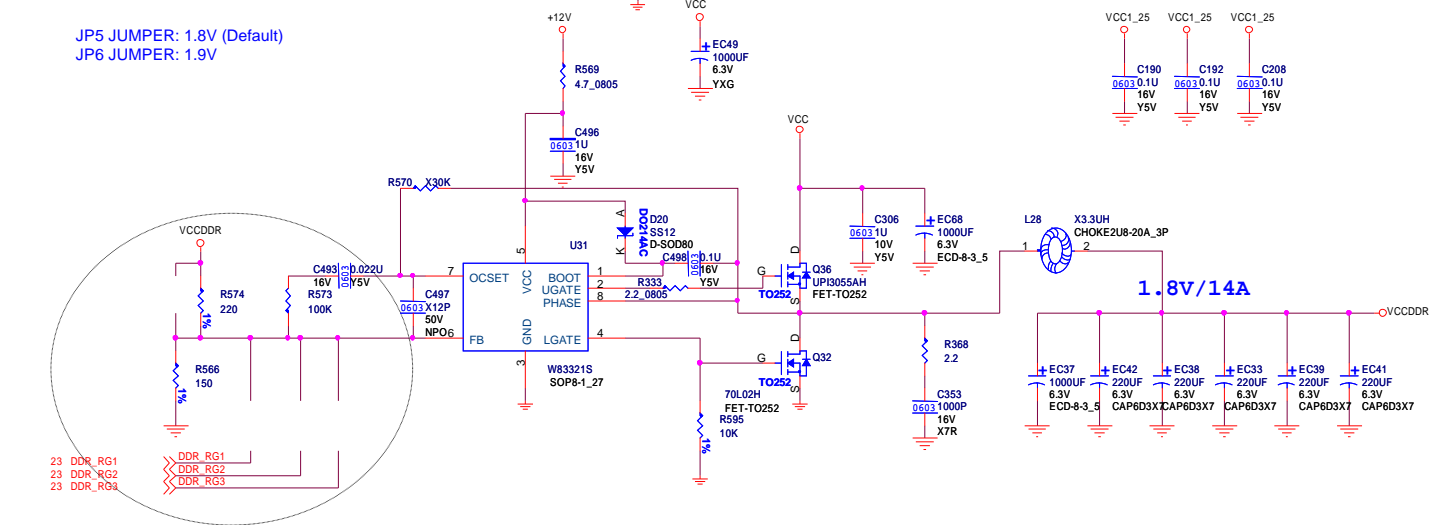
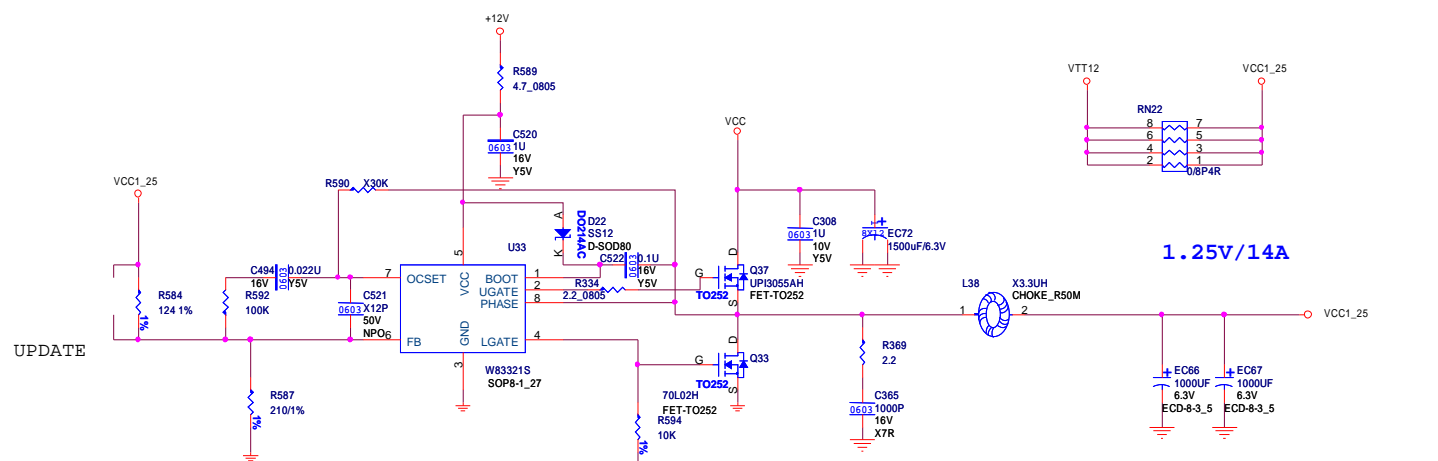
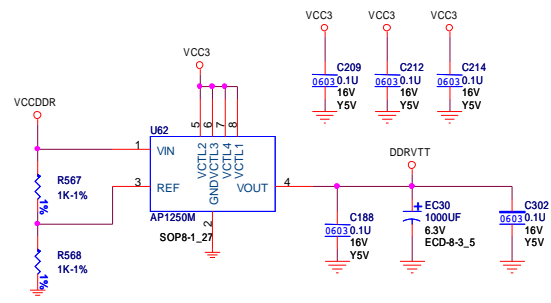
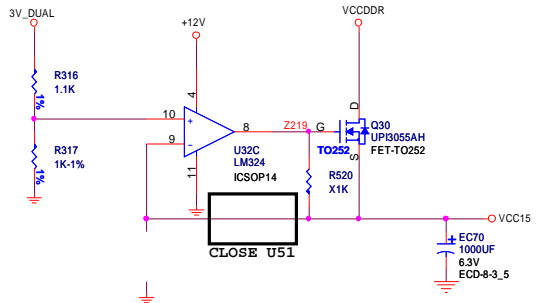
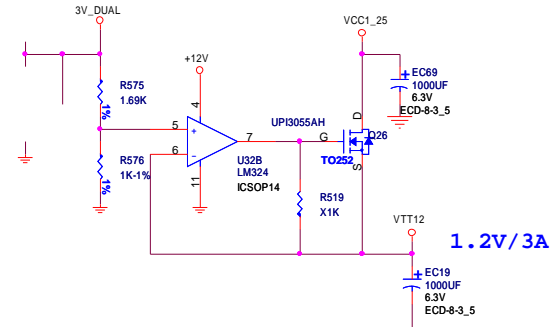
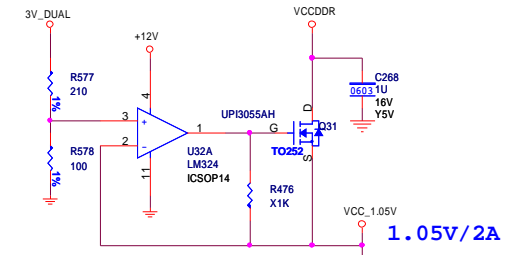


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**ATX POWER & FAN**

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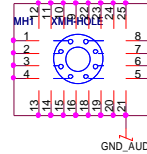
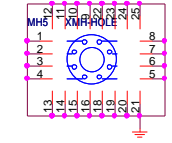
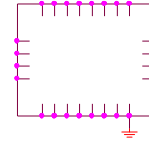
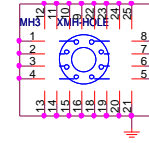
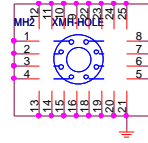
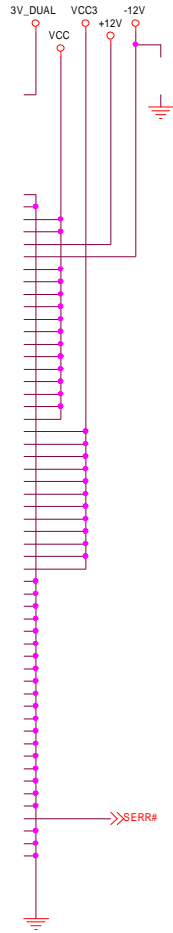


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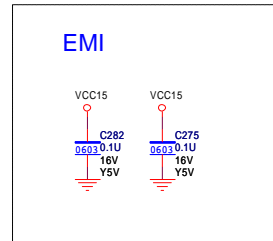
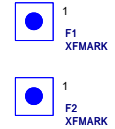
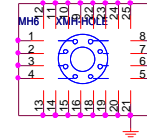
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- AD24
- 14,18 C\_BE#0
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  - 14,18 C\_BE#2
  - 14,18 C\_BE#3
  - 14,18 PIRQ#E
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  - 14,18 PIRQ#G
  - 14,18 PIRQ#H
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  - 14 PGNT#3
  - 14,18 PCI\_PME#
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REQ64#4

VCC3



GND\_AUD



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