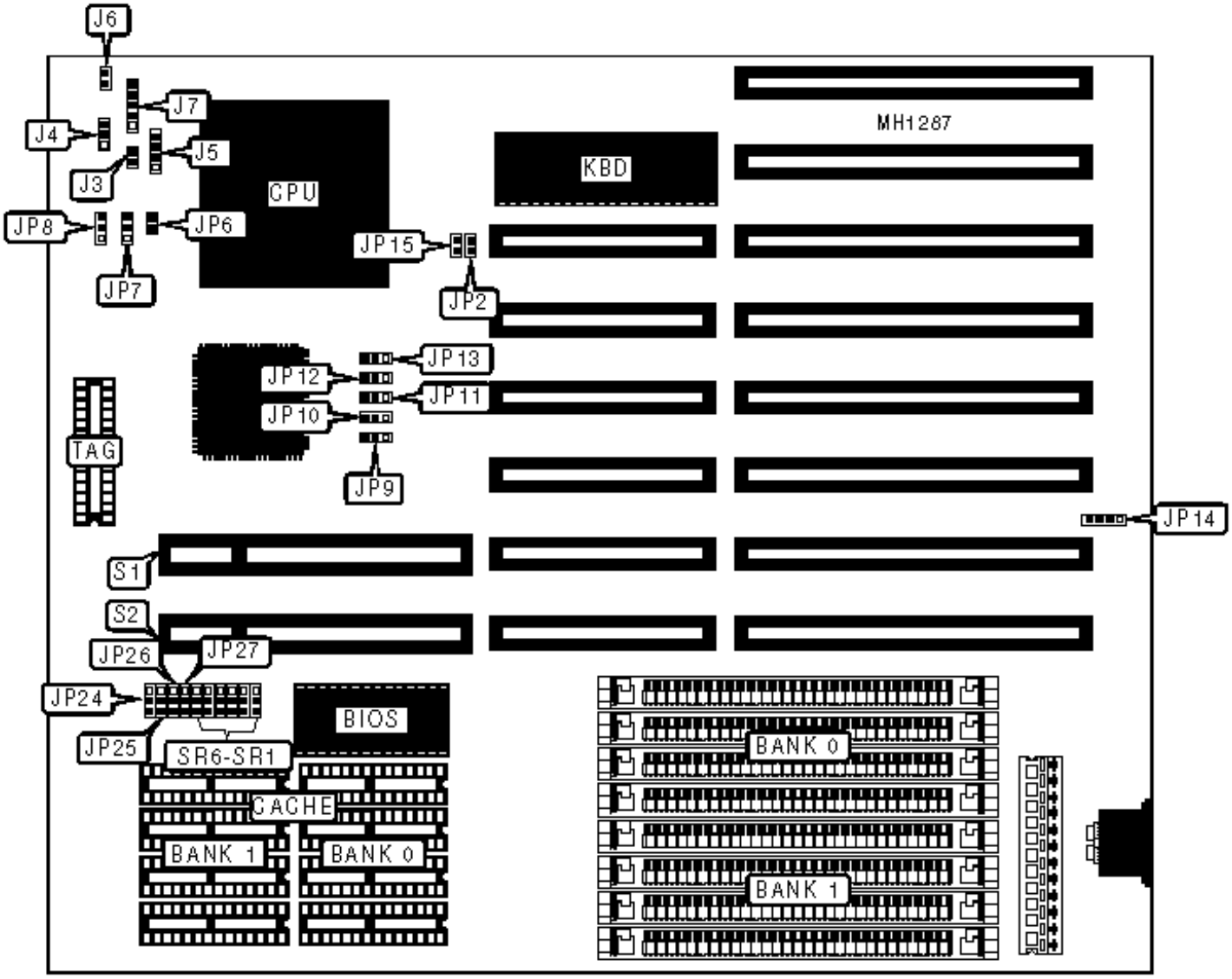
UNIDENTIFIED

LX400/P VESA LOCAL BUS

Configuration



CONNECTIONS

Purpose	Location	Purpose	Location
Turbo LED	J3	Reset switch	J6
Turbo switch	J4	Power LED & keylock	J7
Speaker	J5	32-bit VESA card (2)	S1 & S2

USER CONFIGURABLE SETTINGS

	Function	Jumper	Position
»	Factory configured - do not alter	JP1	closed
»	Monitor type select color	JP2	closed
	Monitor type select monochrome	JP2	open
»	Factory configured - do not alter	JP9	unknown
»	Power good signal detect from power supply	JP14	pins 1 & 2 closed
	Power good signal detect from board	JP14	pins 2 & 3 closed
»	Factory configured - do not alter	JP15	unknown
»	Factory configured - do not alter	JP16	unknown
»	Factory configured - do not alter	JP24	unknown
»	Factory configured - do not alter	JP25	unknown
»	VESA bus wait states select 0	JP26	open
	VESA bus wait state select 1	JP26	open
»	CPU speed select £ 33MHz	JP27	closed
	CPU speed select > 33MHz	JP27	closed

Note: The locations of JP1 and JP16 are unknown.

DRAM CONFIGURATION

Size	Bank 0	Bank 1

1MB	(4) 256K x 9	NONE
2MB	(4) 256K x 9	(4) 256K x 9
4MB	(4) 1M x 9	NONE
8MB	(4) 1M x 9	(4) 1M x 9
16MB	(4) 4M x 9	NONE
20MB	(4) 4M x 9	(4) 1M x 9
32MB	(4) 4M x 9	(4) 4M x 9

CPU SPEED CONFIGURATION				
Speed	JP10	JP11	JP12	JP13
66MHz (internal)	pins 1 & 2 closed	pins 2 & 3 closed	pins 1 & 2 closed	pins 1 & 2 closed
50MHz	pins 1 & 2 closed	pins 1 & 2 closed	pins 1 & 2 closed	pins 1 & 2 closed
50MHz (internal)	pins 2 & 3 closed	pins 2 & 3 closed	pins 1 & 2 closed	pins 1 & 2 closed
33MHz	pins 1 & 2 closed	pins 2 & 3 closed	pins 1 & 2 closed	pins 1 & 2 closed
25MHz	pins 2 & 3 closed	pins 2 & 3 closed	pins 1 & 2 closed	pins 1 & 2 closed
20MHz	pins 2 & 3 closed	pins 2 & 3 closed	pins 2 & 3 closed	pins 2 & 3 closed

CPU JUMPER CONFIGURATION			
CPU	JP6	JP7	JP8
80486DX	closed	pins 1 & 2 closed	pins 1 & 2 closed
80487SX	closed	pins 2 & 3 closed	pins 1 & 2 closed
80486SX	open	open	pins 2 & 3 closed

SRAM JUMPER CONFIGURATION			
Jumper	64KB	128KB	256KB
SR1	pins 2 & 3 closed	pins 1 & 2 closed	pins 2 & 3 closed

SR2	pins 2 & 3 closed	pins 1 & 2 closed	pins 2 & 3 closed
SR3	pins 1 & 2 closed	pins 2 & 3 closed	pins 2 & 3 closed
SR4	pins 2 & 3 closed	pins 2 & 3 closed	pins 2 & 3 closed
SR5	pins 1 & 2 closed	pins 2 & 3 closed	pins 2 & 3 closed
SR6	pins 1 & 2 closed	pins 1 & 2 closed	pins 2 & 3 closed

SRAM CONFIGURATION			
Size	Cache SRAM	Location	TAG
64KB	(8) 8K x 8	Banks 0 & 1	(1) 8K x 8
128KB	(4) 32K x 8	Bank 0	(1) 8K x 8
256KB	(8) 32K x 8	Banks 0 & 1	(1) 32K x 8