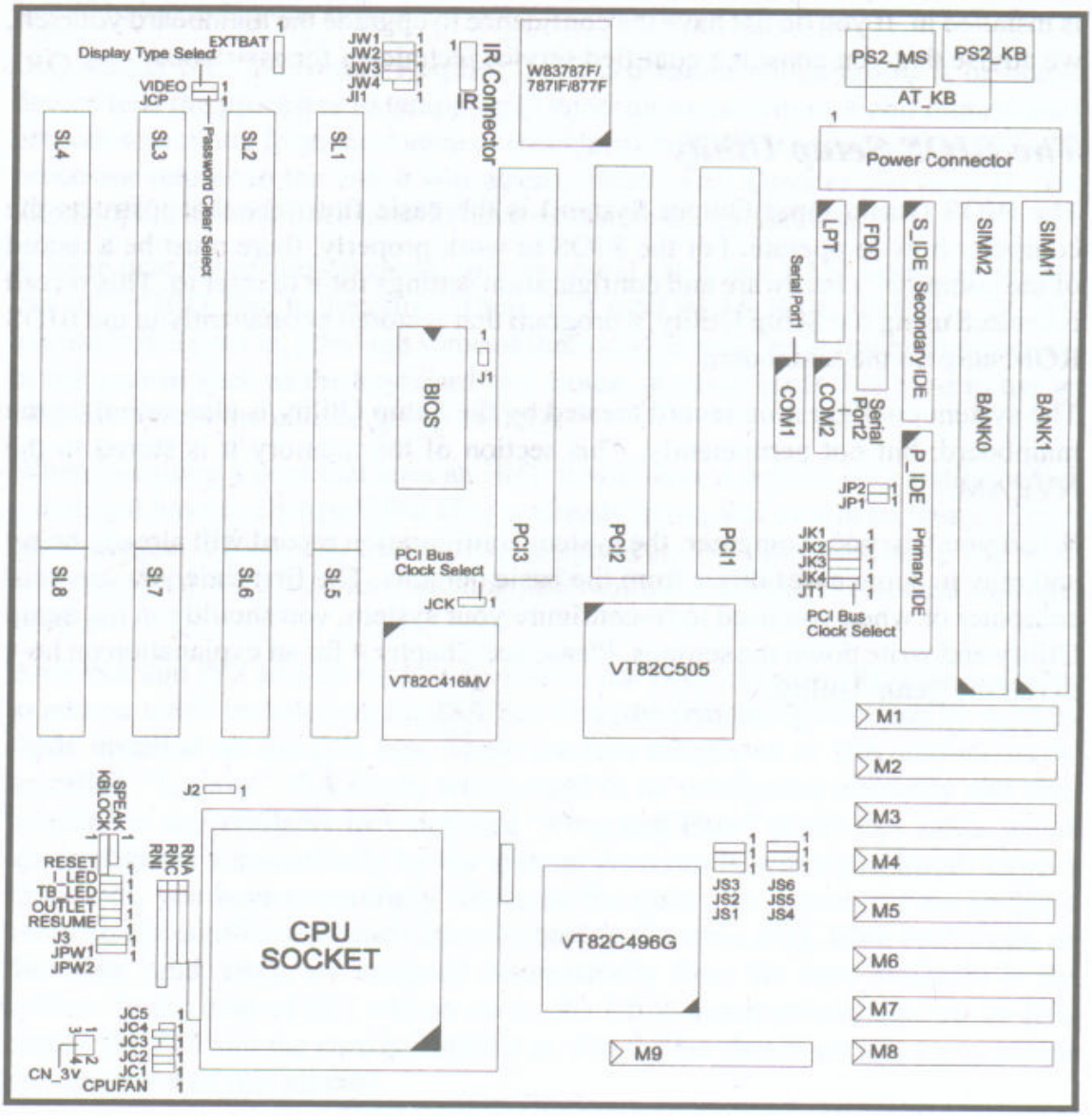
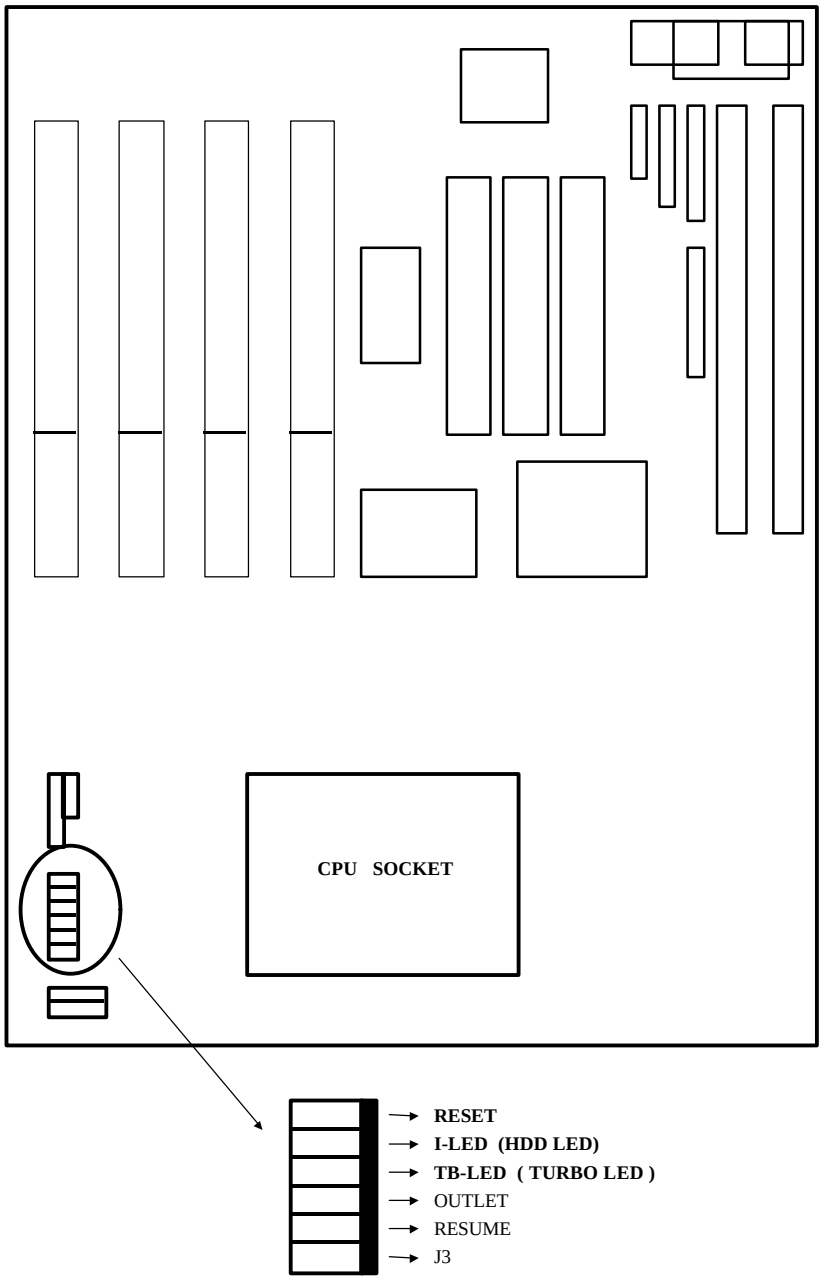
Mainboard Layout



NOTE : When plugging your CPU into the CPU (ZIF) socket, make sure that the pin 1 matches that of the CPU socket.

PIO3 LED PIN-OUT

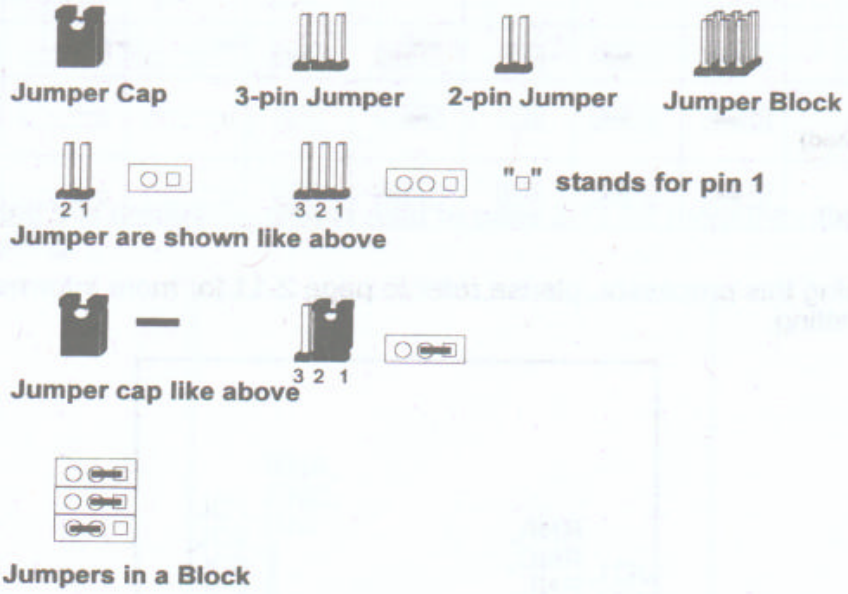


Mainboard Settings

The 486-PIO-3 has several user-adjustable jumpers on the board that allow you to configure your system to suit your requirements. This chapter contains information on the various jumper settings on your mainboard.

Jumpers

Jumpers are used to select the operation modes for your system. Some jumpers on the board have three metal pins with each pin representing a different function. To "**set**" a jumper, a black cap containing metal contacts is placed over the jumper pin/s according to the required configuration. A jumper is said to be "**shorted**" when the black cap has been placed on one or two of its pins. The types of jumpers used in this manual are shown below:



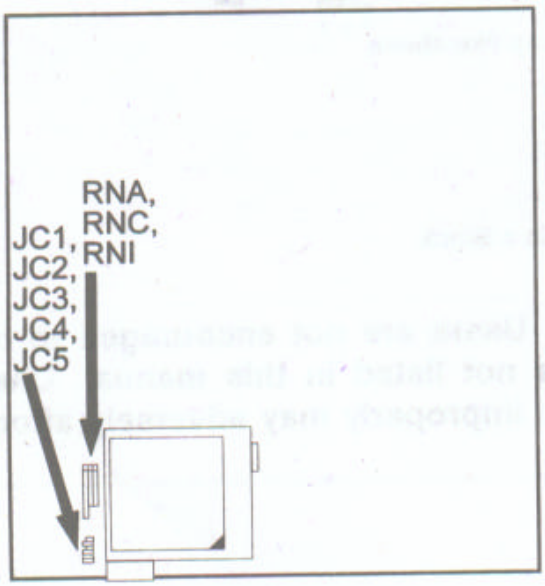
→ **NOTE : Users are not encouraged to change the jumper settings not listed in this manual. Changing the jumper settings improperly may adversely affect system performance.**

CPU Jumper Settings: JC1, JC2, JC3, JC4, JC5, RNA, RNC, RNI

Intel :
486SX/DX/DX2; DX4 ODP; P24S; P24D; P24T;
IntelDX4 -
(Double-Speed: A80486DX4-XX*,
Triple-Speed: A80486DX4-XX*)

	JC1	JC2	JC3	JC4	JC5	RNA	RNC	RNI
486SX						1	1	1 8P4R
486DX/DX2 P24S								8P4R
DX4 ODP P24D								8P4R
P24T								8P4R
DX4 (Double-Speed)								8P4R
DX4 (Triple-Speed)								8P4R

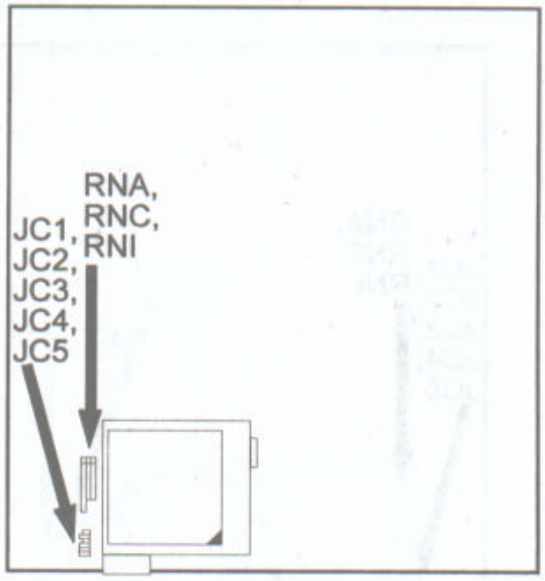
* When using this processor, please refer to page 2-11 for more information about jumper setting.



AMD :
486DX2 -
(A80486DX2-XXV8T*, A80486DX2-XXNV8T*);
486DX4 -
(A80486DX4-100NV8T*, A80486DX4-XXSV8B*,
Am486DX4-100V8T*);
AMD-X5*

	JC1	JC2	JC3	JC4	JC5	RNA	RNC	RNI
486DX2						1	1	1
Enhanced 486DX2								
486DX4								
Enhanced 486DX4								
AMD-X5								

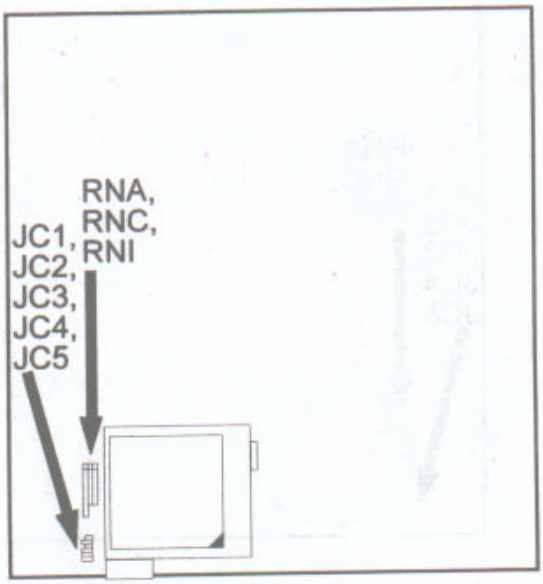
* When using this processor, please refer to page 2-11 for more information about jumper setting.



UMC :
U5S/U5SD/U5SLV -
(U5SX-SUPERXX, U5SD-SUPERXX, U5SLV-SUPERXX*);
Cyrix :
Cx486DX/DX2/DX4 -
(Cx486DX-XXGP, Cx486DX-VXXGP*,
Cx486DX2-XXGP, Cx486DX2-VXXGP*, Cx486DX4-100*);
5x86 -
(5x86-100*, 5x86-120*)

	JC1	JC2	JC3	JC4	JC5	RNA	RNC	RNI
U5SD						1 8P4R	1	1
U5S U5SLV						8P4R		
Cx486DX Cx486DX2							8P4R	
Cx486DX4 5x86								8P4R

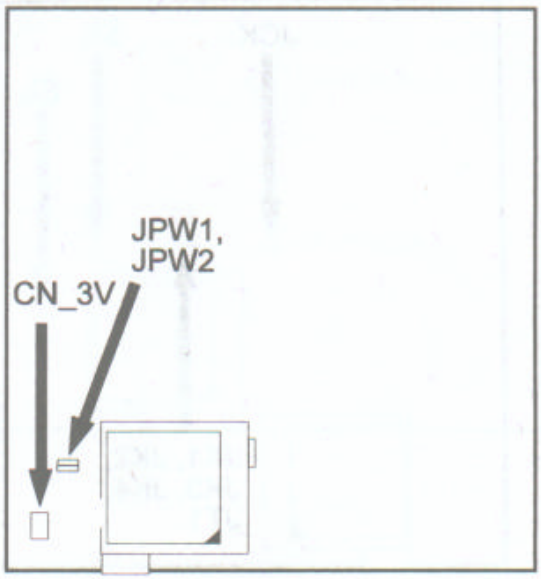
* When using this processor, please refer to page 2-11 for more information about jumper setting.



Low-Voltage CPU Jumper Setting

CPU Voltage Type	Jumper Setting	CPU Model	
3.3V	*JPW1* *JPW2*	*UMC -* U5SLV-SUPERXX	*AMD -* AMD-X5
3.45V	*JPW1* *JPW2*	*AMD -* A80486DX4-100NV8T A80486DX2-XXNV8T A80486DX4-XXSV8B *INTEL 486 -* A80486DX4-75 *Cyrix -* *5x86-100*	 A80486DX2-XXSV8B Am486DX2-XXV8T Am486DX4-100V8T A80486DX4-100 *5x86-120*
3.6V	*JPW1* *JPW2*	*Cyrix -* Cx486DX-VXXGP	
4.0V	*JPW1* *JPW2*	*Cyrix -* Cx486DX2-V80GP	

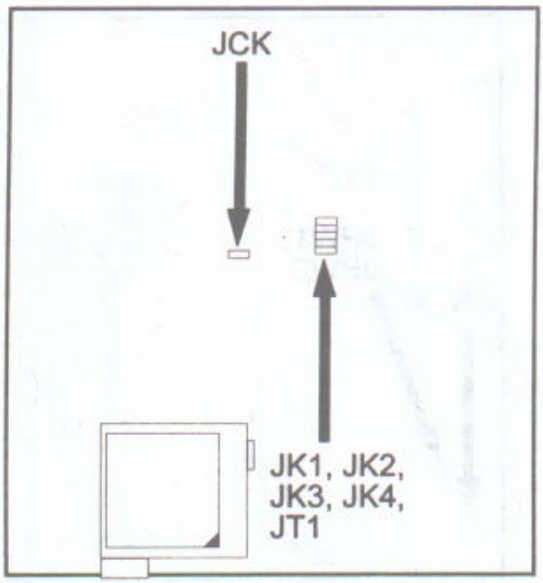
CN_3V	1 2 3 4	For 3.3V, 3.45V, 3.6V and 4.0V CPUs
	1 2 3 4	For 5V CPUs (Default)



CPU Clock Jumper Setting

	50 MHz DX-50	*40 MHz* DX-40 DX2-80	*33.3 MHz (Default)* SX-33 DX-33 DX2-66 DX4-100 X5-133	*25 MHz* SX-25 DX-25 SX2-50 DX2-50 DX4-75
JK1				
JK2				
JK3				
JK4				

JT1, JCK		***PCI Bus Clock Select***
		(When the processor clock is less than or equal to 33 MHz.) PCI Bus Clock = Processor Clock (Default)
		(When the processor clock is greater than 33 MHz.) PCI Bus Clock = Processor Clock / 2



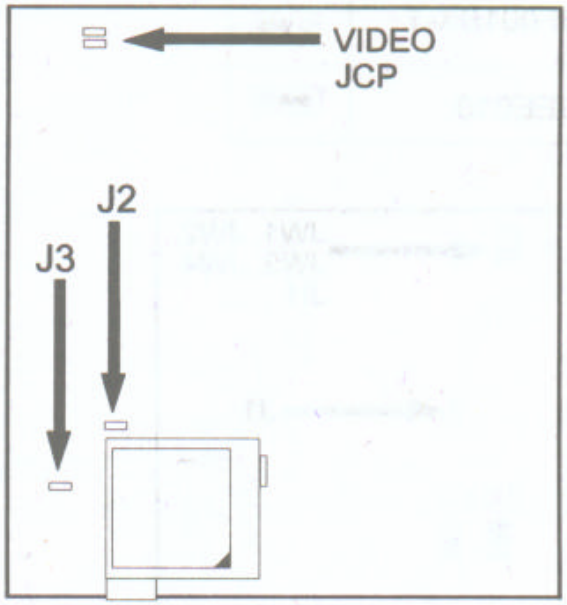
Password Clear: JCP
Display Type Select: VIDEO
KB_LOCK Mode Select: J2
TB_LED Mode Select: J3

Password Clear	JCP
Enabled	
Disabled (Defalut)	

KB_LOCK Mode	J2
IOCHCK	
KB_.LOCK (Default)	

Display Type	VIDEO
Mono/EGA/VGA (Default)	
CGA	

TB_LED Mode	J3
G_LED	
TB_LED (Default)	



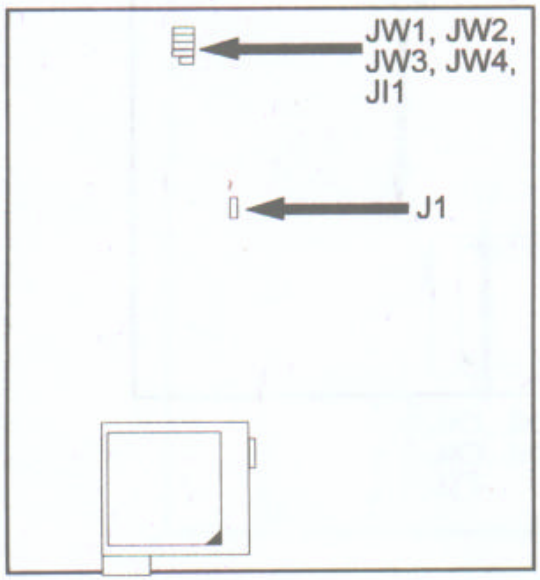
W83787F/787IF Controller: JW1, JW2, JW3, JW4, JI1, J1

W83787IF/877F	JW1	JW2
COM2		
Infrared		

ECP Mode	JW3	JW4
DMA 1 (Default)		
DMA 3		

Printer Port Direction	JI1
OUTPUT	
Bidirection (Default)	

Programmable Flash EPROM Type	J1
Intel 28F001BX-T	
SST 29EE010	

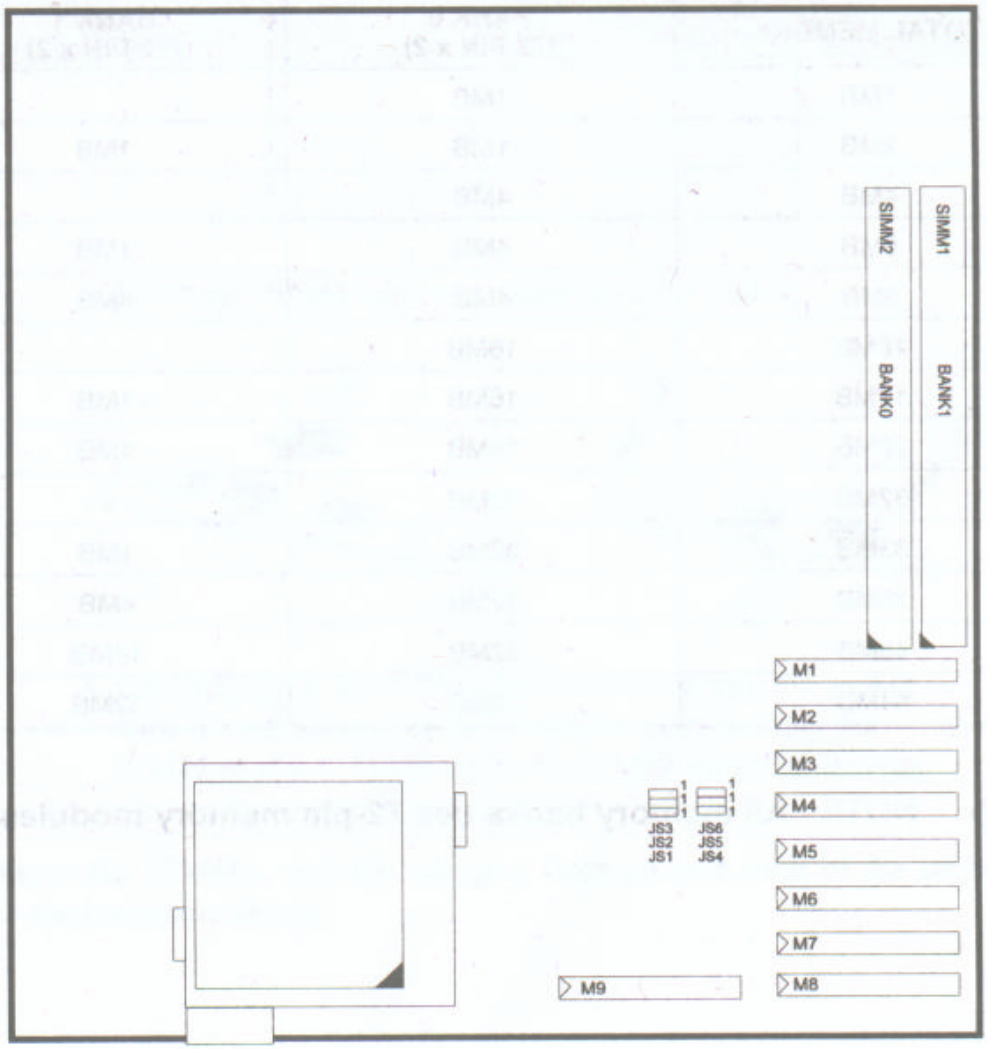


System Memory

The 486-PIO-3 can be equipped with the necessary memory for running all your applications. Memory comes in the form of DRAM (SIMMs) and cache SRAM. This chapter describes these two types of memory and gives instructions on how to install each type on the mainboard.

Memory Locations

The board layout below shows the locations of the DRAM memory banks and the cache SRAM:



Installing DRAM

SIMM Banks

The 486-PIO-3 can accommodate onboard memory from 1 to 64MB using SIMMs (Single-In-Line Memory Modules, one SIMM shown below.) The mainboard has two memory banks — Bank 0 and Bank 1. Each bank has two SIMM sockets which can accept either a 1, 4, 16 or 32MB SIMM in each socket.

DRAM Configuration

Memory may be installed as suggested in the following table. It does not matter to start the installation from Bank 0 or Bank 1.

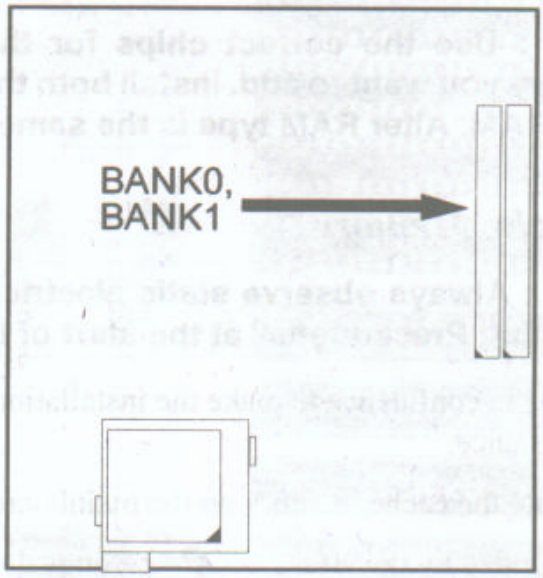
TOTAL MEMORY	BANK 0 (72-PIN x 2)	BANK 1 (72-PIN x 2)
1MB	1MB	
2MB	1MB	1MB
4MB	4MB	
5MB	4MB	1MB
8MB	4MB	4MB
16MB	16MB	
17MB	16MB	1MB
20MB	16MB	4MB
32MB	32MB	
33MB	32MB	1MB
36MB	32MB	4MB
48MB	32MB	16MB
64MB	32MB	32MB

→ **NOTE : All memory banks use 72-pin memory modules.**

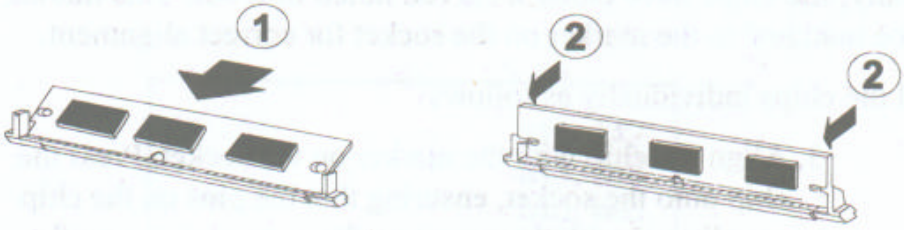
Installation Instructions

→ **NOTE : Always observe static electricity precautions. See "Handling Precautions" at the start of this manual.**

1. Locate the SIMM banks on the mainboard.



2. Insert the SIMM edge connector onto the socket.



3. Carefully push the SIMM down and back into the socket until the retaining clips of the socket snap, holding the SIMM in place. The holes in the SIMM should match the pins on the socket's retaining clips.

To remove the SIMM/s, pull the retaining latch on both ends of the socket and reverse the procedure above.

Cache Memory

The 486-PIO-3 can accept cache SRAM of 128K/256K/512K/1MB in DIP packages. Every time the CPU wants to write data to the external memory, if the location in SRAM is a "**hit**", it writes this data to the cache RAM directly, not to the DRAM.

→ **NOTE : Use the correct chips for the amount of cache memory you want to add. Install both the correct Cache and Tag SRAM. Alter RAM type is the same as Tag RAM.**

Installing Cache Memory

→ **NOTE : Always observe static electricity precautions. See "Handling Precautions" at the start of this manual.**

If you do not have the confidence to make the installation, better consult a service technician for assistance.

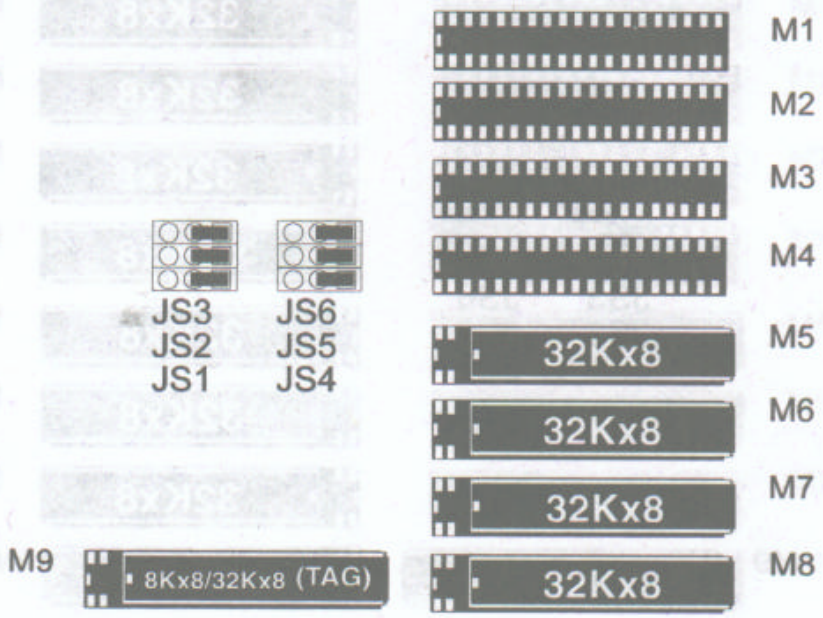
1. Locate the cache memory on the mainboard.
2. Be guided by the Cache SRAM settings depending on your desired SRAM configuration.

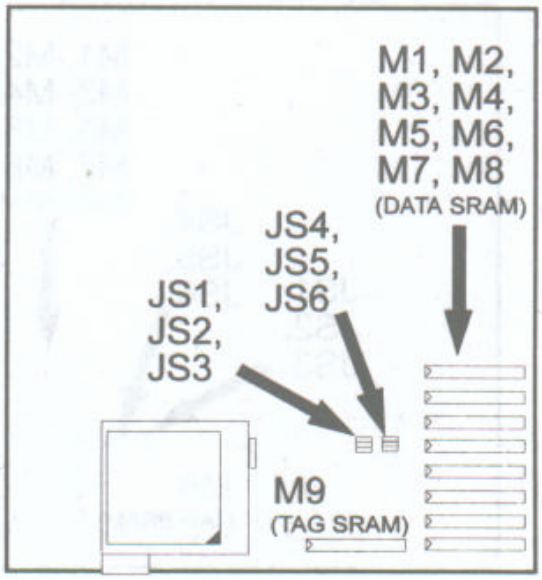
Correct orientation of the chip is necessary for the cache to operate properly. Normally, the chips have either a curved notch or a dot. This marker on the chip must be matched to the marker on the socket for correct alignment.

Install the chips individually as follows:

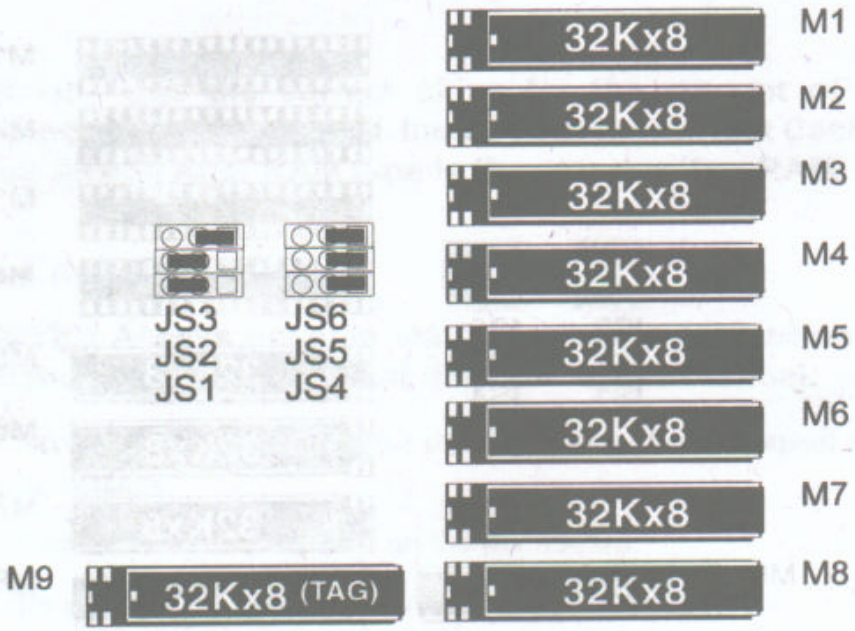
3. Align the chip with the marker on the socket. Press the chip onto the socket, ensuring that the pins on the chip are aligned with the corresponding connections on the socket.
4. Press the chip completely into the socket so that the pins are properly seated.

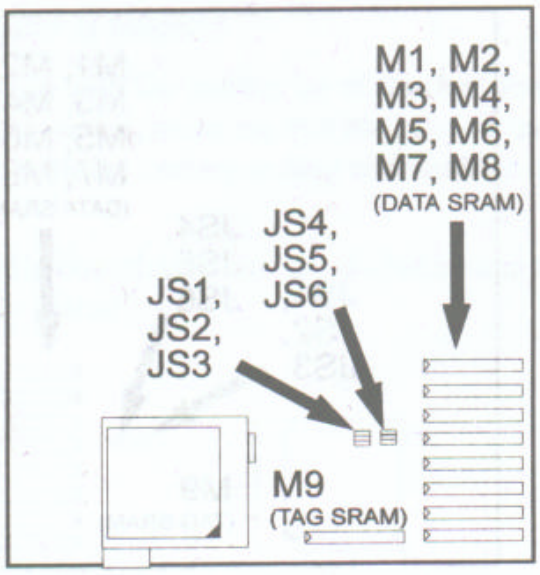
128KB Cache SRAM



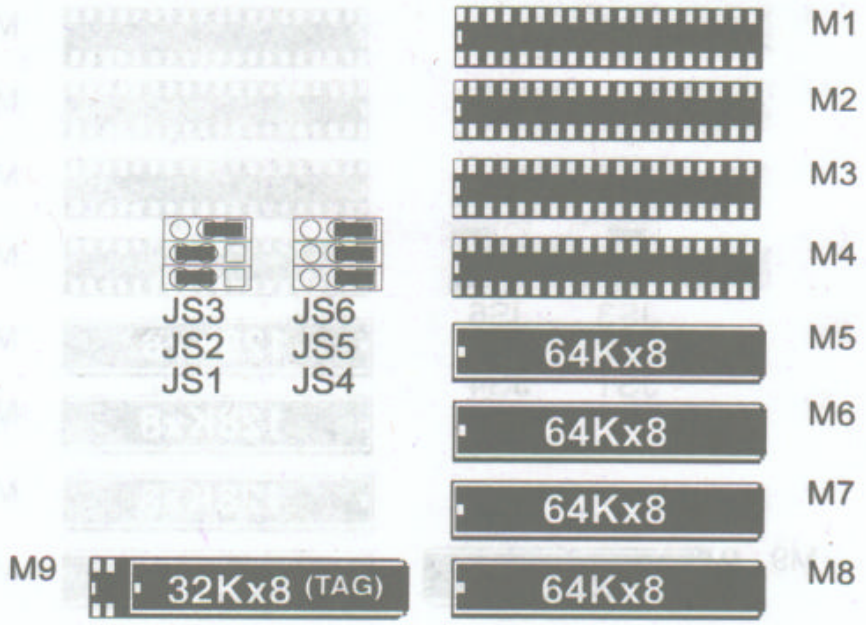


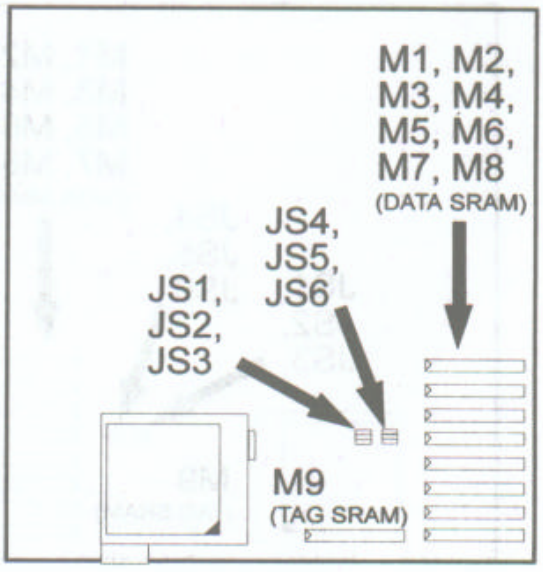
256KB Cache SRAM



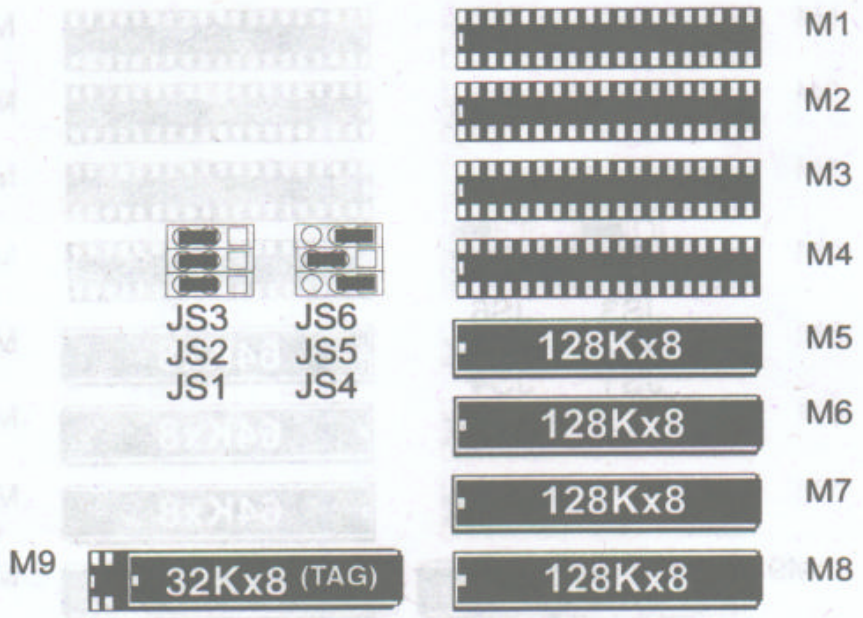


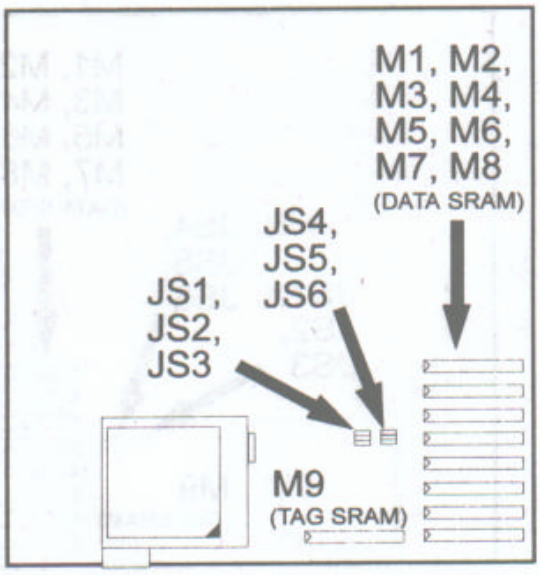
256KB Cache SRAM (The Alternative Insertion)





512KB Cache SRAM





512KB Cache SRAM (The Alternative Insertion)