Mainboard Layout

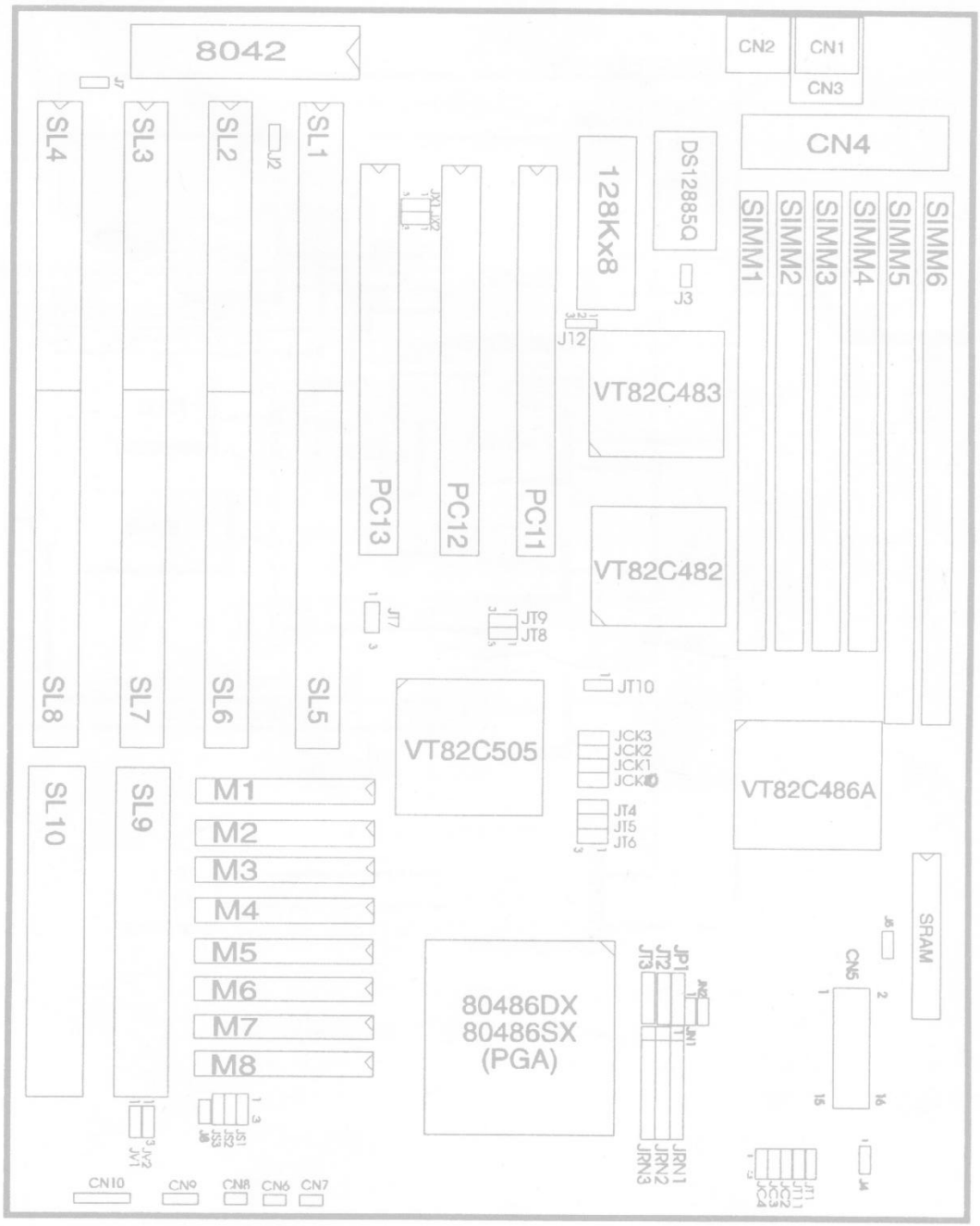

Figure 1-1. Mainboard Layout

Mainboard Settings

The 486-VIP has several user-adjustable jumpers and connectors on the board that allow you to configure your system to suit your every need. This chapter contains information on the various jumper and connector settings you can make on your mainboard.

Jumpers

Jumpers are used to select the operation modes for your system. Some jumpers on the board have three metal pins with each pin representing a different function. To "set" a jumper, a black cap containing metal contacts is placed over the jumper pin/s according to the required configuration. A jumper is said to be "shorted" when the black cap has been placed on one or two of its pins, as shown in the figure below:

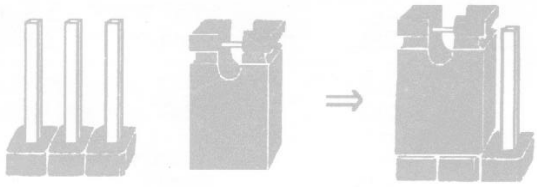

Figure 2-1. Jumper with Pins Shorted

CPU Selector Jumpers

To allow your system to be used with a variety of CPUs, 486-VIP provides jumpers that can be set according to the CPU you want installed. Follow the diagrams found in the lower-middle area of the board to determine the proper arrangement for the CPU you are using.

The next three tables summarizes the settings of the CPU Selector jumpers:

JUMPER	486SX/ Cx486S (M6)	486DX/IntelDX2™ IntelDX4™ Cx486DX (M7)	487SX/P24CT* P24T*
JC2	2-3	1-2	1-2
JC3	2-3	1-2	1-2
JC4	open	1-2	2-3

* P24T and P24CT are the Pentium OverDrive Processors.

JUMPER (RP 0Ω SIP)	Am486DXL	IntelDX4™ SL-enhanced/ P24T	Cx486S/DX	486DX
JRN1	inserted	empty	empty	empty
JRN2	empty	inserted	empty	empty
JRN3	empty	empty	inserted	empty

→ **Note : When the 3.3 volt regulator is not present, the 3.3 volt daughter board should be installed. If not, please read page 2-6 "3.3 Volt Regulator Board Installation".**

JUMPER	PIN DEFINITION	
JT1	1-2 2-3	Cyrix DX Cyrix DX2
JT2	1-2 2-3	IntelDX4™ 3 X mode IntelDX4™ 2 X mode
JT3	1-2 2-3	P24T internal write-back cache P24T internal write-through cache
JT4	1-2 2-3	Other CPUs P24T
JN1, JN2	Short Open	P24D (Pentium OverDrive Processor) Other CPUs
JT5*	1-2 2-3	A26 (default) For card that uses A31
JT6	1-2 2-3	Address area is programmed in VT82C505 chip Supports IRQ15 when SMI# is used
JT7, JT8, JT9 JT11	1-2	(factory default)

*Only one jumper cap is allowed, either JT5 or JT6. Cannot short both jumpers at the same time.

Table 2-1. Jumper Settings for CPU Selector (Continued)

JUMPER	PIN DEFINITION
JT10	1-2 When a PCI IDE card is used 2-3 (default)
JT12	1-2 Other CPUs 2-3 Cyrix CPU
JX1	Power Management Interrupt Select 1-2 Regular CPU (default) 2-3 Cyrix or Intel SL-enhanced CPU
JX2	2-3 (factory default)
JP1	1-2 Regular CPU 2-3 Cyrix or Intel SL-enhanced CPU

Table 2-1. Jumper Settings for CPU Selector

JUMPER	PIN DEFINITION
J2	Dispaly Type Select Short Color Open Mono/EGA/VGA
J3	CMOS Clear Short Clear CMOS Open (default)
J4	Disable Outlet
J5	Green Status LED
J7	Clear Password
J8	Hardware Suspend
JRN4, JRN6 (RP 0Ω SIP)	Internal/External Keyboard Controller Select Inserted Internal keyboard and PS/2 mouse Empty External keyboard and PS/2 mouse
JRN5, JRN7 (RP 0Ω SIP)	Internal/External Keyboard Controller Select Inserted External keyboard and PS/2 mouse Empty Internal keyboard and PS/2 mouse

Table 2-2. Jumper Definitions

CPU Clock VIA (JK1 - JK4)

CLK	JK1	JK2	JK3	JK4
25 MHz	2-3	1-2	2-3	1-2
33.3 MHz	2-3	2-3	1-2	1-2
40 MHz	1-2	1-2	2-3	1-2
50 MHz	2-3	1-2	2-3	2-3

Table 2-3. CPU Clock VIA Jumper Selection (JK1 - JK4)

Connectors

The connectors allow the mainboard to connect electronically with other parts of the system. Some connectors have two pins, others have four or five pins. Some malfunction problems encountered with your system may be caused by loose or improper connections. Ensure that all connections are in place and firmly attached.

CONNECTOR	PIN OUTS	SIGNAL NAME
CN1 PS/2 Keyboard Connector	1 2, 6 3 4 5	Keyboard data NC Ground + 5V Keyboard clock
CN2 PS/2 Mouse Connector	1 2 3 4 5	Mouse data NC Ground + 5V Mouse clock
CN4 Power Connector	1 2, 10, 11, 12 3 4 5, 6, 7, 8 9	Power good + 5V + 12V - 12V Ground - 5V

Table 2-4. Connector Pin Definitions (Continued)

CONNECTOR	PIN OUTS	SIGNAL NAME
CN5* 3.3V Daughter Board Connectors	1, 3, 14, 16 2, 4, 13, 15 5, 12 6 7, 8, 9, 10 11	+ 3.3V + 5V Voltage switch signal NC Ground + 12V
CN7 Turbo LED Connector	1 2	LED + LED -
CN8 Reset Switch Connector	1 2	Ground Reset signal
CN9 Speaker Connector	1 2 3 4	Speaker signal NC Ground + 5V
CN10 Keyboard and Power LED Connector	1, 2 3, 5 4	Power LED Ground Keyboard lock

* When the onboard 3.3 volt regulator is not present, the 3.3 volt daughter board should be installed. If not, please refer to page 2-6 installation of the 3.3 volt regulator daughter board.

Table 2-5. Connector Pin Definitions

→ **Note : Users are not encouraged to change the jumper settings not listed in this manual. Changing the jumper settings improperly may adversely affect system performance.**

VESA Bus Connector

The mainboard provides two high-performance VESA bus connectors, SL9 and SL10, for use with VESA peripherals. The VESA bus connector can be utililized for one Local Bus Master or one Local Bus Slave. The table below gives more information on settings on the mainboard and the VL-bus controller.

JUMPER	PIN DEFINITION
JV1	High Speed Write Select 1-2 One wait write 2-3 Zero wait write
JV2	CPU Speed Select 1-2 ≤ 33MHz (default) 2-3 > 33MHz

Table 2-5. VESA Bus Connector Pin Definitions

Memory Subsystem

The 486-VIP is equipped with the memory necessary for running all your applications. Memory comes in the form of DRAM (SIMMs) and cache SRAM. This chapter describes these two kinds of memory and gives instructions on how to install each kind on the mainboard.

Memory Locations

The board layout below shows the locations of the DRAM memory banks and the cache SRAM:

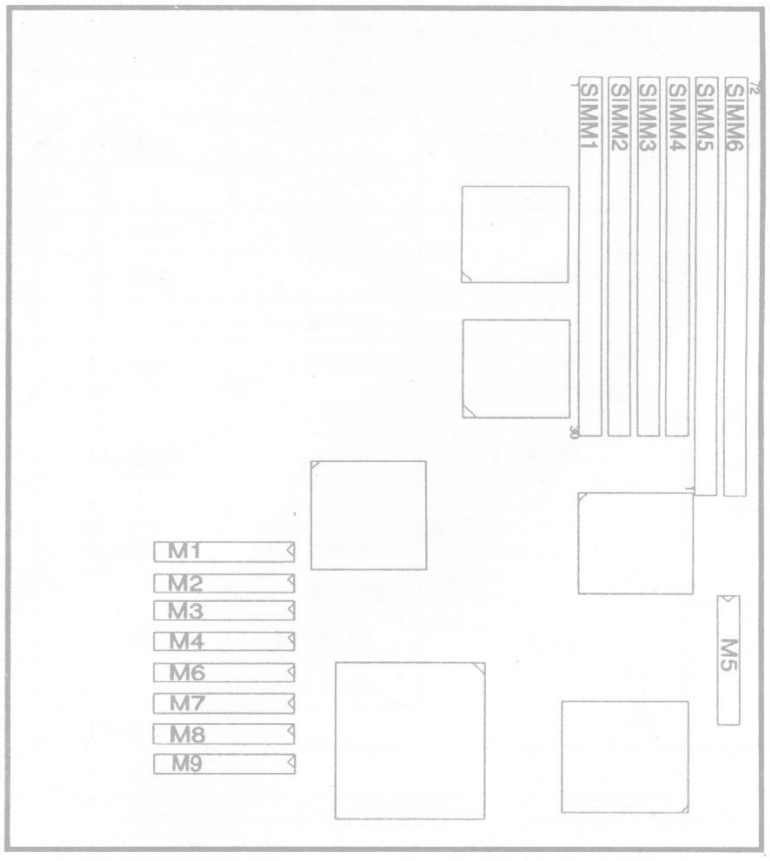

Figure 3-1. Cache and Memory Locations

Installing DRAM

SIMM Banks

The 486-VIP can accommodate on-board memory from 1 to 96MB using SIMMs (Single-In-Line Memory Modules). The mainboard has four memory banks — Bank 0, 1, 2, 3. Each bank can accept either a lMB, 4MB, or 16MB SIMM in each socket.

DRAM Configuration

Memory can be installed in a variety of configurations, as shown in the next table:

TOTAL MEMORY	BANK 0 (30-PIN)	BANK 1 (72-PIN)	BANK 2 (72-PIN)
1MB	256KB x 4		
		1MB x 1	
			1MB x 1
2MB	256KB x 4	1MB x 1	
		1MB x 1	1MB x 1
	256KB x 4		1MB x 1
3MB	256KB x 4	1MB x 1	1MB x 1
4MB	1MB x 4		
		4MB x 1	
			4MB x 1
5MB	256KB x 4	4MB x 1	
	256KB x 4		4MB x 1
	1MB x 4	1MB x 1	
	1MB x 4		1MB x 1
		1MB x 1	4MB x 1
		4MB x 1	1MB x 1

Table 3-1. DRAM Configurations (Continued)

TOTAL MEMORY	BANK 0 (30-PIN)	BANK 1 (72-PIN)	BANK 2 (72-PIN)
6MB	256KB x 4	4MB x 1	1MB x 1
	256KB x 4	1MB x 1	4MB x 1
	1MB x 4	1MB x 1	1MB x 1
8MB	1MB x 4	4MB x 1	
	1MB x 4		4MB x 1
		4MB x 1	4MB x 1
9MB	256KB x 4	4MB x 1	4MB x 1
	1MB x 4	1MB x 1	4MB x 1
	1MB x 4	4MB x 1	1MB x 1
12MB	1MB x 4	4MB x 1	4MB x 1
16MB	4MB x 4		
		16MB x 1	
			16MB x 1
17MB	256KB x 4	16MB x 1	
	256KB x 4		16MB x 1
		1MB x 1	16MB x 1
		16MB x 1	1MB x 1
	4MB x 4	1MB x 1	
	4MB x 4		1MB x 1
18MB	256KB x 4	1MB x 1	16MB x 1
	256KB x 4	16MB x 1	1MB x 1
	4MB x 4	1MB x 1	1MB x 1
20MB	1MB x 4	16MB x 1	
	1MB x 4		16MB x 1
	4MB x 4	4MB x 1	
	4MB x 4		4MB x 1
		4MB x 1	16MB x 1
		16MB x 1	4MB x 1

Table 3-1. DRAM Configurations (Continued)

TOTAL MEMORY	BANK 0 (30-PIN)	BANK 1 (72-PIN)	BANK 2 (72-PIN)
21MB	256KB x 4	4MB x 1	16MB x 1
	256KB x 4	16MB x 1	4MB x 1
	1MB x 4	1MB x 1	16MB x 1
	1MB x 4	16MB x 1	1MB x 1
	4MB x 4	1MB x 1	4MB x 1
	4MB x 4	4MB x 1	1MB x 1
24MB	1MB x 4	4MB x 1	16MB x 1
	1MB x 4	16MB x 1	4MB x 1
	4MB x 4	4MB x 1	4MB x 1
32MB	4MB x 4	16MB x 1	
	4MB x 4		16MB x 1
		16MB x 1	16MB x 1
		32MB x 1 *	
			32MB x 1 *
33MB	256KB x 4	16MB x 1	16MB x 1
	4MB x 4	1MB x 1	16MB x 1
	4MB x 4	16MB x 1	1MB x 1
36MB	1MB x 4	16MB x 1	16MB x 1
	4MB x 4	4MB x 1	16MB x 1
	4MB x 4	16MB x 1	4MB x 1
48MB	4MB x 4	16MB x 1	16MB x 1
64MB	16MB x 4		
65MB	16MB x 4	1MB x 1	
	16MB x 4		1MB x 1
66MB	16MB x 4	1MB x 1	1MB x 1
68MB	16MB x 4	4MB x 1	
	16MB x 4		4MB x 1
69MB	16MB x 4	1MB x 1	4MB x 1
	16MB x 4	4MB x 1	1MB x 1
72MB	16MB x 4	4MB x 1	4MB x 1

* Double-RAS SIMM

Table 3-1. DRAM Configurations (Continued)

TOTAL MEMORY	BANK 0 (30-PIN)	BANK 1 (72-PIN)	BANK 2 (72-PIN)
80MB	16MB x 4	16MB x 1	
	16MB x 4		16MB x 1
81MB	16MB x 4	1MB x 1	16MB x 1
	16MB x 4	16MB x 1	1MB x 1
84MB	16MB x 4	4MB x 1	16MB x 1
	16MB x 4	16MB x 1	4MB x 1
96MB	16MB x 4	16MB x 1	16MB x 1

Table 3-1. DRAM Configurations

→ **NOTE : When using double-RAS SIMMs, it is advised that Bank 2 be used instead of Bank 1 and both cannot contain double-RAS SIMM at the same time. If Bank 1 contains a double-RAS SIMM, then Bank 0 (30-pin) is rendered inoperative.**

Installation Instructions

→ **NOTE : Always observe static electricity precautions. See "Handling Precautions" at the start of this manual.**

1. Locate the SIMM banks on the mainboard. Determine your desired configuration to be installed.
2. Insert the SIMM edge connector at a 90-degree angle onto the socket.

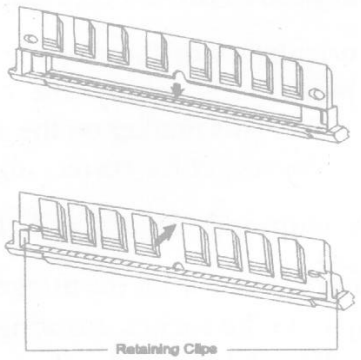

Figure 3-2. Installing SIMMs

3. Carefully push the SIMM down and back into the socket until the retaining clips of the socket snap, holding the SIMM in place. The holes in the SIMM should match the pins on the socket's retaining clips.

To remove the SIMM/s, pull the retaining latch on both ends of the socket and reverse the procedure above.

Cache Memory

The 486-VIP can accept cache memory of 64, 128 or 256KB.

→ **NOTE : Be sure to use the correct chips for the amount of cache memory you want to add. You must install both the correct Cache and Tag SRAM.**
Alter RAM type is always the same as Tag RAM.

Installing Cache Memory

→ **NOTE : Always observe static electricity precautions. See "Handling Precautions" at the beginning of this manual.**

If you do not have the confidence to make the installation, better consult a service technician for assistance.

1. Locate the cache memory on the mainboard. See Figure 3-1 again.

2. Be guided by the Cache SRAM settings depending on your desired SRAM configuration.

Correct orientation of the chips is necessary for the cache to operate properly. Normally, the chips have either a curved notch or a dot. This marker on the chip must be matched to the marker on the socket for correct alignment.

Install the chips individually as follows:

3. Align the chip with the marker on the socket. Press the chip onto the socket, ensuring that the pins on the chip are aligned with the corresponding connections on the socket.

4. Carefully apply enough pressure to partially seat the chip into the socket.

Ensure that all pins are properly aligned with the connectors and that there are no bent pins. If there are any bent pins, remove the chip, straighten the pin and repeat the process.

5. Press the chip completely into the socket so that the pins are properly seated.

The cache size is jumper selectable. M1 - M4 are assigned as Bank 0 and M6 - M9 are assigned as Bank 1.

	64K	128K	256K
Bank 0	8K x 8	32K x 8	32K x 8
Bank 1	8K x 8	empty	32K x 8
Tag RAM (M5)	8K x 8	8K x 8	32K x 8
JS1 (Jumper)	1-2	1-2	2-3
JS2 (Jumper)	1-2	2-3	2-3
JS3 (Jumper)	1-2	2-3	1-2

Table 3-2. Cache Configuration Size