CPU Clock Jumper JK1-JK4 (VT8225N)

CLK 2	JK1	JK2	JK3	JK4
100 MHz	1-2	2-3	1-2	2-3
80 MHz	1-2	1-2	2-3	2-3
66.6 MHz	2-3	2-3	1-2	2-3
50 MHz	2-3	1-2	2-3	2-8
40 MHz	1-2	1-2	2-3	1-2
33.3 MHz	2-3	2-3	1-2	1-2
25 MHz	2-3	1-2	2-3	1-2

Table 2-3. CPU Clock Jumper Selection JK1-JK4 (VT8225N)

Connectors

The connectors allow the mainboard to connect electronically with other parts of the system. Some connectors have two pins, others have four or five pins. Some malfunction problems encountered with your system may be caused by loose or improper connections. Ensure that all connections are in place and firmly attached.

CONNECTOR	PIN OUTS	SIGNAL NAME
J1 Turbo Switch	1 2	Turbo Signal Ground
J3 * Green Power Supply Connector	1 2	Enable/Disable power supply outlet Ground
J4 External Battery Connector	1 2, 3 4	Anode+ NC Cathode –
J8 Turbo LED	1 2	VCC LED
J9 Hardware Reset	1 2	Ground Reset signal
J10 Speaker Connector	1 2 3 4	Speaker signal NC Ground +5V
J11 Keylock and Power LED Connector	1 2 3, 5 4	Power signal Spare Ground Keylock
CN1 PS/2 Keyboard Connector	1 2, 6 3 4 5	Keyboard data NC Ground +5V Keyboard clock
CN2 PS/2 Mouse Connector	1 2, 6 3 4 5	Mouse data NC Ground +5V Mouse clock
CN3 Keyboard Connector	1 2 3 4 5	Keyboard clock Keyboard data NC Ground +5V
CN4 Mouse Connector	1 2 3 4 5	Mouse data NC Ground +5V Mouse clock
CN5 Power Connector	1 2, 10, 11, 12 3 4 5, 6, 7, 8 9	Power good +5V +12V –12V Ground –5V

Table 2-4. Connector Pin Definitions

JUMPER	486SX/P23S* (PGA)	P24S*/P4S*/ 486DX/DX2 (PGA)	P24T* (PGA)	Cx486S (M6) (PGA)	Cx486DX (M7) Cx486S+ Cx487S (M6+C6) (PGA)
JC1	2-3 shorted	1-2 shorted	1-2 shorted	2-3 shorted	1-2 shorted
JC2	2-3 shorted	1-2 shorted	1-2 shorted	2-3 shorted	1-2 shorted
JC3	open	shorted	open	shorted	shorted
JC4	open	open	shorted	open	open
JC5	shorted	shorted	open	open	open
JC7	1-2 shorted	1-2 shorted	2-3 shorted	1-2 shorted	1-2 shorted

* P23S, P24S, and P4S are the SL-enhanced CPUs while P24T is the Pentium Overdrive Processor.

JUMPER (RP 0Ω 10p5R)	P23S/P4S/P24S (PGA)	486DX/DX2/SX (PGA)	Cx486S Cx486S+Cx487S Cx486DX (M6, M6+C6, M7) (PGA)	P23S/P4S/Cx486S (PQFP)
RN13	inserted	empty	empty	empty
RN14	empty	empty	empty	inserted
RN16	empty	empty	inserted	empty

JUMPER	PIN DEFINITION
JC6	80486SX/P23S/P4S/Cx486S PQFP Select Short Disable Open Enable
JCX1	Short Cyrix Cx486S/DX Open Intel S-series CPU, others (default)
JCX2	1-2 Intel S-series CPU, others (default) 2-3 Cyrix Cx486S/DX
JX2, JP2	1-2 * IRQ15 (Regular CPUs -- default) 2-3 – SMI (Cyrix or Intel S-series CPUs)

* IRQ15 is no longer available for the other devices when SMI is selected.

Table 2-1. Jumper Settings for CPU Selector

JUMPER	PIN DEFINITION
J2	Display Type Select Open Mono/EGA/VGA (default) Short Color
J5	External, Internal Battery Select 1-2 External battery 2-3 Internal battery (default)
J6	Short Adaptec ISA Master 1542B/C SCSI card only (Transfer rate ≥ 5.7MB/s) Open Default (Transfer rate < 5.7MB/s)
J7	Password Clear (Award/AMI BIOS Select) Short Clear password Open (default)
J12	Cyrix CPU 2 X Clock Mode Select 1-2 2 X 2-3 1 X (default)
JP1 JP5	JP1 JP5 1-2 1-2 (factory default)
JP4	Local IDE 1-2 Default 2-3 For VESA Local VGA Card installed at VESA slot 0 only
JT1	P24T Write-back/Write-through Select 1-2 Write-back 2-3 Write-through
JX1	Regular CPU Clock Select 1-2 1 X (default) 2-3 2 X

Table 2-2. Jumper Definitions

NOTE : Users are not encouraged to change the jumper settings not listed in this manual as they are considered factory defaults which may adversely affect system performance.

- Dallas DS1287/DS12885Q/VIA VT82885V real time clock/calendar.
- Provides built-in power management features ideal for Green PCs.

Mainboard Layout

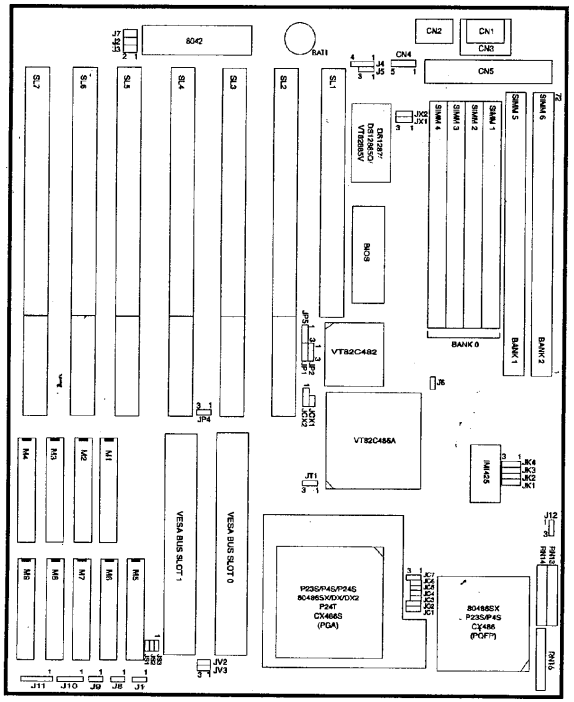

Figure 1-1. Mainboard Layout

* Insert two pin connector wire from Green Power Supply into Connector J3.

VESA Bus Connector

The cache system board provides two high-performance VESA bus connectors, SL14 and SL15, for use with VESA peripherals. These connectors can be utilized for one Local Bus Master and one Local Bus Slave, either (SL14) or (SL15).

The following tables give the pin assignments for SL14 and SL15. Side A of the connector are pin outs on the board's component side while Side B are pin outs on the board's solder side. Jumpers JV2 and JV3 give more information on settings on the mainboard and the VL-bus controller.

JUMPER	PIN DEFINITION
JV2	CPU Speed Select 1-2 > 33 MHz 2-3 ≤ 33 MHz
JV3	High Speed Write Select 1-2 One wait write 2-3 Zero wait write (default)

→ **NOTE : The two VESA Local Bus slot can accommodate either one VESA Master with one VESA Slave or two VESA Slaves.**

CONNECTOR	SIDE A - PINS AND PIN OUTS		SIDE B - PINS AND PIN OUTS	
SL15 — Local Bus Connector	01	DAT01	01	DAT00
	02	DAT03	02	DAT02
	03, 10, 17, 24, 35, 43, 51	Ground	03	DAT04
	04	DAT05	04	DAT06
	05	DAT07	05	DAT08
	06	DAT09	06, 14, 22, 29, 38, 49, 55	Ground
	07	DAT11	07	DAT10
	08	DAT13	08	DAT12
	09	DAT15	09, 20, 32, 57	VCC
	11	DAT17	10	DAT14
	12, 27, 40, 53	VCC	11	DAT16
	13	DAT19	12	DAT18
	14	DAT21	13	DAT20
	15	DAT23	15	DAT22
	16	DAT25	16	DAT24
	18	DAT27	17	DAT26
	19	DAT29	18	DAT28
	20	DAT31	19	DAT30
	21	ADR30	21	ADR31
	22	ADR28	23	ADR29
	23	ADR26	24	ADR27
	25	ADR24	25	ADR25
	26	ADR22	26	ADR23
	28	ADR20	27	ADR21
	29	ADR18	28	ADR19
	30	ADR16	30	ADR17
	31	ADR14	31	ADR15
	32	ADR12	33	ADR13
	33	ADR10	34	ADR11
	34	ADR08	35	ADR09
	36	ADR06	36	ADR07
	37	ADR04	37	ADR05
	38	WBACK#	39	ADR03
	39	BE0#	40	ADR02
	41	BE1#	41	NC
	42	BE2#	42	RESET#
	44	BE3#	43	D/C#
	45	ADS#	44	M/IO#
	48	LRDY#	45	W/R#
	49	LDEV0#	48	RDYRTN#
	50	LREQ#	50	IRQ9
	52	LGNT#	51	BRDY#
	54, 55, 56	ID2, 3, 4	52	BLAST#
	57	LKEN#	53, 54	ID0, 1
	58	LEADS#	56	LCLK0
			58	LBS16#

Table 2-5. Local Bus Connector Pin Assignment (Continued)

CONNECTOR	SIDE A - PINS AND PIN OUTS		SIDE B - PINS AND PIN OUTS	
SL14 — Local Bus Connector	01	DAT01	01	DAT00
	02	DAT03	02	DAT02
	03, 10, 17, 24, 35, 43, 51	Ground	03	DAT04
	04	DAT05	04	DAT06
	05	DAT07	05	DAT08
	06	DAT09	06, 14, 22, 29, 38, 49, 55	Ground
	07	DAT11	07	DAT10
	08	DAT13	08	DAT12
	09	DAT15	09, 20, 32, 57	VCC
	11	DAT17	10	DAT14
	12, 27, 40, 53	VCC	11	DAT16
	13	DAT19	12	DAT18
	14	DAT21	13	DAT20
	15	DAT23	15	DAT22
	16	DAT25	16	DAT24
	18	DAT27	17	DAT26
	19	DAT29	18	DAT28
	20	DAT31	19	DAT30
	21	ADR30	21	ADR31
	22	ADR28	23	ADR29
	23	ADR26	24	ADR27
	25	ADR24	25	ADR25
	26	ADR22	26	ADR23
	28	ADR20	27	ADR21
	29	ADR18	28	ADR19
	30	ADR16	30	ADR17
	31	ADR14	31	ADR15
	32	ADR12	33	ADR13
	33	ADR10	34	ADR11
	34	ADR08	35	ADR09
	36	ADR06	36	ADR07
	37	ADR04	37	ADR05
	38	WBACK#	39	ADR03
	39	BE0#	40	ADR02
	41	BE1#	41	NC
	42	BE2#	42	RESET#
	44	BE3#	43	D/C#
	45	ADS#	44	M/IO#
	48	LRDY#	45	W/R#
	49	LDEV1#	48	RDYRTN#
	50	LREQ#	50	IRQ9
	52	LGNT#	51	BRDY#
	54, 55, 56	ID2, 3, 4	52	BLAST#
	57	LKEN#	53, 54	ID0, 1
	58	LEADS#	56	LCLK1
			58	LBS16#

Table 2-5. Local Bus Connector Pin Assignment

Memory Subsystem

The 486-GVT-2 is equipped with the memory necessary for running all your applications. Memory comes in the form of DRAM (SIMMs) and cache SRAM. This chapter describes these two kinds of memory and gives instructions on how to install each kind on the mainboard.

Memory Locations

The board layout below shows the locations of the DRAM memory banks and the cache SRAM:

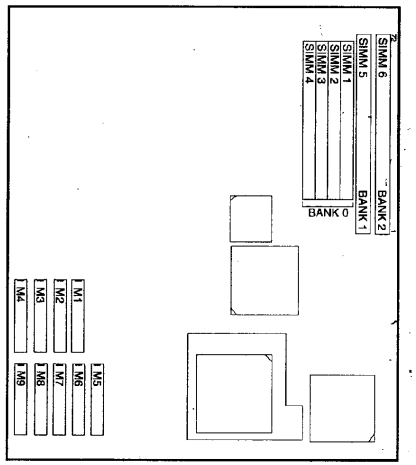

Figure 3-1. Cache and Memory Locations

Here under are the jumper setting for Intel Pentium overdrive 83Mhz on GVT-2 M/B.

JC1 ------ 1-2
JC2 ------ 1-2
JC3 ------ open
JC4 ------ short
JC5 ------ open
JC6 ------ short
JC7 ------ 2-3

JK1 ------ 2-3
JK2 ------ 2-3
JK3 ------ 1-2
JK4 ------ 1-2

RN Configuration --> RN13 ---- ON (Resistor Inserted)

Other jumpers
JCX1 -------- open
JCX2 -------- 1-2
JX2 --------- 2-3
JP2 --------- 2-3
J12 --------- Open

Note: Please use the latest BIOS for GVT-2 Motherboard.

FIC Technical Support
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