Mainboard Layout

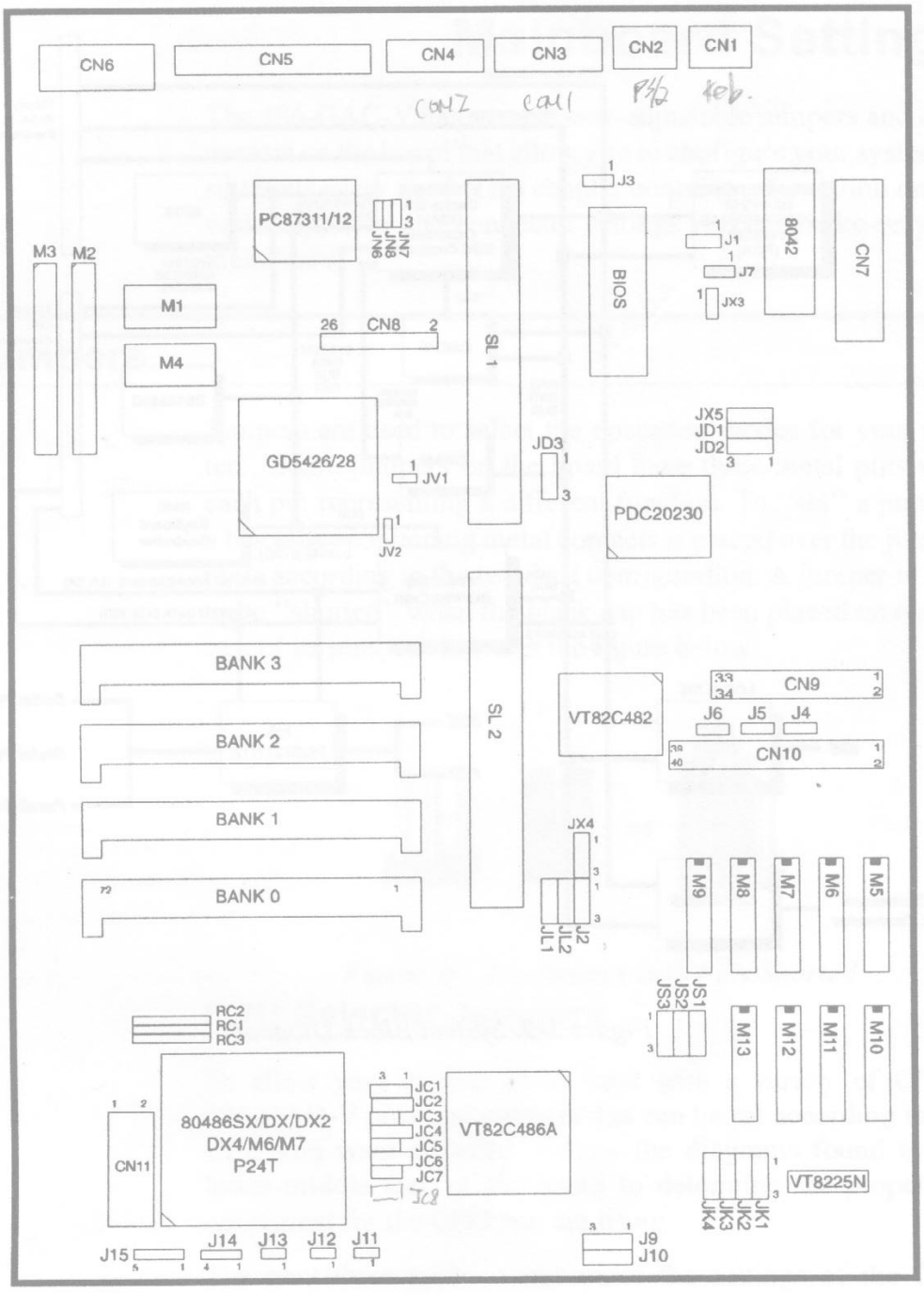


Figure 1-1. Mainboard Layout

Mainboard Settings

The 486-GAC-V has several user-adjustable jumpers and connectors on the board that allow you to configure your system to suit your every need. This chapter contains information on the various jumper and connector settings you can make on your mainboard.

Jumpers

Jumpers are used to select the operation modes for your system. Some jumpers on the board have three metal pins with each pin representing a different function. To "set" a jumper, a black cap containing metal contacts is placed over the jumper pin/s according to the required configuration. A jumper is said to be "shorted" when the black cap has been placed on one or two of its pins, as shown in the figure below:

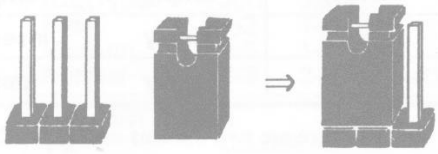


Figure 2 - 1 Jumper with Pins Shorted

CPU Selector Jumpers

To allow your system to be used with a variety of CPUs, 486-GAC-V provides jumpers that can be set according to the CPU you want installed. Follow the diagrams found in the lower-middle area of the board to determine the proper arrangement for the CPU you are using.

The next three tables summarizes the settings of the CPU Selector jumpers:

JUMPER	486SX/P23S*/ Cx486S (M6) (PGA)	Am486DXL P24S*/P4S*/ 486DX/ IntelDX2™/ IntelDX4™/ Cx486DX (M7)/ Cx486S+Cx487S (M6+C6) (PGA)	P24T*/P24CT (PGA)	P24D* (PGA)
JC1	2-3	1-2	1-2	1-2
JC2	2-3	1-2	1-2	1-2
JC3	open	open	short	open
JC4	1-2	1-2	2-3	2-3

* P23S, P24S, P24D, and P4S are the SL-enhanced CPUs while P24T is the Overdrive Processor.

→ **#NOTE : When the onboard 3.3 volt regulator is not present, the 3.3 volt daughter board should be installed. If not, please refer to page 2-12 installation of the 3.3 volt regulator daughter board.**

JUMPER (RP 0Ω 8P4R)	486SX/DX/ IntelDX2™	P23S/P4S/ P24S	Cx486S/DX	P24D/ IntelDX4™/ P24CT	Am486DXL
JC5	open	short	open	short	open
RC1	empty	empty	empty	inserted	empty
RC2	empty	empty	inserted	empty	empty
RC3*	empty	empty	empty	empty	inserted

*There are two options of VIA 82C486A on RC3 : 1235 and 1272. If 1235 is selected, RC3 performs its function. If 1272 is chosen, RC3 will not work.

JUMPER	PIN DEFINITION
J2, J10, JX5	1-2 Regular CPU 2-3 SL-enhanced CPU
JC6	IntelDX4™ Internal Clock Select Open Internal 3 X (default) 1-2 Internal 2.5 X 2-3 Internal 2 X
JC7	P24T Write-back/Write-through Select Short Write-back Open Write-through
JX3	1-2 Intel SL-enhanced CPU 2-3 Cyrix CPU, AMD

JX4	Open 1-2 2-3	Regular CPU Intel SL-enhanced CPU Cyrix CPU, AMD
JC8	Open Short	For Cyrix CPU Other CPU

Table 2-1. Jumper Settings for CPU Selector

JUMPER	PIN DEFINITION
J1	I/O Channel Ready Select Short — Adaptec ISA Master 1542B/C SCSI card only (Transfer rate ≥ 5.7MB/s) Open — Default (Transfer rate < 5.7MB/s)
J7	Password Clear Short — Clear password Open — (default)
J4	HDD_BALE Short — Enable Open — Disable (default)
J5	HDD_IOCHRDY Short — Enable Open — Disable (default)
J9	1-2 — (factory default)
JD1, JD2	HDD Speed Select (PDC 20230 Only) IDE Type — JD1 — JD2 Fast — 1-2 — 1-2 Medium — 2-3 — 1-2 Normal — 2-3 — 2-3 (default)
JD3	Local IDE Select 1-2 — Disable 2-3 — Enable (default)
JN6	NS87312 I/O Port Address Select 1-2 — Index port = 26Eh, data port = 26Fh (default) 2-3 — Index port = 398h, data port = 399h
JN7, JN8	Printer Port Direction Select Direction — JN7 — JN8 Output only — 1-2 — 2-3 (default) Input only — 1-2 — 1-2 Bi-directional — 2-3 — 1-2, 2-3

Table 2-2. Jumper Definitions

JUMPER	PIN DEFINITION
JV1	IRQ_9 On/Off Select Short Enable Open Disable (default)
JV2	Onboard VGA On/Off Select 1-2 Disable 2-3 Enable (default)

Table 2-3. Video Jumper Definitions

CPU Clock Jumper JK1-JK4 (VT8225N)

CLK	JK1	JK2	JK3	JK4
50 MHz	2-3	1-2	2-3	2-3
40 MHz	1-2	1-2	2-3	1-2
33.3 MHz	2-3	2-3	1-2	1-2
25 MHz	2-3	1-2	2-3	1-2

Table 2-4. CPU Clock Jumper Selection JK1-JK4 (VT8225N)

Connectors

The connectors allow the mainboard to connect electronically with other parts of the system. Some connectors have two pins, others have four or five pins. Some malfunction problems encountered with your system may be caused by loose or improper connections. Ensure that all connections are in place and firmly attached.

CONNECTOR	PIN OUTS	SIGNAL NAME
J3 * Green Power Supply Connector	1 2	Enable/Disable power supply outlet Ground
J6 HDD_LED Connector	1 2	LED – LED +
J11 Turbo Switch Connector	1 2	Ground Turbo Signal
J12 Turbo LED Connector	1 2	LED – LED +

J13 Reset Switch Connector	1 2	Ground Reset signal
J14 Speaker Connector	1 2 3 4	Speaker signal NC Ground +5V
J15 Keylock and Power LED Connector	1, 2 3, 5 4	Power LED Ground Keyboard clock
CN1 PS/2 Keyboard Connector	1 2, 6 3 4 5	Keyboard data NC Ground +5V Keyboard clock
CN2 PS/2 Mouse Connector	1 2 3, 6 4 5	Mouse data NC Ground +5V Mouse clock
CN3, CN4 Serial Port 1, 2 Connector	1 2 3 4 5 6 7 8 9	Data carrier detect Receive data Transmit data Data transmit ready Signal ground Ready to receive data Request to send data Clear to send Ring indicator
CN6 VGA Connector	1 2 3 4, 9, 11, 12, 15 5-8, 10 13 14	Red Green Blue NC Ground Horizontal sync Vertical sync
CN7 Power Connector	1* 2, 10, 11, 12 3 4 5, 6, 7, 8 9	Power good +5V +12V –12V Ground –5V

* Insert two pin connector wire from Green Power Supply into Connector J3.

Table 2-5. Connector Pin Definitions (Continued)

CONNECTOR	PIN OUTS	SIGNAL NAME
CN5 Parallel Port Connector	1	LPT strobe
	2	Data bit 0
	3	Data bit 1
	4	Data bit 2
	5	Data bit 3
	6	Data bit 4
	7	Data bit 5
	8	Data bit 6
	9	Data bit 7
	10	LPT acknowledge
	11	LPT busy
	12	Paper end
	13	Selected status
	14	Auto line feed
	15	LPT error
	16	Initiate printer
	17	Select printer
	18-25	Ground
CN8 8514A Connector	1	VP0
	2, 4, 6, 16, 18, 20, 22, 25	Ground
	3	VP1
	5	VP2
	7	VP3
	8	Enable video data
	9	VP4
	10	Enable sync signal
	11	VP5
	12	Enable video dot clock
	13	VP6
	14, 24, 26	NC
	15	VP7
	17	Video dot clock
	19	Blanking
	21	Horizontal sync
	23	Vertical sync
CN11 3.3V Daughter Board Connector	1, 3, 14, 16	+ 3V
	2, 4, 13, 15	VCC
	5, 12	Voltage switch
	6, 11	+ 12V
	7, 8, 9, 10	Ground

Table 2-5. Connector Pin Definitions (Continued)

CONNECTOR	PIN OUTS	SIGNAL NAME
CN9 FDD Connector	2	Density selection
	4, 6	NC
	8	Index detection
	10	Select motor A
	12	Select drive A
	14	Select drive B
	16	Select motor B
	18	Direction control
	20	Step pulse
	22	Write data
	24	Write enable
	26	Track 0
	28	Write protect
	30	Read data
	32	Head select
	34	Disk change
	1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 31, 33	Ground

Table 2-5. Connector Pin Definitions (Continued)

→ **NOTE : Users are not encouraged to change the jumper settings not listed in this manual as they are considered factory defaults which may adversely affect system performance.**

CONNECTOR	PIN OUTS	SIGNAL NAME
CN10 HDD IDE Connector	1	Reset hard disk
	2, 19, 22, 24, 26, 30, 40	Ground
	3	HDD7
	4	HDD8
	5	HDD6
	6	HDD9
	7	HDD5
	8	HDD10
	9	HDD4
	10	HDD11
	11	HDD3
	12	HDD12
	13	HDD2
	14	HDD13
	15	HDD1
	16	HDD14
	17	HDD0
	18	HDD15
	20, 21, 29, 34	NC
	23	HDD I/O write
	25	HDD I/O read
	27	IOCHRDY
	28	HDD address latch
	31	IRQ14
	32	IOCS16
	33	HDD A1
	35	HDD A0
	36	HDD A2
	37	HDD chip select 0
	38	HDD chip select 1
	39	HDD active

Table 2-5. Connector Pin Definitions

ISA/VESA Bus Connector

The mainboard provides one high-performance ISA/VESA bus connectors, SL1 and SL2, for use with ISA/VESA peripherals. The VESA bus connector can be utilized for one Local Bus Master or one Local Bus Slave (SL2).

The following tables give the pin assignments for SL1 and SL2. Side A of the connector are pin outs on the board's component side while Side B are pin outs on the board's solder side. Jumpers JL1 and JL2 give more information on settings on the mainboard and the VL-bus controller.

JUMPER	PIN DEFINITION
JL1	High Speed Write Select 1-2 Zero wait write (default) 2-3 One wait write
JL2	CPU Speed Select 1-2 ≤ 33MHz (default) 2-3 > 33MHz

CONNECTOR	SIDE A - PINS AND PIN OUTS		SIDE B - PINS AND PIN OUTS	
SL1 ISA Bus Slot	01	+12V	01	+12V
	02, 03	Ground	02	+5V
	04	IOCHCK#	03, 04	Ground
	05	SD7	05	RES_DRV
	06	SD6	06	+5V
	07	SD5	07	IRQ9
	08	SD4	08	–5V
	09	SD3	09	DREQ2
	10	SD2	10	–12V
	11	SD1	11	0WS#
	12	SD0	12	+12V
	13	IOCHRDY	13	Ground
	14	AEN	14	SMEMW#
	15	LA19	15	SMEMR#
	16	LA18	16	IOW#
	17	LA17	17	IOR#
	18	LA16	18	DACK3#
	19	SA15	19	DREQ3
	20	SA14	20	DACK1#
	21	SA13	21	DREQ1
	22	SA12	22	REFRESH#
	23	SA11	23	SYS_CLK
	24	SA10	24	IRQ7
	25	SA9	25	IRQ6
	26	SA8	26	IRQ5
	27	SA7	27	IRQ4
	28	SA6	28	IRQ3
	29	SA5	29	DACK2#
	30	SA4	30	TC
	31	SA3	31	BALE
	32	SA2	32	+5V
	33	SA1	33	OSC
	34	SA0	34, 35	Ground
	35, 36	Ground	36	– LDEV1
	37, 38	+5V	37	+5V
	39	SBHE#	38	+5V
	40	LA23	39	MEMCS16#
	41	LA22	40	IOCS16#
	42	LA21	41	IRQ10
	43	LA20	42	IRQ11
	44	LA19	43	IRQ12
	45	LA18	44	IRQ13
	48	LA17	45	IRQ14
	49	MEMR#	48	DACK0#
	50	MEMW#	49	DREQ0
	51	SD8	50	DACK5#
	52	SD9	51	DREQ5
	53	SD10	52	DACK6#
	54	SD11	53	DREQ6
	55	SD12	54	DACK7#
	56	SD13	55	DREQ7
	57	SD14	56	+5V
	58	SD15	57	MASTER#
			58	Ground

CONNECTOR	SIDE A - PINS AND PIN OUTS		SIDE B - PINS AND PIN OUTS	
SL2 VESA Slot	01	DAT01	01	DAT00
	02	DAT03	02	DAT02
	03	Ground	03	DAT04
	04	DAT05	04	DAT06
	05	DAT07	05	DAT08
	06	DAT09	06	Ground
	07	DAT11	07	DAT10
	08	DAT13	08	DAT12
	09	DAT15	09	VCC
	10	Ground	10	DAT14
	11	DAT17	11	DAT16
	12	VCC	12	DAT18
	13	DAT19	13	DAT20
	14	DAT21	14	Ground
	15	DAT23	15	DAT22
	16	DAT25	16	DAT24
	17	Ground	17	DAT26
	18	DAT27	18	DAT28
	19	DAT29	19	DAT30
	20	DAT31	20	VCC
	21	ADR30	21	ADR31
	22	ADR28	22	Ground
	23	ADR26	23	ADR29
	24	Ground	24	ADR27
	25	ADR24	25	ADR25
	26	ADR22	26	ADR23
	27	VCC	27	ADR21
	28	ADR20	28	ADR19
	29	ADR18	29	Ground
	30	ADR16	30	ADR17
	31	ADR14	31	ADR15
	32	ADR12	32	VCC
	33	ADR10	33	ADR13
	34	ADR08	34	ADR11
	35	Ground	35	ADR09
	36	ADR06	36	ADR07
	37	ADR04	37	ADR05
	38	WBACK#	38	Ground
	39	BE0#	39	ADR03
	40	VCC	40	ARD02
	41	BE1#	41	NC
	42	BE2#	42	RESET#
	43	Ground	43	D/C#
	44	BE3#	44	M/IO#
	45	ADS#	45	W/R#
	48	LRDY#	48	RDYRTN#
	49	LDEV0#	49	Ground
	50	LREQ0#	50	IRQ9
	51	Ground	51	BRDY#
	52	LGNT0#	52	BLAST#
	53	VCC	53	ID0
	54	ID2	54	ID1
	55	ID3	55	Ground
	56	ID4	56	LCLK
	57	LKEN#	57	VCC
	58	LEADS#	58	LBS16#

3.3 Volt regulator board installation

This section describes the installation of the 3.3 volt regulator board used for the IntelDX4 CPU.

The IntelDX4 CPU is a new member of the Intel 486 processor family based on the Intel 486DX2 microprocessor core. It offers features such as System management mode (SMM) and stop Clock Mode ideal for power managememt function. It's internal core frequency can operate to maximum of 100MHZ. It also operates with a 3.3 volt (Vcc) supply.

If the on board 3.3 volt regulator is not present, the 3.3 volt regulator must be installed before using the InterDX4 CPU. Please also refer to the steps below on how to install the 3.3 volt regulator.

Please also refer to page 2-2 for the correct CPU jumper selection.

1. Remove jumpers from connector PS3V.
2. Please the 3.3 volt regulator board as shown on the figure below with the correct pin orientation.

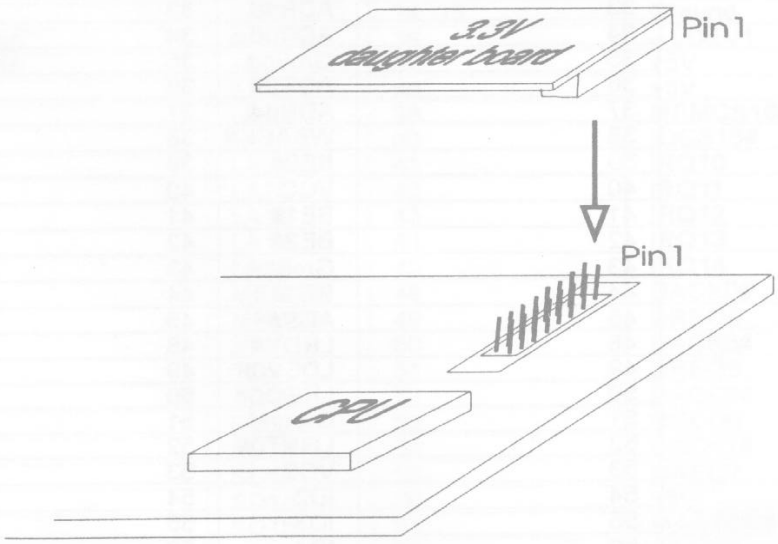


Figure 2 - 2. 3.3 volt regulator board installation

Memory Subsystem

The 486-GAC-V is equipped with the memory necessary for running all your applications. Memory comes in the form of DRAM (SIMMs) and cache SRAM. This chapter describes these two kinds of memory and gives instructions on how to install each kind on the mainboard.

Memory Locations

The board layout below shows the locations of the DRAM memory banks and the cache SRAM:

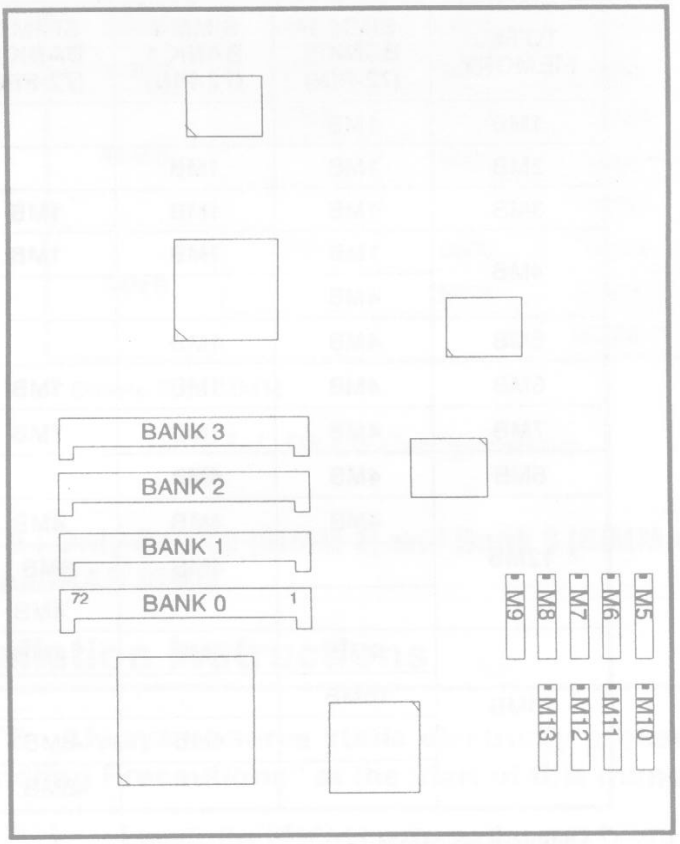


Figure 3-1. Cache and Memory Locations

Installing DRAM

SIMM Banks

The 486-GAC-V can accommodate on-board memory from 1 to 64MB using SIMMs (Single-In-Line Memory Modules). The mainboard has four memory banks — Bank 0, 1, 2, 3. Each bank can accept either a lMB, 4MB, or 16MB SIMM in each socket.

DRAM Configuration

Memory can be installed in a variety of configurations, as shown in the next table:

TOTAL MEMORY	SIMM 1 BANK 0 (72-PIN)	SIMM 2 BANK 1 (72-PIN)	SIMM 3 BANK 2 (72-PIN)	SIMM 4 BANK 3 (72-PIN)
1MB	1MB			
2MB	1MB	1MB		
3MB	1MB	1MB	1MB	
4MB	1MB	1MB	1MB	1MB
	4MB			
5MB	4MB	1MB		
6MB	4MB	1MB	1MB	
7MB	4MB	1MB	1MB	1MB
8MB	4MB	4MB		
12MB	4MB	4MB	4MB	
		4MB	8MB *	
			4MB	8MB *
16MB	4MB	4MB	4MB	4MB
	16MB			
		4MB	8MB *	4MB
			8MB *	8MB *

* Double-RAS SIMM

Table 3-1. DRAM Configurations (Continued)

TOTAL MEMORY	SIMM 1 BANK 0 (72-PIN)	SIMM 2 BANK 1 (72-PIN)	SIMM 3 BANK 2 (72-PIN)	SIMM 4 BANK 3 (72-PIN)
17MB	16MB	1MB		
18MB	16MB	1MB	1MB	
19MB	16MB	1MB	1MB	1MB
20MB	16MB	4MB		
21MB	16MB	4MB	1MB	
22MB	16MB	4MB	1MB	1MB
24MB	16MB	4MB	4MB	
28MB	16MB	4MB	4MB	4MB
32MB	16MB	16MB		
			32MB *	
33MB	16MB	16MB	1MB	
34MB	16MB	16MB	1MB	1MB
36MB	16MB	16MB	4MB	
40MB	16MB	16MB	4MB	4MB
48MB	16MB	16MB	16MB	
		16MB	32MB *	
			16MB	32MB *
64MB	16MB	16MB	16MB	16MB
		16MB	32MB *	16MB
			32MB *	32MB *

* Double-RAS SIMM

Table 3-1. DRAM Configurations

→ **NOTE : Only Bank 2 (SIMM 3) and Bank 3 (SIMM 4) supports Double-RAS SIMM.**

Installation Instructions

→ **NOTE : Always observe static electricity precautions. See "Handling Precautions" at the start of this manual.**

1. Locate the SIMM banks on the mainboard. Determine your desired configuration to be installed.

2. Insert the SIMM edge connector at a 75-degree angle onto the socket.

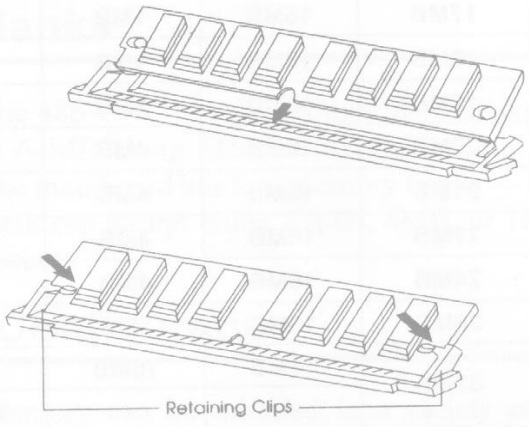


Figure 3-2. Installing SIMMs

3. Carefully push the SIMM down and back into the socket until the retaining clips of the socket snap, holding the SIMM in place. The holes in the SIMM should match the pins on the socket's retaining clips.

To remove the SIMM/s, pull the retaining latch on both ends of the socket and reverse the procedure above.

Cache Memory

The 486-GAC-V can accept cache memory of 64, 128 or 256KB.

→ **NOTE : Be sure to use the correct chips for the amount of cache memory you want to add. You must install both the correct Cache and Tag SRAM.**
Alter RAM type is always the same as Tag RAM.

Installing Cache Memory

→ **NOTE : Always observe static electricity precautions. See "Handling Precautions" at the beginning of this manual.**

If you do not have the confidence to make the installation, better consult a service technician for assistance.

1. Locate the cache memory on the mainboard. See Figure 3-1 again.
2. Be guided by the Cache SRAM settings depending on your desired SRAM configuration.

Correct orientation of the chips is necessary for the cache to operate properly. Normally, the chips have either a curved notch or a dot. This marker on the chip must be matched to the marker on the socket for correct alignment.

Install the chips individually as follows:

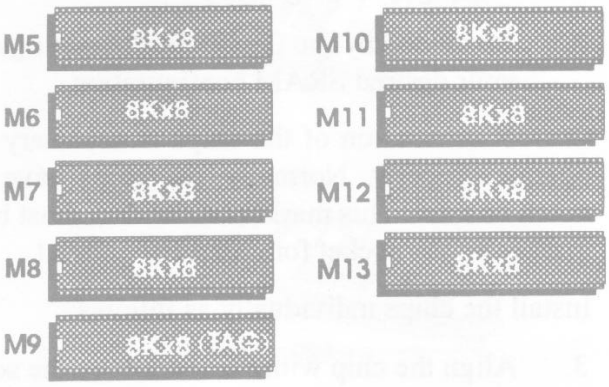
3. Align the chip with the marker on the socket. Press the chip onto the socket, ensuring that the pins on the chip are aligned with the corresponding connections on the socket.
4. Carefully apply enough pressure to partially seat the chip into the socket.

Ensure that all pins are properly aligned with the connectors and that there are no bent pins. If there are any bent pins, remove the chip, straighten the pin and repeat the process.

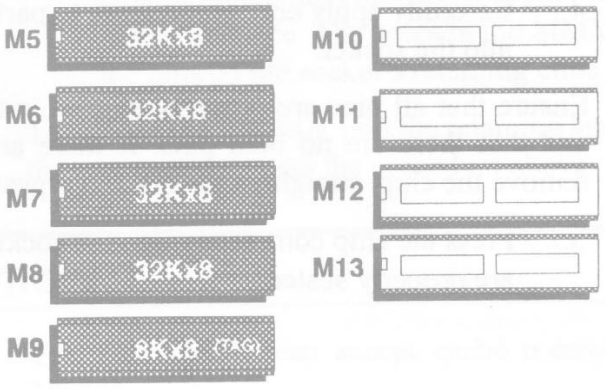
5. Press the chip completely into the socket so that the pins are properly seated.

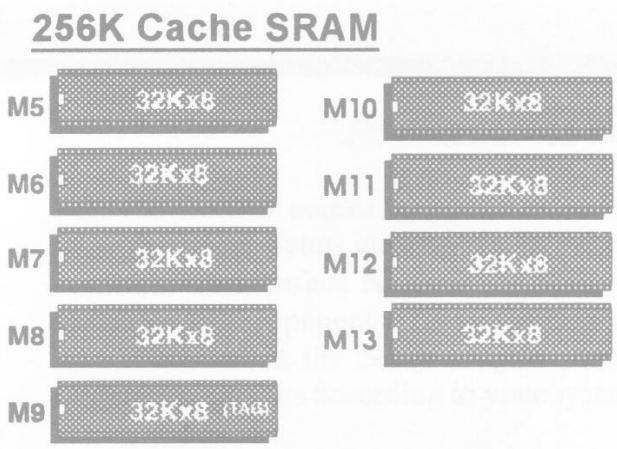
Cache SRAM Specifications and Settings

64K Cache SRAM



128K Cache SRAM





The cache size is jumper selectable. M5 - M9 are assigned as Bank 0 and M10 - M13 are assigned as Bank 1.

	64K	128K	256K
Bank 0	8K x 8	32K x 8	32K x 8
Bank 1	8K x 8	Empty	32K x 8
Tag RAM (M9)	8K x 8	8K x 8	32K x 8
JS1 (Jumper)	1-2	2-3	2-3
JS2 (Jumper)	2-3	1-2	2-3
JS3 (Jumper)	1-2	1-2	2-3

Table 3-2. Cache Configuration Size