Mitac MTC IH4077C

Processor: 80486SX/80486DX/80486DX2/P23N/Pentium Overdrive

Processor Speed: 25/33/40/50/50(internal)/66(internal)/80(internal) MHz

Chip Set: UMC UM82C491F Max. Onboard DRAM: 32MB Cache: 0/64/128/256KB

BIOS: Award

Dimensions: 254mm x 218mm (10" x 8.5")

I/O Options: 32-bit VESA local bus slots (2)

NPU Options: None

CONNECTIONS:

Purpose Location

Internal battery J1 (Close to enable onboard)

External battery J2
Reset switch J4
Power LED J5
Turbo switch J6
Keylock J7
Speaker J8

32-bit VESA local bus MCA1 & MCA2

USER CONFIGURABLE SETTINGS (* = Default)

Function	Jumper	Position
VESA Slot 1 and 2 (MCA1 + MCA2)	JP2	pins 1 & 2 closed*
VESA Only Slot1 (MCA1)	JP2	pins 2 & 3 closed
VL-BUS 1 Wait state	JP7	pins 1 & 2 closed*
VL-BUS 0 Wait state	JP7	pins 2 & 3 closed
Factory configured - do not alter	JP8	No jumpers*
PQFP CPU Disabled	JP17	Closed*
POFP CPU Enabled	JP17	Open

PQFP CPU Disabled JP17 Closed*
PQFP CPU Enabled JP17 Open
Factory configured - do not alter JP19 Closed*
Factory configured - do not alter JP20 Open*

DRAM CONFIGURATION

Size	Bank	0 2				Banl	ς 1		
4MB	(4)	1M	х	9		NON	S		
8MB	(4)	1M	х	9	`	(4)	1M	х	9
16MB	(4)	4M	х	9		NON	S		
32MB	(4)	4M	х	9		(4)	4M	x	9

CACHE CONFIGURATION

Size	Bank 0	Bank 1	TAG
64KB			
128KB	(4) 32K x 8	NONE	(1) 8K x 8
256KB	(4) 32K x 8	(4) 32K x 8	(1) 32K x 8

CACHE JUMPER CONFIGURATION (see Cache Note below)

Size	JP9	JP10	JP11	JP12
64K	1 & 2	Open	Open	Open
128K	2 & 3	2 & 3	Open	Close
256K	1 & 2	1 & 2	Close	Close

CPU TYPE CONFIGURATION

Type	JP14	JP15	
00406037	Onon		

80486SX Open pins 2 & 3 closed 80486DX 1 & 2 closed 1 & 2, 3 & 4 closed 80486DX2 1 & 2 closed 1 & 2, 3 & 4 closed P23N / T 2 & 3 closed 1 & 2, 3 & 4 closed

CPU SPEED CONFIGURATION

Clock	Speed	JP6	JP5	JP4
25MHz		Open	Open	Closed
33MHz		Closed	Closed	Open
40MHz		Open	Closed	Closed
50MHz		Closed	Open	Open

BUS SPEED CONFIGURATION

CPU speed JP16 <= 33MHz Open > 33MHz Closed

Cache Note: If No cache memory is installed and the Cache Size jumpers are set, the board will successfully boot reporting 0 cache.

