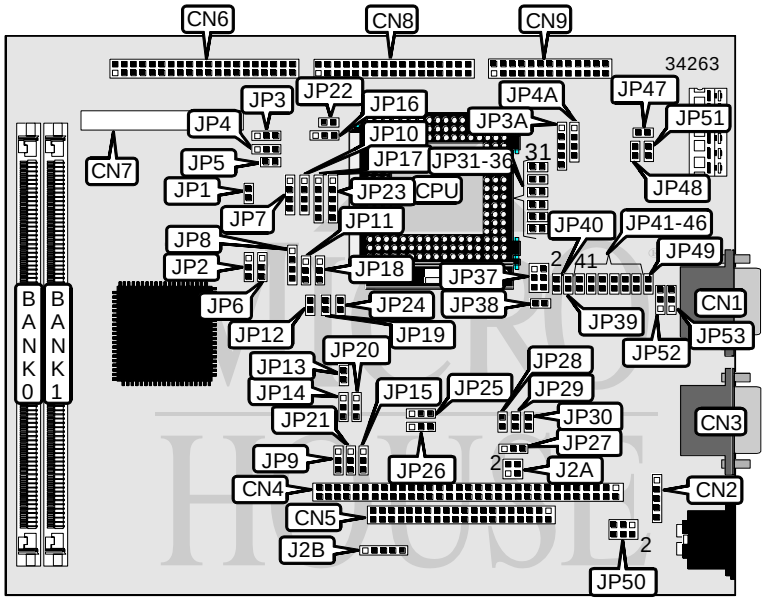
J & J TECHNOLOGY, INC
JJ.109 CPU BOARD

Processor	CXM6/80486SX/SL80486SX/CX486DX/AM486DXL/80486DX/ SL80486DX/CX486DX2/SL80486DX2/80486DX4/AM486DX4/AM5X86
Processor Speed	25/33/40/50(internal)/50/66(internal)/80(internal)/100(internal)/ 120(internal)/133(internal)MHz
Chip Set	SIS
Video Chip Set	None
Maximum Onboard Memory	32MB
Maximum Video Memory	None
Cache	128KB
BIOS	Award
Dimensions	190mm x 124mm
I/O Options	Floppy drive interface, green PC connector, IDE interface, parallel port, serial ports (2), PC/104 connectors (2), VGA module connector
NPU Options	None



CONNECTIONS			
Purpose	**Location**	**Purpose**	**Location**
Serial port 1	CN1	Floppy drive interface	CN8
Auxiliary keyboard connector	CN2	Parallel port	CN9
Serial port 2	CN3	Power LED & keylock	JP3A
PC/104 connector	CN4	Speaker	JP4A
PC/104 connector	CN5	Green PC connector	JP13
IDE interface	CN6	Reset switch	JP48
VGA module connector	CN7	IDE interface LED	JP51

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USER CONFIGURABLE SETTINGS		
Function	**Label**	**Position**
Turbo disabled	J1	Pins 1 & 2 closed
Turbo enabled	J1	Pins 2 & 3 closed
Use non turbo pin for break switchJP14	J1	Pins 4 & 5 closed
í Factory configured - do not alter	J2A	Unidentified
í Factory configured - do not alter	J2B	Unidentified
IDE interface enabled	JP1	Open
IDE interface disabled	JP1	Closed
All CPU types	JP12	Open
CX486S2 CPU only	JP12	Closed
RC pin used for break switch	JP14	Pins 1 & 2 closed
RC pin used for RC	JP14	Pins 2 & 3 closed
Internal CLK = CPU OSC	JP15	Pins 1 & 2 closed
Internal CLK = 1/2 CPU OSC	JP15	Pins 2 & 3 closed
CLKIN = CPUCLK	JP20	Pins 1 & 2 closed
CLKIN delayed for CPUCLK	JP20	Pins 2 & 3 closed
í Factory configured - do not alter	JP22	Unidentified
CLK down by STPCLK control	JP27	Pins 1 & 2 closed
CLK down by SMOUT 0 control	JP27	Pins 2 & 3 closed
Monitor type select EGA	JP38	Closed
Monitor type select monochrome/VGA	JP38	Open
í Factory configured - do not alter	JP47	Unidentified

DRAM CONFIGURATION		
Size	**Bank 0**	**Bank 1**
1MB	(1) 256K x 36	None
2MB	(1) 512K x 36	None
2MB	(1) 256K x 36	(1) 256K x 36
4MB	(1) 1M x 36	None
4MB	(1) 512K x 36	(1) 512K x 36
8MB	(1) 2M x 36	None
8MB	(1) 1M x 36	(1) 1M x 36
16MB	(1) 4M x 36	None
16MB	(1) 2M x 36	(1) 2M x 36
32MB	(1) 4M x 36	(1) 4M x 36

CACHE CONFIGURATION
Note: The location of the 128KB cache is unidentified.

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CPU SPEED SELECTION			
Speed	**JP28**	**JP29**	**JP30**
25MHz	Closed	Open	Open
33MHz	Closed	Closed	Closed
40MHz	Closed	Closed	Open
50iMHz	Closed	Open	Open
50MHz	Open	Open	Closed
66iMHz	Closed	Closed	Closed
80iMHz	Closed	Closed	Open
100iMHz	Closed	Closed	Closed
120iMHz	Closed	Closed	Open
133iMHz	Closed	Closed	Closed

CPU TYPE SELECTION						
Type	**JP3**	**JP4**	**JP5**	**JP7**	**JP8**	**JP9**
CXM6	Open	2 & 3	Open	1 & 2, 3 & 4	2 & 3	2 & 3
80486SX	Open	Open	Open	Open	Open	1 & 2
SL80486SX	1 & 2	Open	Open	2 & 3	Open	1 & 2
CX486DX	Open	2 & 3	Open	1 & 2, 3 & 4	2 & 3	2 & 3
AM486DXL	Open	Open	Open	Open	3 & 4	2 & 3
80486DX	Open	Open	Open	Open	Open	1 & 2
SL80486DX	1 & 2	Open	Open	2 & 3	Open	1 & 2
CX486DX2	Open	2 & 3	Open	1 & 2, 3 & 4	2 & 3	2 & 3
SL80486DX2	1 & 2	Open	Open	2 & 3	Open	1 & 2
80486DX4	1 & 2	Open	Open	2 & 3	Open	1 & 2
AM486DX4	2 & 3	Open	Closed	2 & 3	Open	2 & 3
AM 5X86	2 & 3	Open	Closed	2 & 3	*	2 & 3
Note: Pins designated should be in the closed position. * = Close JP6 pin 3 to JP8 pin 3.						

CPU TYPE SELECTION (CON'T)					
Type	**JP10**	**JP11**	**JP16**	**JP17**	**JP18**
CXM6	Open	2 & 3	1 & 2	2 & 3, 4 & 5	1 & 2
80486SX	Open	2 & 3	2 & 3	Open	1 & 2
SL80486SX	Open	2 & 3	2 & 3	3 & 4	1 & 2
CX486DX	3 & 4	2 & 3	1 & 2	2 & 3	1 & 2
AM486DXL	1 & 2	2 & 3	1 & 2	Open	2 & 3
80486DX	3 & 4	2 & 3	1 & 2	Open	1 & 2
SL80486DX	3 & 4	2 & 3	1 & 2	3 & 4	1 & 2
CX486DX2	3 & 4	2 & 3	1 & 2	2 & 3	1 & 2
SL80486DX2	3 & 4	2 & 3	1 & 2	3 & 4	1 & 2
80486DX4	3 & 4	2 & 3	1 & 2	3 & 4	1 & 2
AM486DX4	3 & 4	1 & 2	1 & 2	1 & 2, 3 & 4	1 & 2
AM 5X86	3 & 4	1 & 2	1 & 2	1 & 2, 3 & 4	1 & 2
Note: Pins designated should be in the closed position.					

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CPU TYPE SELECTION (CON'T)						
Type	**JP19**	**JP21**	**JP23**	**JP24**	**JP25**	**JP26**
CXM6	Open	1 & 2	2 & 3	Open	1 & 2	1 & 2
80486SX	Open	2 & 3	Open	Open	1 & 2	1 & 2
SL80486SX	Open	2 & 3	4 & 5	Open	1 & 2	1 & 2
CX486DX	Closed	1 & 2	2 & 3	Open	1 & 2	1 & 2
AM486DXL	Closed	1 & 2	Open	Open	1 & 2	1 & 2
80486DX	Closed	2 & 3	Open	Open	1 & 2	1 & 2
SL80486DX	Closed	2 & 3	4 & 5	Open	1 & 2	1 & 2
CX486DX2	Closed	1 & 2	2 & 3	Open	1 & 2	1 & 2
SL80486DX2	Closed	2 & 3	4 & 5	Open	1 & 2	1 & 2
80486DX4	Closed	2 & 3	4 & 5	Open	2 & 3	2 & 3
AM486DX4	Closed	1 & 2	4 & 5	Closed	2 & 3	2 & 3
AM 5X86	Closed	1 & 2	4 & 5	Closed	2 & 3	2 & 3
Note: Pins designated should be in the closed position. * = Close JP6 pin 3 t0 JP8 pin 3.						

VL IDE SPEED SELECTION		
Speed	**JP2**	**JP6**
í 0	Pins 2 & 3 closed	Pins 2 & 3 closed
2	Pins 1 & 2 closed	Pins 2 & 3 closed
4	Pins 2 & 3 closed	Pins 1 & 2 closed
6	Pins 1 & 2 closed	Pins 1 & 2 closed

DMA CHANNEL SELECTION						
Channel	**JP31**	**JP32**	**JP33**	**JP34**	**JP35**	**JP36**
0	Closed	Open	Open	Open	Open	Closed
1	Open	Open	Open	Closed	Closed	Open
í 3	Open	Closed	Closed	Open	Open	Open

PARALLEL PORT INTERRUPT SELECTION		
IRQ	**JP52**	**JP53**
IRQ5	Pins 2 & 3 closed	Pins 1 & 2 closed
í IRQ7	Pins 1 & 2 closed	Pins 2 & 3 closed

MEDIA SENSE VALIDITY SELECTION		
Setting	**JP40**	**JP42**
Disabled	Closed	Closed
Enabled	Open	Open

WATCHDOG STATUS SELECTION	
Setting	**JP50**
í Program	Pins 3 & 4 closed
Enabled	Pins 1 & 2 closed
Disabled	Pins 5 & 6 closed

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WATCHDOG TIMER SELECTION	
Timer	**JP37**
í 1.5 seconds	Pins 1 & 2 closed
15 seconds	Pins 3 & 4 closed
150 seconds	Pins 5 & 6 closed

INDEX & REGISTER SELECTION			
Index address	**Data address**	**JP39**	**JP41**
398H	399H	Open	Open
í 26EH	26FH	Closed	Open
15CH	15DH	Open	Closed
02EH	02FH	Closed	Closed

FER = 4F, CF SELECTION										
FDC	**IDE**	**COM1**	**COM2**	**LPT**	**DATA**	**J43**	**J44**	**J45**	**J46**	**J49**
PRI	PRI	COM1	COM2	LPT2	10	Open	Open	Open	Open	Open
PRI	PRI	COM1	COM2	LPT1	11	Closed	Open	Open	Open	Open
PRI	SEC	COM1	COM2	LPT1	11	Open	Closed	Open	Open	Open
PRI	PRI	COM3	COM4	LPT1	39	Closed	Closed	Open	Open	Open
PRI	PRI	COM2	COM3	LPT2	24	Open	Open	Closed	Open	Open
PRI	SEC	COM3	COM4	LPT2	38	Closed	Open	Closed	Open	Open

FER = 4B, CB SELECTION										
FDC	**IDE**	**COM1**	**COM2**	**LPT**	**DATA**	**J43**	**J44**	**J45**	**J46**	**J49**
PRI	PRI	COM1	None	LPT2	00	Open	Closed	Closed	Open	Open
PRI	PRI	COM1	None	LPT1	01	Closed	Closed	Closed	Open	Open
PRI	SEC	COM1	None	LPT1	01	Open	Open	Open	Closed	Open
PRI	PRI	COM3	None	LPT1	09	Closed	Open	Open	Closed	Open
PRI	PRI	COM3	None	LPT2	08	Open	Closed	Open	Closed	Open
PRI	SEC	COM3	None	LPT2	08	Closed	Closed	Open	Closed	Open

FER = OF SELECTION										
FDC	**IDE**	**COM1**	**COM2**	**LPT**	**DATA**	**J43**	**J44**	**J45**	**J46**	**J49**
PRI	None	COM1	COM2	LPT2	10	Open	Open	Closed	Closed	Open
PRI	None	COM1	COM2	LPT1	11	Closed	Open	Closed	Closed	Open
PRI	None	COM3	COM4	LPT1	39	Open	Closed	Closed	Closed	Open
PRI	None	COM2	COM3	LPT2	24	Closed	Closed	Closed	Closed	Open

FER = 49, C9 SELECTION										
FDC	**IDE**	**COM1**	**COM2**	**LPT**	**DATA**	**J43**	**J44**	**J45**	**J46**	**J49**
PRI	PRI	None	None	LPT2	00	Open	Open	Open	Open	Closed
PRI	PRI	None	None	LPT1	01	Closed	Open	Open	Open	Closed
PRI	SEC	None	None	LPT1	01	Open	Closed	Open	Open	Closed
PRI	SEC	None	None	LPT2	00	Closed	Closed	Open	Open	Closed

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FER = 07 SELECTION										
FDC	**IDE**	**COM1**	**COM2**	**LPT**	**DATA**	**J43**	**J44**	**J45**	**J46**	**J49**
None	None	COM1	COM2	LPT2	10	Open	Open	Closed	Open	Closed
None	None	COM1	COM2	LPT1	11	Closed	Open	Closed	Open	Closed
None	None	COM3	COM4	LPT1	39	Open	Closed	Closed	Open	Closed
None	None	COM2	COM3	LPT2	24	Closed	Closed	Closed	Open	Closed

FER = 47, C7 SELECTION										
FDC	**IDE**	**COM1**	**COM2**	**LPT**	**DATA**	**J43**	**J44**	**J45**	**J46**	**J49**
None	PRI	COM1	COM2	LPT2	10	Open	Open	Open	Closed	Closed
None	PRI	COM1	COM2	LPT1	11	Closed	Open	Open	Closed	Closed
None	SEC	COM1	COM2	LPT1	11	Open	Closed	Open	Closed	Closed
None	PRI	COM3	COM4	LPT1	39	Closed	Closed	Open	Closed	Closed
None	PRI	COM2	COM3	LPT2	24	Open	Open	Closed	Closed	Closed
None	SEC	COM3	COM4	LPT2	38	Closed	Open	Closed	Closed	Closed

FER = 08 SELECTION										
FDC	**IDE**	**COM1**	**COM2**	**LPT**	**DATA**	**J43**	**J44**	**J45**	**J46**	**J49**
PRI	None	None	None	None	00	Closed	Closed	Closed	Closed	Open

FER = 00 SELECTION										
FDC	**IDE**	**COM1**	**COM2**	**LPT**	**DATA**	**J43**	**J44**	**J45**	**J46**	**J49**
NA	None	None	None	None	00	Closed	Closed	Closed	Closed	Closed