UNIDENTIFIED 386DX W/B

80386DX/CX486DLC **Processor**

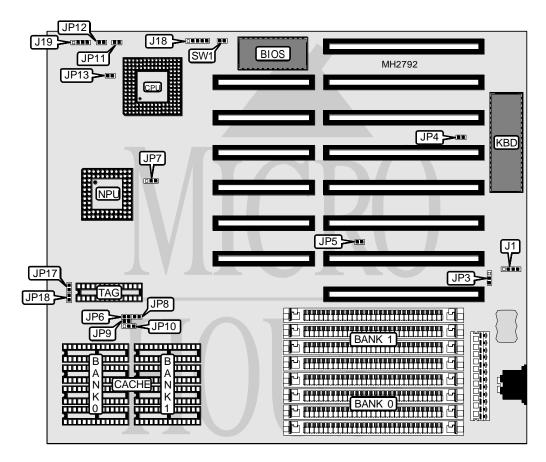
Processor Speed 33/40MHz Chip Set OPTI Max. Onboard DRAM 32MB

64/128/256KB Cache

BIOS AMI

Dimensions 254mm x 218mm

I/O Options None **NPU Options** CX487DLC



CONNECTIONS				
Purpose	Location	Purpose	Location	
External battery	J1	Turbo switch	JP11	
Power LED & keylock	J18	Turbo LED	JP12	
Speaker	J19	Reset switch	SW1	

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USER CONFIGURABLE SETTINGS			
Function	Jumper	Position	
í CMOS memory normal operation	JP3	pins 2 & 3 closed	
CMOS memory clear	JP3	pins 1 & 2 closed	
í Monitor type select color	JP4	Closed	
Monitor type select monochrome	JP4	Open	
í CPU clock type select single phase	JP7	pins 2 & 3 closed	
CPU clock type select double phase	JP7	pins 1 & 2 closed	

	DRAM CONFIGURATION	
Size	Bank 0	Bank 1
1MB	(4) 256K x 9	NONE
2MB	(4) 256K x 9	(4) 256K x 9
4MB	(4) 1M x 9	NONE
5MB	(4) 256K x 9	(4) 1M x 9
8MB	(4) 1M x 9	(4) 1M x 9
16MB	(4) 4M x 9	NONE
20MB	(4) 1M x 9	(4) 4M x 9
20MB	(4) 4M x 9	(4) 1M x 9
32MB	(4) 4M x 9	(4) 4M x 9

CACHE CONFIGURATION				
Size	Bank 0	Bank 1	TAG	
64KB	(4) 8K x 8	(4) 8K x 8	(1) 8K x 8	
128KB	(4) 32K x 8	NONE	(1) 8K x 8	
256KB	(4) 32K x 8	(4) 32K x 8	(1) 32K x 8	

CACHE JUMPER CONFIGURATION						
Size	JP6	JP8	JP9	JP10	JP17	JP18
64KB	Open	Open	Open	2 & 3	Open	Open
128KB	Closed	Closed	Open	1 & 2	Open	Closed
256KB	Closed	Closed	Closed	2 & 3	Closed	Closed
Note: Pins designated should be in the closed position.						

CPU TYPE CONFIGURATION				
Type	JP1	JP5	JP13	
Cyrix	Closed	Closed	Closed	
Intel	Open	Open	Open	
Note: The location of JP1 is unidentified.				