ELITEGROUP COMPUTER SYSTEMS, INC.
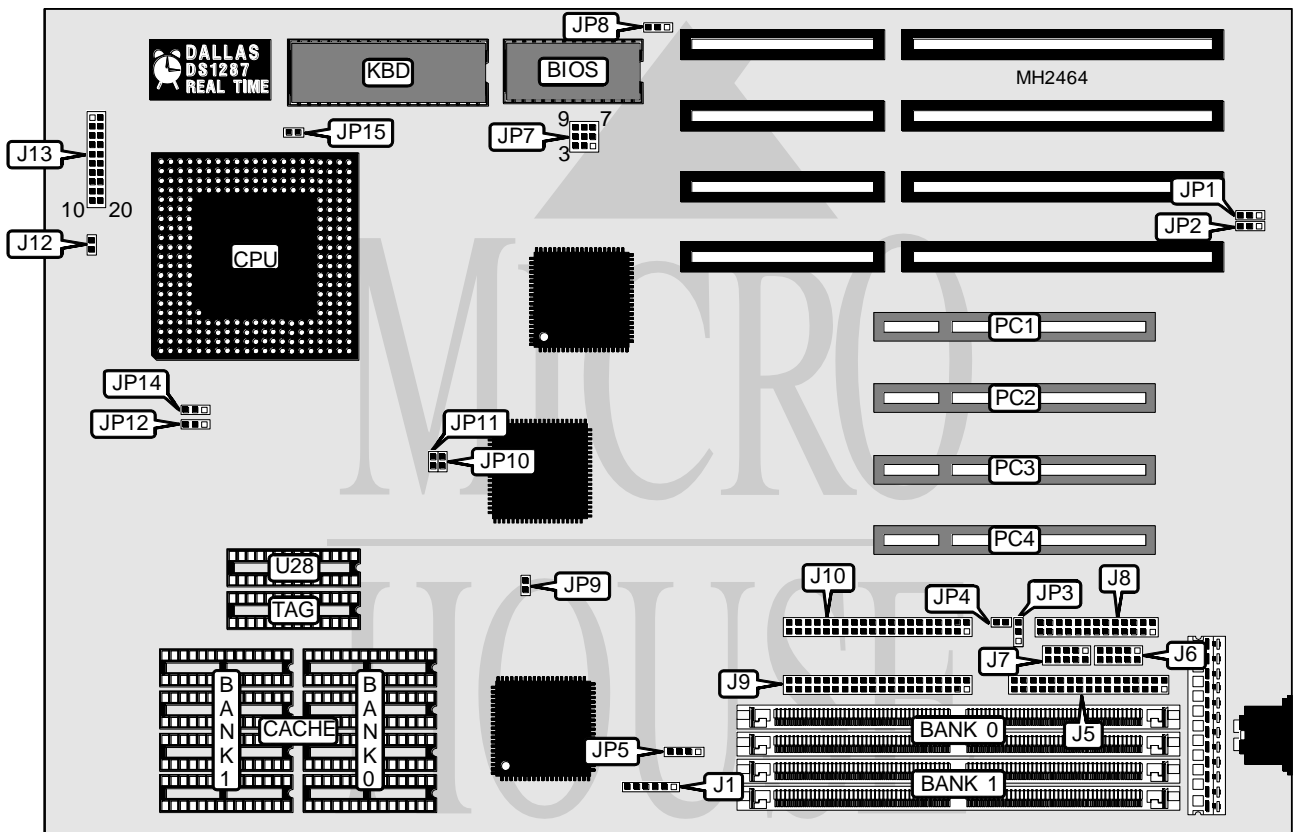# SI54P AIO

Processor	Pentium
Processor Speed	75/90/100MHz
Chip Set	SIS
Max. Onboard DRAM	128MB
Cache	256/512/1024KB
BIOS	Award
Dimensions	330mm x 218mm
I/O Options	32-bit PCI slots (4), floppy drive interface, green PC connector, IDE interfaces (2), parallel port, serial ports (2)
NPU Options	None

CONNECTIONS			
Purpose	Location	Purpose	Location
3.3v connector	J1	Turbo LED	J13 pins 2 - 3
Floppy drive interface	J5	Green PC connector	J13 pins 4 - 5
Serial port 1	J6	Turbo switch	J13 pins 6 - 7
Serial port 2	J7	Reset switch	J13 pins 9 - 10
Parallel port	J8	Power LED & keylock	J13 pins 11 - 15
IDE interface 1	J9	Speaker	J13 pins 17 - 20
IDE interface 2	J10	32-bit PCI slots	PC1 - PC4
IDE interface LED	J12		

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USER CONFIGURABLE SETTINGS		
Function	Jumper	Position
í On board I/O enabled	JP3	pins 1 & 2 closed
On board I/O disabled	JP3	pins 2 & 3 closed
í PCI IDE interface enabled	JP4	Open
PCI IDE interface disabled	JP4	Closed
í DRAM parity check enabled	JP9	Closed
DRAM parity check disabled	JP9	Open
í Factory configured - do not alter	JP15	N/A

DRAM CONFIGURATION		
Size	Bank 0	Bank 1
2MB	(2) 256K x 36	NONE
4MB	(2) 256K x 36	(2) 256K x 36
4MB	(2) 512K x 36	NONE
8MB	(2) 512K x 36	(2) 512K x 36
8MB	(2) 1M x 36	NONE
16MB	(2) 1M x 36	(2) 1M x 36
16MB	(2) 2M x 36	NONE
32MB	(2) 2M x 36	(2) 2M x 36
36MB	(2) 512K x 36	(2) 4M x 36
36MB	(2) 4M x 36	(2) 512K x 36
48MB	(2) 2M x 36	(2) 4M x 36
64MB	(2) 4M x 36	(2) 4M x 36
64MB	(2) 8M x 36	NONE
128MB	(2) 8M x 36	(2) 8M x 36

DRAM JUMPER CONFIGURATION	
Size	JP5
Single sided only	pins 2 & 3 closed
Single and double sided	pins 1 & 2, 3 & 4 closed

CACHE CONFIGURATION				
Size	Bank 0	Bank 1	TAG	Dirty (U28)
256KB	(4) 32K x 8	(4) 32K x 8	(1) 32K x 8	(1) 32K x 8
512KB	(4) 64K x 8	(4) 64K x 8	(1) 32K x 8	(1) 32K x 8
1MB	(4) 128K x 8	(4) 128K x 8	(1) 32K x 8	(1) 32K x 8

CACHE JUMPER CONFIGURATION		
Size	JP10	JP11
256KB	Open	Open
512KB	Open	Closed
1MB	Closed	Closed

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CPU SPEED CONFIGURATION	
Speed	JP7
75MHz	pins 2 & 3, 5 & 6, 7 & 8 closed
90MHz	pins 2 & 3, 4 & 5, 8 & 9 closed
100MHz	pins 1 & 2, 5 & 6, 7 & 8 closed

CPU SIGNAL CONFIGURATION		
Type	JP12	JP14
Write back cache	pins 1 & 2 closed	N/A
Write through cache	pins 2 & 3 closed	N/A
Always invalidated	N/A	pins 1 & 2 closed
Write to invalidated	N/A	pins 2 & 3 closed

ECP MODE CONFIGURATION		
Setting	JP1	JP2
DRQ1 - DACK1	pins 1 & 2 closed	pins 2 & 3 closed
DRQ3 - DACK3	pins 2 & 3 closed	pins 1 & 2 closed

BIOS CONFIGURATION	
Setting	JP8
Flash ROM +5v	pins 1 & 2 closed
Flash ROM +12v	pins 2 & 3 closed
EPROM	Open