AUVA COMPUTER, INC. TAM33-MA0/TAM40-MA0/TAM33-MA1/TAM40-MA1/TAM33-MAK

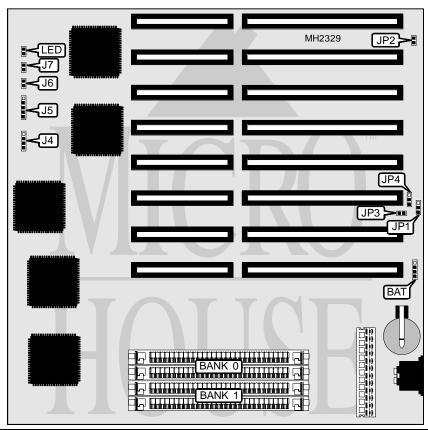
80386DX/CX486DLC (exact location unknown) **Processor**

Processor Speed 33/40MHz Unidentified **Chip Set** Max. Onboard DRAM 32MB Cache 8KB

BIOS Unidentified **Dimensions** 240mm x 220mm

I/O Options None

NPU Options CX487DLC/80387/3167 (exact location unknown)



CONNECTIONS				
Purpose	Location	Purpose	Location	
External battery	BAT	Turbo switch	J6	
Speaker	J4	Reset switch	J7	
Power LED & keylock	J5	Turbo LED	LED	

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USER CONFIGURABLE SETTINGS				
Function	Jumper	Position		
í CMOS memory select normal	JP1	pins 1 & 2 closed		
CMOS memory clear	JP1	pins 2 & 3 closed		
Note: Exact configurations for JP2 - Monitor type select are unidentified.				

DRAM CONFIGURATION				
Size	Bank 0	Bank 1		
1MB	(4) 256K x 9	NONE		
2MB	(4) 256K x 9	(4) 256K x 9		
4MB	(4) 1M x 9	NONE		
5MB	(4) 256K x 9	(4) 1M x 9		
8MB	(4) 1M x 9	(4) 1M x 9		
16MB	(4) 4M x 9	NONE		
20MB	(4) 1M x 9	(4) 4M x 9		
32MB	(4) 4M x 9	(4) 4M x 9		

CMOS CONFIGURATION				
Type	Type JP3			
DS1287	Open	pins 1 & 2 closed		
MC146818	Closed	pins 2 & 3 closed		