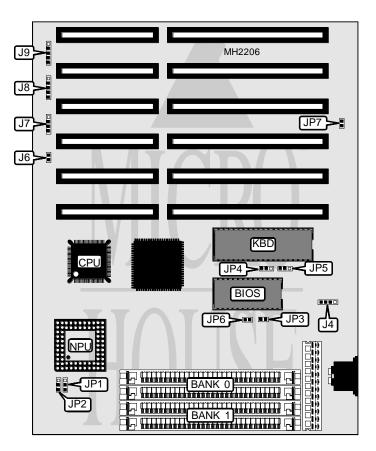
UNIDENTIFIED PVI-486AP4

Processor
Processor Speed
Chip Set
Max. Onboard DRAM
Cache
BIOS
Dimensions
I/O Options
NPU Options

80386SX 25/33/40MHz ALI 16MB None AMI/Award 254mm x 218mm None 80387SX



CONNECTIONS					
Purpose	Location	Purpose	Location		
External battery	J4	Turbo switch & LED	18		
Reset switch	JG	Power LED & keylock	19		
Speaker	J7				

Continued on next page. . .

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USER CONFIGURABLE SETTINGS				
Function	Jumper	Position		
í NPU synchronous with CPU	JP2	pins 1 & 2 closed		
NPU asynchronous with CPU	JP2	pins 2 & 3 closed		
í CMOS memory normal operation	JP3	Open		
CMOS memory clear	JP3	Closed		
í Monitor type select color	JP4	pins 2 & 3 closed		
Monitor type select monochrome	JP4	pins 1 & 2 closed		
í Parity check enabled	JP6	Open		
Parity check disabled	JP6	Closed		
í TTL installed	JP7	Open		
TTL not installed	JP7	Closed		

DRAM CONFIGURATION				
Size	Bank 0	Bank 1		
512KB	(2) 256K x 9	NONE		
1MB	(2) 256K x 9	(2) 256K x 9		
2MB	(2) 1M x 9	NONE		
4MB	(2) 1M x 9	(2) 1M x 9		
8MB	(2) 4M x 9	NONE		
16MB	(2) 4M x 9	(2) 4M x 9		

CPU SPEED CONFIGURATION				
Speed	JP1	JP5		
25MHz	pins 1 & 2 closed	pins 2 & 3 closed		
33MHz	pins 2 & 3 closed	pins 2 & 3 closed		
40MHz	pins 1 & 2 closed	pins 1 & 2 closed		