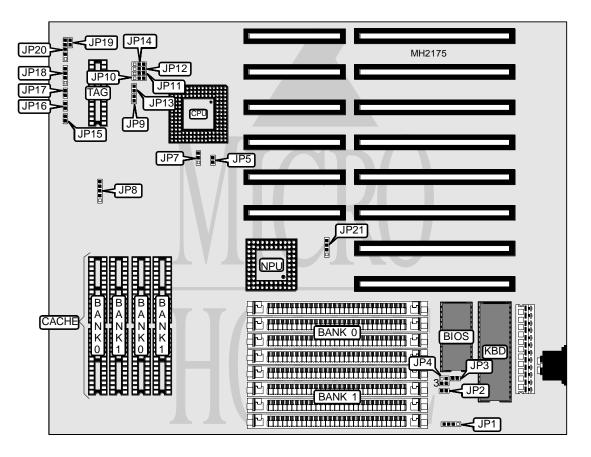
ROBOTECH, INC. G M B - 3 8 6 U N

Processor	80386DX
Processor Speed	33/40MHz
Chip Set	UMC
Max. Onboard DRAM	32MB
Cache	32/64/128/256KB
BIOS	AMI
Dimensions	254mm x 220mm
I/O Options	None
NPU Options	80387DX/3167



CONNECTIONS				
Purpose Location Purpose Location				
External battery	JP1	Speaker	JP18	
Turbo LED	JP16	Reset switch	JP19	
Turbo switch	JP17	Power LED & keylock	JP20	

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USER CONFIGURABLE SETTINGS				
Function	Jumper	Position		
í CMOS memory normal operation	JP2	pins 1 & 2 closed		
CMOS memory clear	JP2	pins 2 & 3 closed		
í Monitor type select color	JP3	Closed		
Monitor type select monochrome	JP3	Open		

DRAM CONFIGURATION				
Size	Bank 0	Bank 1		
1MB	(4) 256K x 9	NONE		
2MB	(4) 256K x 9	(4) 256K x 9		
4MB	(4) 1M x 9	NONE		
5MB	(4) 256K x 9	(4) 1M x 9		
8MB	(4) 1M x 9	(4) 1M x 9		
16MB	(4) 4M x 9	NONE		
20MB	(4) 256K x 9	(4) 1M x 9		
20MB	(4) 1M x 9	(4) 256K x 9		
32MB	(4) 4M x 9	(4) 4M x 9		

CACHE CONFIGURATION					
Size	Bank 0	Bank 1	TAG		
32KB	(4) 8K x 8	NONE	(1) 8K x 8		
64KB	(4) 8K x 8	(4) 8K x 8	(1) 8K x 8		
128KB	(4) 32K x 8	NONE	(1) 8K x 8		
256KB	(4) 32K x 8	(4) 32K x 8	(1) 32K x 8		

	CACHE JUMPER CONFIGURATION (WRITE BACK)							
Size	JP8	JP9	JP10	JP11	JP12	JP13	JP14	JP15
32KB	2&3	Open	2&3	1&2	2&3	Open	2&3	Open
64KB	1 & 2	Closed	2&3	2&3	1&2	Open	2&3	Open
128KB	1&2,3&4	Closed	1&2	2&3	2&3	Closed	2&3	Open
256KB	1&2,4&5	Closed	2&3	2&3	2&3	Closed	1&2	Closed
Note: Pins designated should be in the closed position.								

	CACHE JUMPER CONFIGURATION (WRITE THROUGH)							
Size	JP8	JP9	JP10	JP11	JP12	JP13	JP14	JP15
32KB	2 & 3	Open	2&3	2&3	2&3	Open	2&3	Open
64KB	1 & 2	Closed	2&3	2&3	2&3	Open	2&3	Open
128KB	1&2,3&4	Closed	2&3	2&3	2&3	Closed	2&3	Open
256KB	1&2,4&5	Closed	2&3	2&3	2&3	Closed	2&3	Closed
Note: Pins designated should be in the closed position.								

CPU SPEED CONFIGURATION				
Speed	JP7	JP21		
33MHz	pins 1 & 2 closed	pins 1 & 2 closed		
40MHz	pins 2 & 3 closed	pins 1 & 2 closed		

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MATH COPROCESSOR WAIT STATE CONFIGURATION		
Wait states	JP5	
0 wait states	Closed	
1 wait state	Open	

A20 GATE CONFIGURATION				
Setting	JP4			
Hardware emulate	Open			
8042 keyboard controller	pins 1 & 2 closed			
Cyrix CPU emulate	pins 2 & 4 closed			
Keyboard controller controls Cyrix CPU	pins 3 & 4 closed			