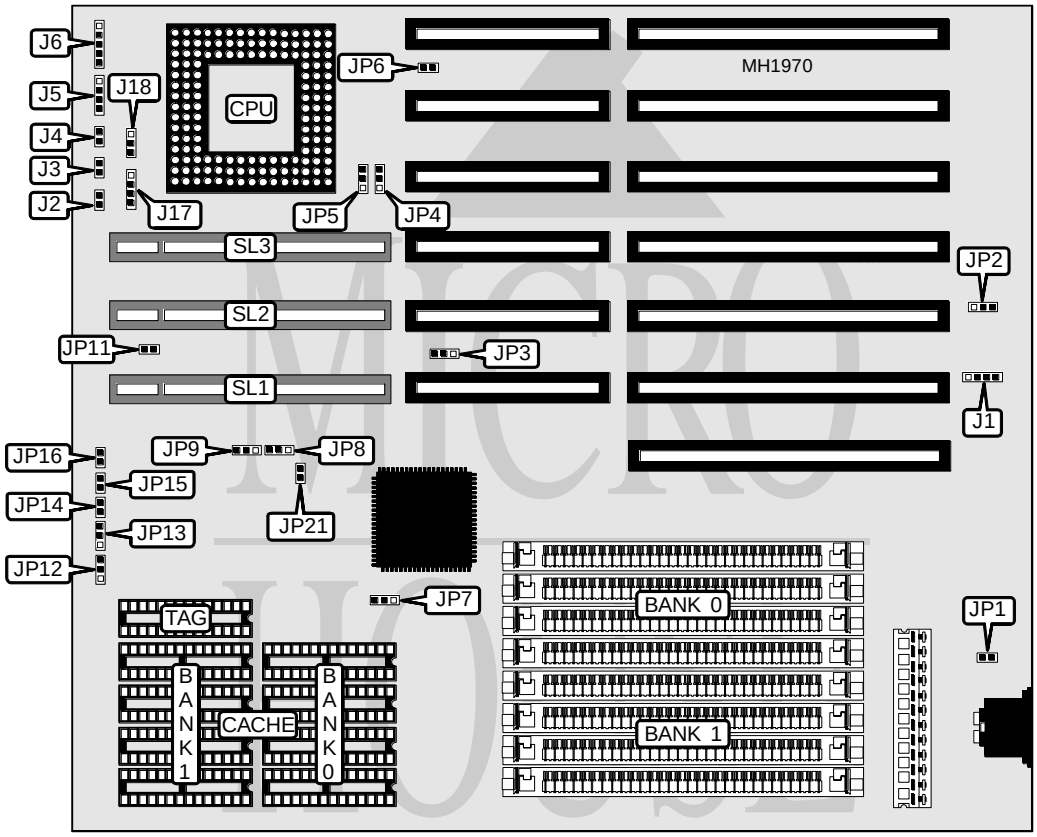
PINE TECHNOLOGY
P T - 4 2 8

Processor	80486SX/80486DX/80486DX2
Processor Speed	25/33/40/50(internal)/50/66(internal)MHz
Chip Set	UMC
Max. Onboard DRAM	32MB
Cache	32/64/128/256KB
BIOS	AMI
Dimensions	250mm x 220mm
I/O Options	32-bit VESA local bus slots (3)
NPU Options	None



CONNECTIONS			
Purpose	Location	Purpose	Location
External battery	J1	Speaker	J5
Reset switch	J2	Power LED & keylock	J6
Turbo switch	J3	32-bit VESA Local bus slots	SL1,SL2 & SL3
Turbo LED	J4		

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USER CONFIGURABLE SETTINGS		
Function	Jumper	Position
í Battery type select - internal	JP1	Closed
Battery type select - internal	JP1	Open
í Power good signal detect from power supply	JP2	pins 1 & 2 closed
Power good signal detect from board	JP2	pins 2 & 3 closed
í VGA card select - normal	JP3	pins 1 & 2 closed
VGA card select - POWER 9000	JP3	pins 2 & 3 closed
í CPU test logic enabled	JP6	Open
CPU test logic disabled	JP6	Closed
í (MCA1) LDEV# direct connect to 491 ELBA#	JP7	pins 1 & 2 closed
LDEV# through and gate to 491 ELBA#	JP7	pins 2 & 3 closed
í CPU speed select < 33MHz	JP11	Open
CPU speed select > 33MHz	JP11	Closed

DRAM CONFIGURATION		
Size	Bank 0	Bank 1
1MB	(4) 256K x 9	NONE
2MB	(4) 256K x 9	(4) 256K x 9
4MB	(4) 1M x 9	NONE
5MB	(4) 1M x 9	(4) 256K x 9
8MB	(4) 1M x 9	(4) 1M x 9
16MB	(4) 4M x 9	NONE
20MB	(4) 1M x 9	(4) 4M x 9
32MB	(4) 4M x 9	(4) 4M x 9

CACHE CONFIGURATION			
Size	Bank 0	Bank 1	TAG
32KB	(4) 8K x 8	NONE	(1) 8K x 8
64KB	(4) 8K x 8	(4) 8K x 8	(1) 8K x 8
128KB	(4) 32K x 8	NONE	(1) 8K x 8
256KB	(4) 32K x 8	(4) 32K x 8	(1) 32K x 8

CACHE JUMPER CONFIGURATION					
Size	JP12	JP13	JP14	JP15	JP16
32MB	Open	2 & 3	Open	Open	Open
64KB	Open	1 & 2	Open	Closed	Open
128KB	2 & 3	2 & 3	Open	Closed	Closed
256KB	1 & 2	1 & 2	Closed	Closed	Closed
Note: pins designated should be in the closed position.					

CPU TYPE CONFIGURATION		
CPU Type	J17	J18
80486SX	pins 2 & 3 closed	Open
80486DX/DX2	pins 1, 2, 3 & 4 closed	pins 1 & 2 closed
Pentium Overdrive	pins 1, 2, 3 & 4 closed	pins 2 & 3 closed

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CPU SPEED CONFIGURATION (CHRONTEL CH9007C CLOCK)		
Speed	JP8	JP9
25MHz	pins 1 & 2 closed	pins 1 & 2 closed
33MHz	pins 2 & 3 closed	pins 1 & 2 closed
40MHz	pins 1 & 2 closed	pins 2 & 3 closed
50iMHz	pins 1 & 2 closed	pins 1 & 2 closed
50MHz	pins 2 & 3 closed	pins 2 & 3 closed
66iMHz	pins 2 & 3 closed	pins 1 & 2 closed

CPU SPEED CONFIGURATION (PHASE LINE PLL52C05)			
Speed	JP8	JP9	JP21
25MHz	pins 1 & 2 closed	pins 1 & 2 closed	Closed
33MHz	pins 2 & 3 closed	pins 1 & 2 closed	Closed
40MHz	pins 1 & 2 closed	pins 2 & 3 closed	Open
50iMHz	pins 1 & 2 closed	pins 1 & 2 closed	Closed
50MHz	pins 2 & 3 closed	pins 2 & 3 closed	Open
66iMHz	pins 2 & 3 closed	pins 1 & 2 closed	Closed

VESA ID4 CONFIGURATION		
50MHz delay	JP4	JP5
No delay	pins 1 & 2 closed	pins 1 & 2 closed
1 - T	pins 2 & 3 closed	pins 2 & 3 closed