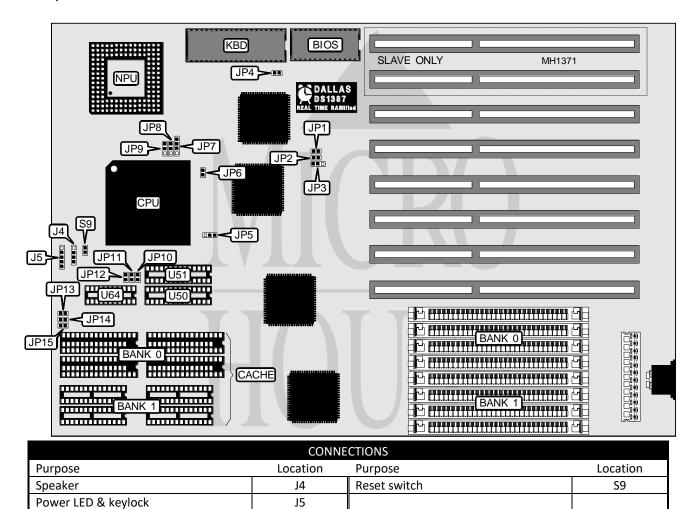
NOVACOR, INC. OPTIMUM EISA486SD - 6A5B1

| Processor | 80486SX/80487SX/80486DX | | | | |
|-------------------|-------------------------|--|--|--|--|
| Processor Speed | 20/25/33/40/50MHz | | | | |
| Chip Set | OPTI | | | | |
| Max. Onboard DRAM | 32MB | | | | |
| SRAM Cache | 64/128/256/512KB | | | | |
| BIOS | AMI | | | | |
| Dimensions | 330mm x 218mm | | | | |
| I/O Options | None | | | | |
| NPU Options | 4167 | | | | |



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| USER CONFIGURABLE SETTINGS | | | | | | |
|--------------------------------|--------|-------------------|--|--|--|--|
| Function | Jumper | Position | | | | |
| í Monitor type select color | JP4 | closed | | | | |
| Monitor type select monochrome | JP4 | open | | | | |
| CPU speed select iOCS/1 | JP8 | pins 1 & 2 closed | | | | |
| CPU speed select iOCS/2 | JP8 | pins 2 & 3 closed | | | | |

| DRAM CONFIGURATION | | | | | |
|--------------------|------------|------------|--|--|--|
| Size | Bank 0 | Bank 1 | | | |
| 4MB | (4) 1M x 9 | NONE | | | |
| 8MB | (4) 1M x 9 | (4) 1M x 9 | | | |
| 16MB | (4) 4M x 9 | NONE | | | |
| 20MB | (4) 1M x 9 | (4) 4M x 9 | | | |
| 32MB | (4) 4M x 9 | (4) 4M x 9 | | | |

| CPU TYPE CONFIGURATION | | | | | |
|-------------------------------------|-----------------------------|-------------------|--|--|--|
| CPU | JP7 | JP9 | | | |
| 80486DX | pins 1 & 2 and 3 & 4 closed | pins 2 & 3 closed | | | |
| 80487SX pins 1 & 2 and 3 & 4 closed | | pins 1 & 2 closed | | | |
| 80486SX | pins 2 & 3 closed | open | | | |

| CPU SPEED CONFIGURATION | | | | | | |
|-------------------------|--------|--------|-------------------|--------|--|--|
| Speed | JP1 | JP2 | JP3 | JP6 | | |
| 50MHz | closed | closed | pins 1 & 2 closed | open | | |
| 40MHz | open | closed | pins 1 & 2 closed | open | | |
| 33MHz | closed | open | pins 1 & 2 closed | open | | |
| 25MHz | open | open | pins 1 & 2 closed | open | | |
| 20MHz | open | open | pins 2 & 3 closed | closed | | |

| SRAM JUMPER CONFIGURATION | | | | | | | |
|--|-------------------|--------|--------|--------|--------|--------|--------|
| Size JP5 JP10 JP11 JP12 JP13 JP14 JP15 | | | | | | | JP15 |
| 64KB | pins 2 & 3 closed | open | open | open | open | open | open |
| 128KB | pins 1 & 2 closed | open | open | closed | open | closed | open |
| 256KB | pins 2 & 3 closed | open | closed | closed | closed | closed | open |
| 512KB | pins 1 & 2 closed | closed | closed | closed | closed | closed | closed |

| SRAM CONFIGURATION | | | | | | |
|--|--------------|-------------|-------------|------------|-----------------|--|
| Size | Cache SRAM | Location | TAG (U50) | TAG (U51) | Dirty bit (U64) | |
| 64KB | (8) 8K x 8 | Banks 0 & 1 | (1) 8K x 8 | N/A | (1) 16K x 1 | |
| 128KB | (4) 32K x 8 | Bank 0 | (1) 8K x 8 | N/A | (1) 16K x 1 | |
| 256KB | (8) 32K x 8 | Banks 0 & 1 | (1) 8K x 8 | (1) 8K x 8 | (1) 16K x 1 | |
| 512KB | (4) 128K x 8 | Bank 0 | (1) 32K x 8 | N/A | (1) 64K x 1 | |
| Note: Dirty bit (U64) can always accommodate (1) 64K x 1 for any of the four configurations. | | | | | | |