DD & TT ENTERPRISE USA COMPANY
DT-423S4L (REVISION C2 AND EARLIER)

Processor	80486SX/80487SX/80486DX
Processor Speed	20/25/33/50MHz
Chip Set	Symphony
Max. Onboard DRAM	32MB
Cache	64/256/1024KB
BIOS	AMI/MR
Dimensions	330mm x 218mm
I/O Options	None
NPU Options	4167
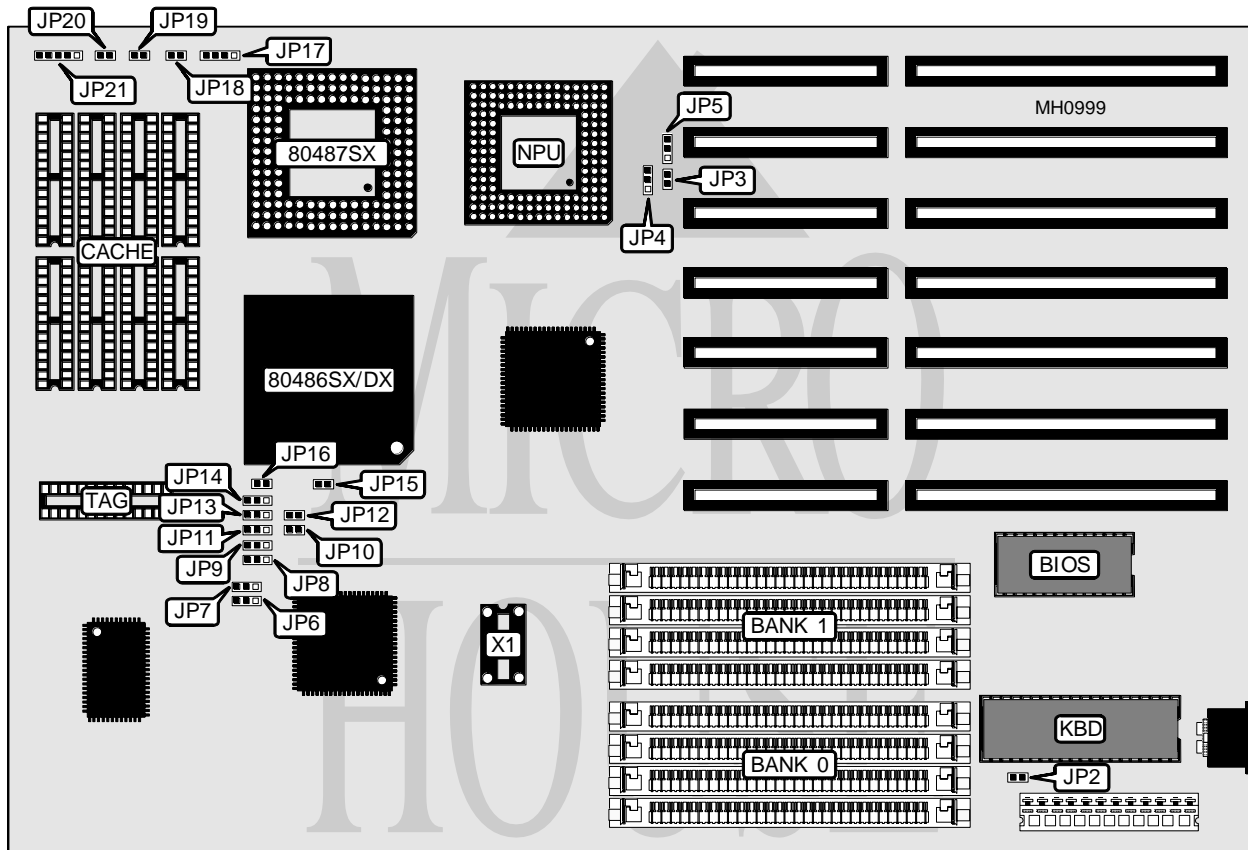
CONNECTIONS			
Purpose	Location	Purpose	Location
Speaker	JP17	Turbo switch	JP20
Turbo LED	JP18	Power LED & keylock	JP21
Reset switch	JP19		

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USER CONFIGURABLE SETTINGS		
Function	Jumper	Position
í Password check disabled	JP2	Open
Password check enabled	JP2	Closed
í Post-write buffer wait states select zero	JP12	Closed
Post-write buffer wait state select one	JP12	Open
í Cache burst fill cycle select 2-1-1-1	JP16	Open
Cache burst fill cycle select 3-2-2-2	JP16	Closed
Note: The oscillator installed at X1 must match the speed of the CPU installed. (iOSC/1)		

DRAM CONFIGURATION		
Size	Bank 0	Bank 1
1MB	(4) 256K x 9	NONE
2MB	(4) 256K x 9	(4) 256K x 9
4MB	(4) 1M x 9	NONE
5MB	(4) 1M x 9	(4) 256K x 9
5MB	(4) 256K x 9	(4) 1M x 9
8MB	(4) 1M x 9	(4) 1M x 9
16MB	(4) 4M x 9	NONE
17MB	(4) 4M x 9	(4) 256K x 9
20MB	(4) 4M x 9	(4) 1M x 9
20MB	(4) 1M x 9	(4) 4M x 9
32MB	(4) 4M x 9	(4) 4M x 9

CACHE CONFIGURATION		
Size	Bank 0	TAG
64KB	(8) 8K x 8	(1) 8K x 8
256KB	(8) 32K x 8	(1) 32K x 8
1024KB	(8) 128K x 8	(1) 128K x 8

CACHE JUMPER CONFIGURATION					
Size	JP8	JP9	JP11	JP13	JP14
64KB	1 & 2	1 & 2	1 & 2	1 & 2	1 & 2
256KB	2 & 3	2 & 3	2 & 3	1 & 2	1 & 2
1024KB	2 & 3	2 & 3	2 & 3	2 & 3	2 & 3
Note: Pins designated should be in the closed position.					

CPU TYPE CONFIGURATION			
Type	JP3	JP4	JP5
80486SX	Open	Open	pins 2 & 3 closed
80487SX	Closed	pins 2 & 3 closed	pins 1 & 2 closed
80486DX	Closed	pins 1 & 2 closed	pins 1 & 2 closed

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CPU SPEED CONFIGURATION		
Speed	JP7	JP10
iOSC/2 (use when CPU speed <= 33MHz)	pins 2 & 3 closed	Open
iOSC/1 (use when CPU speed > 33MHz)	pins 1 & 2 closed	Closed

SYSTEM READY CONFIGURATION		
Setting	JP6	JP15
SYSTEM READY signal select extended	pins 2 & 3 closed	Closed
SYSTEM READY signal select non-extended	pins 1 & 2 closed	Open