## JPN CORPORATION

## AT 286

| Processor | 80286 |
| :--- | :--- |
| Processor Speed | $12 / 16 / 25 \mathrm{MHz}$ |
| Chip Set | ACT |
| Max. Onboard DRAM | 4 MB |
| Cache | None |
| BIOS | AMI |
| Dimensions | $305 \mathrm{~mm} \times 222 \mathrm{~mm}$ |
| I/O Options | None |
| NPU Options | 80287 |



| Purpose |  |  |  |
| :--- | :---: | :--- | :---: |
| Location | Purpose | Location |  |
| Turbo LED | JP2 | External battery | JP11 |
| Power LED \& keylock | JP7 | Speaker | JP14 |
| Reset switch | JP10 | Turbo switch | JP19 |

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| USER CONFIGURABLE JUMPERS |  |  |
| :---: | :---: | :---: |
| Function | Jumper/Switch | Position |
| í BIOS type select 27128 | JP6 | pins 1 \& 2 closed |
| BIOS type select 27256 | JP6 | pins 2 \& 3 closed |
| í Monitor type select color | JP9 | pins 2 \& 3 closed |
| Monitor type select monochrome | JP9 | pins 1 \& 2 closed |
| í Battery select internal | JP12 | pins 2 \& 3 closed |
| Battery select external | JP12 | pins 1 \& 2 closed |
| í Power good signal detect from power supply | JP13 | pins 1 \& 2 closed |
| Power good signal detect from board | JP13 | pins 2 \& 3 closed |
| í Bus speed select 8Mhz | JP17 | pins 1 \& 2 closed |
| Bus speed select 6Mhz | JP17 | pins 2 \& 3 closed |
| í Parity check enabled | JP20 | pins $1 \& 2$ closed |
| Parity check disabled | JP20 | pins 2 \& 3 closed |
| í DRAM speed select 1 wait state | SW1/4 | On |
| DRAM speed select 0 wait states | SW1/4 | Off |


| DRAM CONFIGURATION |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Size | Bank 0 | Parity (P-0) | Bank 1 | Parity (P-1) | Bank 2 | Bank 3 |
| 512KB | (4) 44256 | (2) 41256 | NONE | NONE | NONE | NONE |
| 512KB | NONE | NONE | NONE | NONE | (2) $256 \mathrm{~K} \times 9$ | NONE |
| 640KB | (4) 44256 | (2) 41256 | (4) 4464 | (2) 4164 | NONE | NONE |
| 640KB | NONE | NONE | (4) 4464 | (2) 4164 | (2) $256 \mathrm{~K} \times 9$ | NONE |
| 1MB | (4) 44256 | (2) 41256 | (4) 44256 | (2) 41256 | NONE | NONE |
| 1 MB | (4) 44256 | (2) 41256 | NONE | NONE | NONE | (2) $256 \mathrm{~K} \times 9$ |
| 1MB | NONE | NONE | NONE | NONE | (2) $256 \mathrm{~K} \times 9$ | (2) $256 \mathrm{~K} \times 9$ |
| 2MB | NONE | NONE | NONE | NONE | (2) $1 \mathrm{M} \times 9$ | NONE |
| 4MB | NONE | NONE | NONE | NONE | (2) $1 \mathrm{M} \times 9$ | (2) $1 \mathrm{M} \times 9$ |


| DRAM SWITCH CONFIGURATION |  |  |  |
| :---: | :---: | :---: | :---: |
| Size | SW1/1 | SW1/2 | SW1/3 |
| 512 KB | On | On | On |
| 640 KB | On | Off | Off |
| 1 MB | On | Off | On |
| 2 MB | Off | On | On |
| 4 MB | Off | Off | On |

