I General Description

The UMC's HEAT (High End AT) Chip Set UM82C380 is a highly integrated, flexible solution for high performance 80386 PC/AT compatible systems. Fabricated using advanced 1.2μ CMOS VLSI technology, it provides high reliability, low power, low chip count features for system implementation. A commercial 25MHz/0 wait state. 12MByte main memory system with cache memory control and math-coprocessor features can be easily built in a standard baby AT size mother board (12" x 8.6") with all necessary components included.

II Features

- Highly integrated 25 MHz/0 wait state 80386 PC/AT compatible
- Supports UMC UM82152/INTEL 82385 Cache Controllers
- Easy Page/Cache mode interchange on motherboard
- 32-bit memory bus interface
- Slow DRAM 100/120 ns at 25/20 MHz 0 wait state operation
- Supports 1M/256K SIM module
- On-board memory up to 12MBytes, extendable to 32MBytes using add-on card
- Shadow RAM for system BIOS
- 8MHz I/O bus timing
- Supports 80287/80387 /3167 Math-coprocessor
- EMS 4.0 interface through software emulation
- DOS/OS2/XENIX/UNIX operation
- Commercially available BIOS (Phoenix/Award/AMI) applicable

III System Description

The UM82C380 series consists of five chips, the UM82C381 System Controller, UM82C382 Address Buffer, UM82C383 Data Buffer, UM82C384 Memory Controller and UM82C388/389 Cache Interface. Combined with UMC's UM82C206 Integrated Peripheral Controller, the chip set forms a highly integrated solution for 25MHz 80386 PC/AT systems with Page/Cache Mode options.

The UM82C380 series supports a local 32-bit CPU/MP bus, a 32-bit memory data bus, a 16-bit AT channel bus, an 8 bit I/O channel peripheral data bus and 8MHz system clock to provide the best compatibility with industry standards.

The UM82C381 is a System Controller. It provides all four bus control signals, synchronized reset for CPU and peripherals, refresh control, math-coprocessor (80287/80387) interface, address decoding logic, CLK2, BCLK and timer clock generation.

The UM82C382 is an Address Buffer. It provides address interface to processor address, system address, DMA address XA and latched XD bus. A 10-bit refresh counter is included for both 256K and 1M DRAM refresh.

The UM82C383 is a Data Buffer. It provides bus interface for CPU local data bus, system data bus and peripheral data bus. Word-swap logic is also built in to facilitate the 80386 read or write 32-bit data through PC/AT 16-bit data bus.

The UM82C384 is a Memory Controller. It provides control for 32-bit memory data bus, memory paging control for 256K and 1M DRAM, RAS and CAS control for system memory.

The UM82C388 is a Cache interface. It provides a simple DRAM controller to interface INTEL 82385 Cache controller with the system memory.

The UM82C389 is another Cache Interface. It also provides a simple DRAM Controller to interface UM82152 Cache Controller with the System Memory, it has been highly integrated for easy application.

IV System Configurations

Basically, three different 80386 PC/AT system configurations can be implemented using UM82C380 series HEAT chip set. These are Page Mode, UM82152 Cache Control Mode, and INTEL 82385 Cache Control Mode. All three mode implementations will require the four common core logic devices of HEAT chip set; UM82C381, UM82C382, UM82C383 and UM82C206. The UM82C384 will be needed for Page Mode , while UM82C389 and UM82C388 are needed for UM82152 and 82385 Cache Control Modes. The block diagrams and the required IC list for each system configuration is illustrated in Figures 1,2, and 3 .

A software driver is required to initiate the UM82152 when the system is working in UM82152 Cache Control Mode. A PAL equation is needed to implement the HEAT chip set working in INTEL 82385 Cache Control Mode. Either or both of these tools can be requested from UMC's worldwide sales offices.

V Remarks

Throughout HEAT documents,a "*" will be attached to specific pin name if it's active low, CLK2* ,for example.

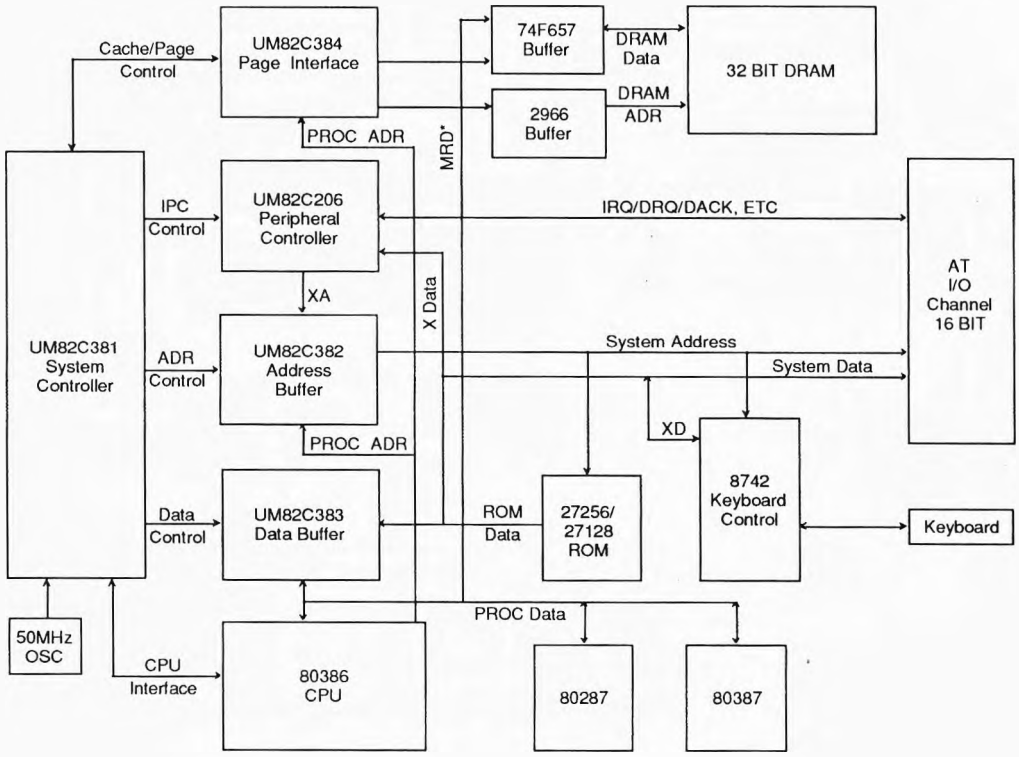

Figure 1. HEAT Chip Set System Diagram (Page Mode)

Required IC List:

80386	x1	80387	x1	
UM82C206	x1	27256	x2	
UM82C381	X1	AM2966	x4	
UM82C382	x1	74F657	x4	
UM82C383	x1	74F04	x1	
UM82C384	x1	74C04	x1	
8042	x1	7406	x1	

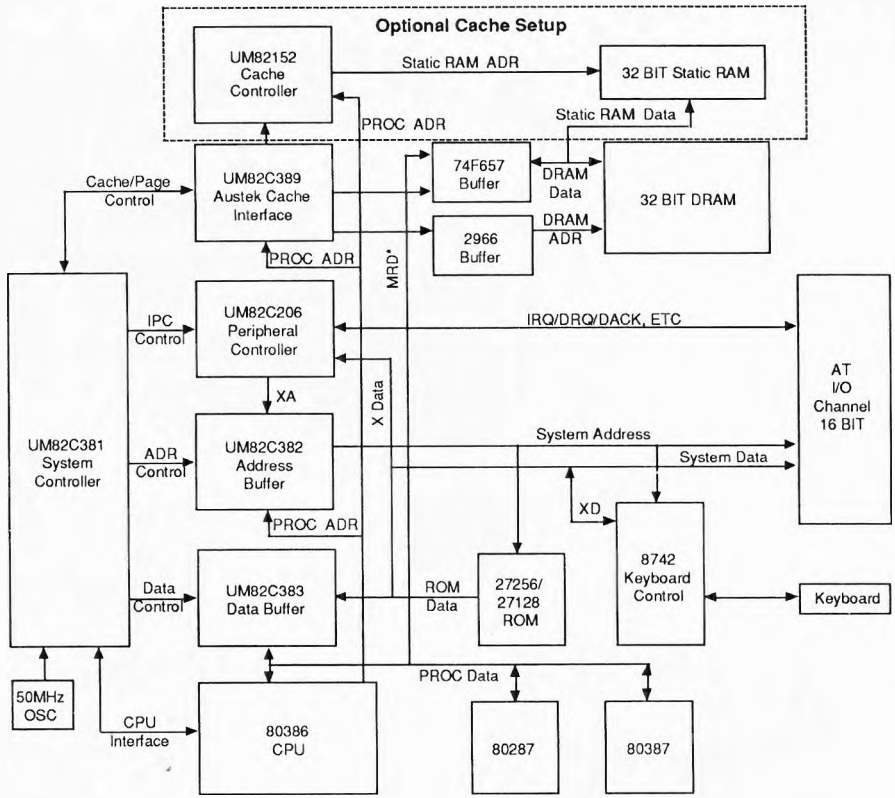

Figure 2. HEAT Chip Set System Diagram (Cache Mode with UM82152)

Required IC List:

80386	x1	UM82152	x1	74F657	
UM82C206	x1	8Kx8-25	x4	74F04	x1
UM82C381	x1	8042	x1	74C04	x1
UM82C382	x1	80387	x1	7406	x1
UM82C383	x1	27256	x2	*74F74	x1
UM82C389	x1	AM2966	x4	*74F258	x1
74F08	x1	74F74	x1		

*needed only when using 27256

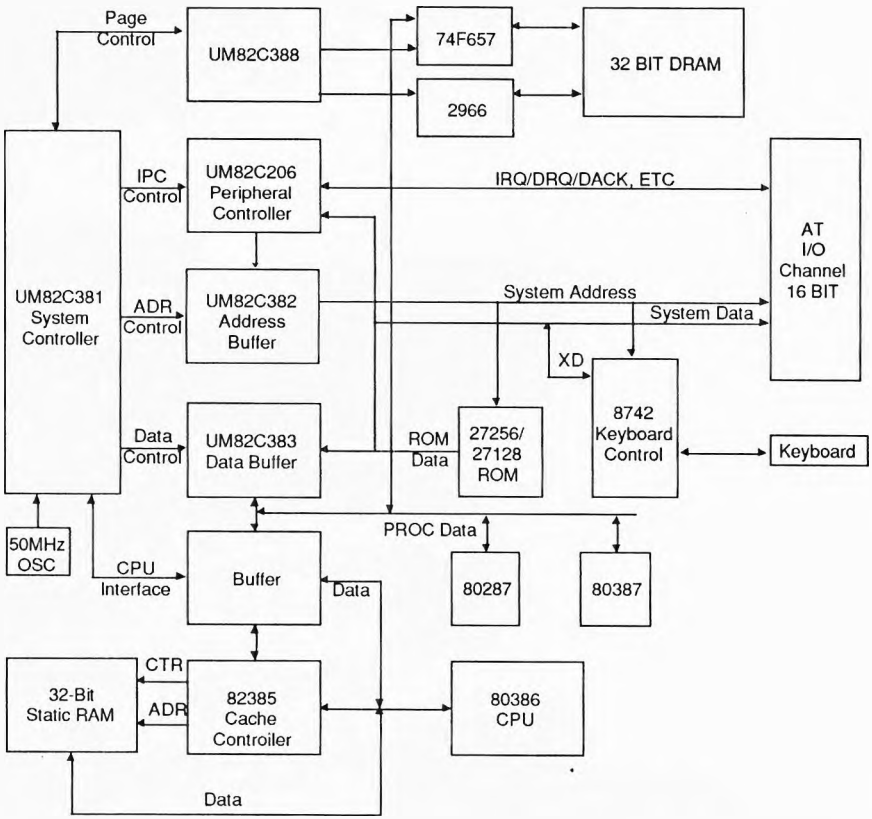

Figure 3. HEAT Chip Set System Diagram (Cache Mode with INTEL 82385)

Required IC List

80386	x1	82385	x1	74F04	x1
UM82C206	x1	4Kx4-25	x16	74C04	x1
UM82C381	x1	8042	x1	7406	x1
UM82C382	x1	27256	x2	74F74	x1
UM82C383	x1	AM2966	x4	74F646	x4
UM82C388	x1	74F657	x4	74F573	x2
74F08	x1	74F32	x1	18P8A	x1