1.0 INTRODUCTION TO THE OTI-051 SYSTEM CONTROLLER

OTI-051 is a custom integrated circuit designed for the OakHorizon chip set running with 80286 and 80386SX microprocessors. The chip provides all the system support logic for the system. It integrates all the functions of CPU interface and data flow control.

A summary of the special features provided by OTI-051 is listed below.

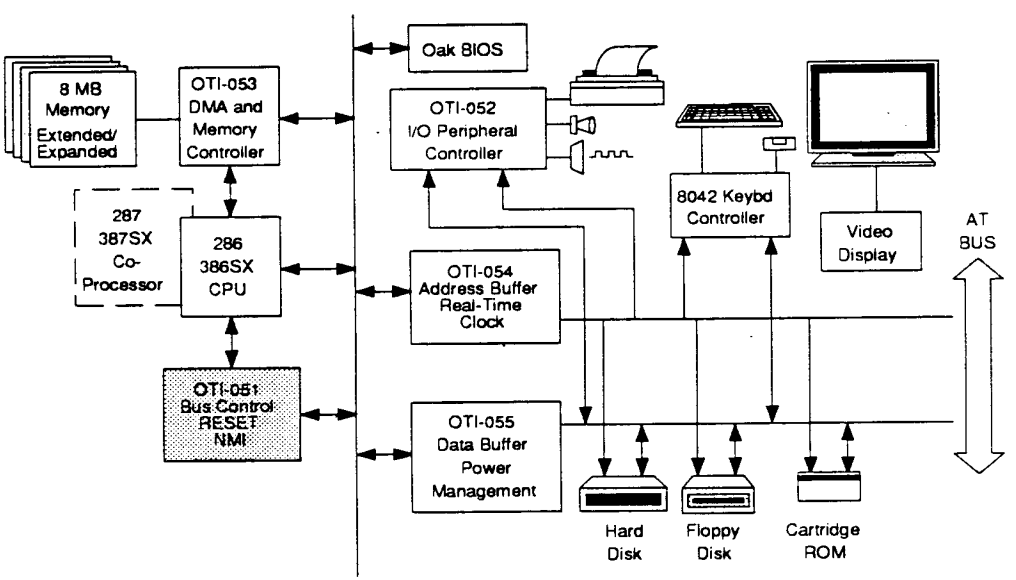
System Control: - Supports 8 MHz, 10 MHz, 12.5 MHz, 16 MHz and 20 MHz system speeds

I/O Channel:
- Asynchronous mode: 8 MHz independent of system speed
- Synchronous mode: 8, 10 or 12.5 MHz dependent on the system speed
- Programmable wait states

Laptop Support: - Power management scheme

Misc:
- Fast RESET
- Timeout Counter

System Block Diagram



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2.0 PIN-OUT ASSIGNMENT

Table 1. OTI-051 Pin Description

SYMBOL	PIN #	TYPE	NAME and FUNCTION
			***** CPU INTERFACE *****
SA23 - SA0	68-62,60-44	I	ADDRESS BUS: These are address bus lines corresponding to A23-A0 of the 80286/80386SX and 80287/80387SX bus. OTI-051 monitors these lines when the CPU or co-processor is in control of the bus.
SD15 - SD0	98-95,93-91 89-81	I/O	DATA BUS: These are the bidirectional data bus lines corresponding to D15-D0 of the 80286/80386SX CPU.
S0-/WR- S1-/DC	77 78	I	BUS CYCLE STATUS: These signals together with M/IO and COD/INTA- are used to decode different bus cycles.

80286 Bus Cycle Status Definition*

COD/INTA	M/IO	S1	S0	Bus Cycle Initiated
0 (Low)	0	0	0	Interrupt acknowledge
0	0	0	1	Will not occur
0	0	1	0	Will not occur
0	0	1	1	None; not a status cycle
0	1	0	0	IF A1=1 then halt; else shutdown
0	1	0	1	Memory data read
0	1	1	0	Memory data write
0	1	1	1	None; not a status signal
1 (High)	0	0	0	Will not occur
1	0	0	1	I/O read
1	0	1	0	I/O write
1	0	1	1	None; not a status cycle
1	1	0	0	Will not occur
1	1	0	1	Memory instruction read
1	1	1	0	Will not occur
1	1	1	1	None; not a status signal

80386SX Bus Cycle Status Definition*

M/IO	D/C#	W/R #	Bus Cycle Type	
0	0	0	Interrupt Acknowledge	
0	0	1	Will not occur	
0	1	0	I/O Data Read	
0	1	1	I/O Data Write	
1	0	0	Memory Code Read	
1	0	1	Halt: Address = 2 (BE0# 1 BE1# 1 BE2# 0 BE3# 1 A2-A31 0)	Shutdown Address = 1 (BE0# 0 BE1# 1 BE2# 1 BE3# 1 A2-A31 0)
1	1	0	Memory data read	
1	1	1	Memory data write	

* For more information on CPU bus cycle status, refer to the CPU databook.

M/IO-	79	I	MEMORY OR I/O CYCLE: is an input signal from the CPU indicating whether the present cycle is memory or I/O access.

Table 1. OTI-051 Pin Description (Continued)

SYMBOL	PIN #	TYPE	NAME and FUNCTION
SRDY-	80	I/O	SYSTEM READY: is an active low signal to acknowledge to the CPU that a data transfer for either memory or I/O is complete.
ADS-	76	I	ADDRESS STROBE: is an active low signal coming from 80386SX. This input is also used to detect the presence of a 80386SX.
			***** BUS INTERFACE *****
IORD-	26	I/O	I/O READ COMMAND: active low command to instruct the I/O device to drive its data onto the data bus. This pin becomes an input during the MASTER mode.
IOWR-	25	I/O	I/O WRITE COMMAND: active low command to instruct the I/O device to read the data present on the data bus. This pin becomes an input during the MASTER mode.
MEMRD-	28	I/O	MEMORY READ COMMAND: active low signal to instruct the memory subsystem to drive its data onto the data bus. This pin becomes an input during the MASTER mode.
MEMWR-	27	I/O	MEMORY WRITE COMMAND: active low signal to instruct the memory subsystem to store the data present on the data bus. This pin becomes an input during the MASTER mode.
INTA-	29	O	INTERRUPT ACKNOWLEDGE: is an active low signal to enable the interrupt controller's interrupt vector data onto the data bus by a sequence of interrupt acknowledge pulses issued by the CPU.
ALE	38	O	ADDRESS LATCH ENABLE: is an active high pulse signal during TS of any bus cycle including DMA and memory refresh cycle. The address should be latched using the ALE falling edge.
BHE-	42	I	BYTE HIGH ENABLE: is an active low signal used to enable data onto the most significant half of the data bus (D15 - D8). It is an input line when the CPU is in control.
GATEA20	40	I	GATE A20: is an active high signal from 8042 used to gate address A20.
A20	39	I/O	ADDRESS A20: is Address A20 line gated by GATEA20 from 8042 and the alternate A20 gate from port 92(Hex). This pin becomes an input during the MASTER mode.
A0	41	I/O	ADDRESS LINE 0: is the latched version of address 0. It is used along with BHE signal to distinguish the 8/16 bit and odd/even byte operation: **BHE- A0 OPERATION** 0 0 Word (D15 - D0) 0 1 Odd Byte (D15 - D8) 1 0 Even Byte (D7 - D0) 1 1 Not Used This pin becomes an input during the MASTER mode.
WS0-	7	I	ZERO WAIT STATE: is an active low signal indicating the present cycle can be completed without any wait state.
IOCS16-	8	I	16-BIT I/O CHIP SELECT: indicates to the system that the present data transfer is a 1 wait-state, 16-bit I/O cycle.
MEMCS16-	9	I	16-BIT MEMORY CHIP SELECT: indicates to the system that the present data transfer is a 1 wait-state, 16-bit memory cycle.

Table 1. OTI-051 Pin Description (Continued)

SYMBOL	PIN #	TYPE	NAME and FUNCTION
CMDEN-	20	O	COMMAND ENABLE: is an active low control signal to enable or disable the command buffer going to the I/O channel bus (PC bus). It is used to prevent bus contention between I/O devices that share the same address space resided in the X bus and in the I/O channel bus. CMDEN- is active if: 1. Non DMA, all I/O cycles except: 1.1 Floppy I/O if an on-board floppy is enabled. 1.2 Hard Disk I/O if an on-board hard disk controller is enabled. 1.3 Serial Com #1 if an on-board serial com. is enabled. 1.4 Parallel I/O if an on-board parallel port is enabled. 1.5 Video I/O if on-board video is enabled. 1.6 Co-processor I/O. 2. During DMA cycle. 3. During memory refresh cycle. 4. Non-DMA, PC memory cycle except: 4.1 On-board video is enabled and an on-board Video BIOS ROM has been specified. 4.2 On-board video is enabled and an on-board Video Memory has been specified.
PCDIR	21	O	PC DATA BUS DIRECTION: is the control signal to the data transceiver between the CPU and PC data bus: - PCDIR is high ==> the CPU drives the PC data bus (write cycle). - PCDIR is low ==> the PC drives the CPU data bus (read cycle). PCDIR is normally high. It becomes low when: 1. Interrupt acknowledge cycle. 2. Non DMA, memory read cycle. 3. Non DMA, I/O read cycle. 4. DMA, memory cycle.
PCENH-	22	O	PC DATA BYTE HIGH BUS ENABLE: is an active low control signal to enable the data buffer (D15 - D8) between the CPU and PC data bus. PCENH- is active if: 1. Non DMA, I/O odd byte write cycle, except co-processor I/O. 2. Non DMA, PC odd byte memory write cycle. 3. DMA, on-board odd byte system memory on either read or write cycle. 4. Interrupt acknowledge cycle. (INTA- active) 5. Non DMA, PC memory read cycle. (Neither ROM nor system memory is accessed) 6. Non DMA, I/O read cycle if those I/O are not in OTI-051, except co-processor I/O.
PCENL-	23	O	PC DATA BYTE LOW BUS ENABLE: is an active low control signal to enable the data buffer (D7 - D0) between the CPU and PC data bus. PCENL- is active if: 1. Non DMA, I/O even byte write cycle, except co-processor I/O. 2. Non DMA, PC even byte memory write cycle. 3. DMA, on-board even byte system memory on either read or write cycle. 4. Interrupt acknowledge cycle. (INTA- active) 5. Non DMA, PC memory read cycle. (Neither ROM nor system memory is accessed) 6. Non DMA, I/O read cycle if those I/O devices are not in OTI-051, except co-processor I/O.

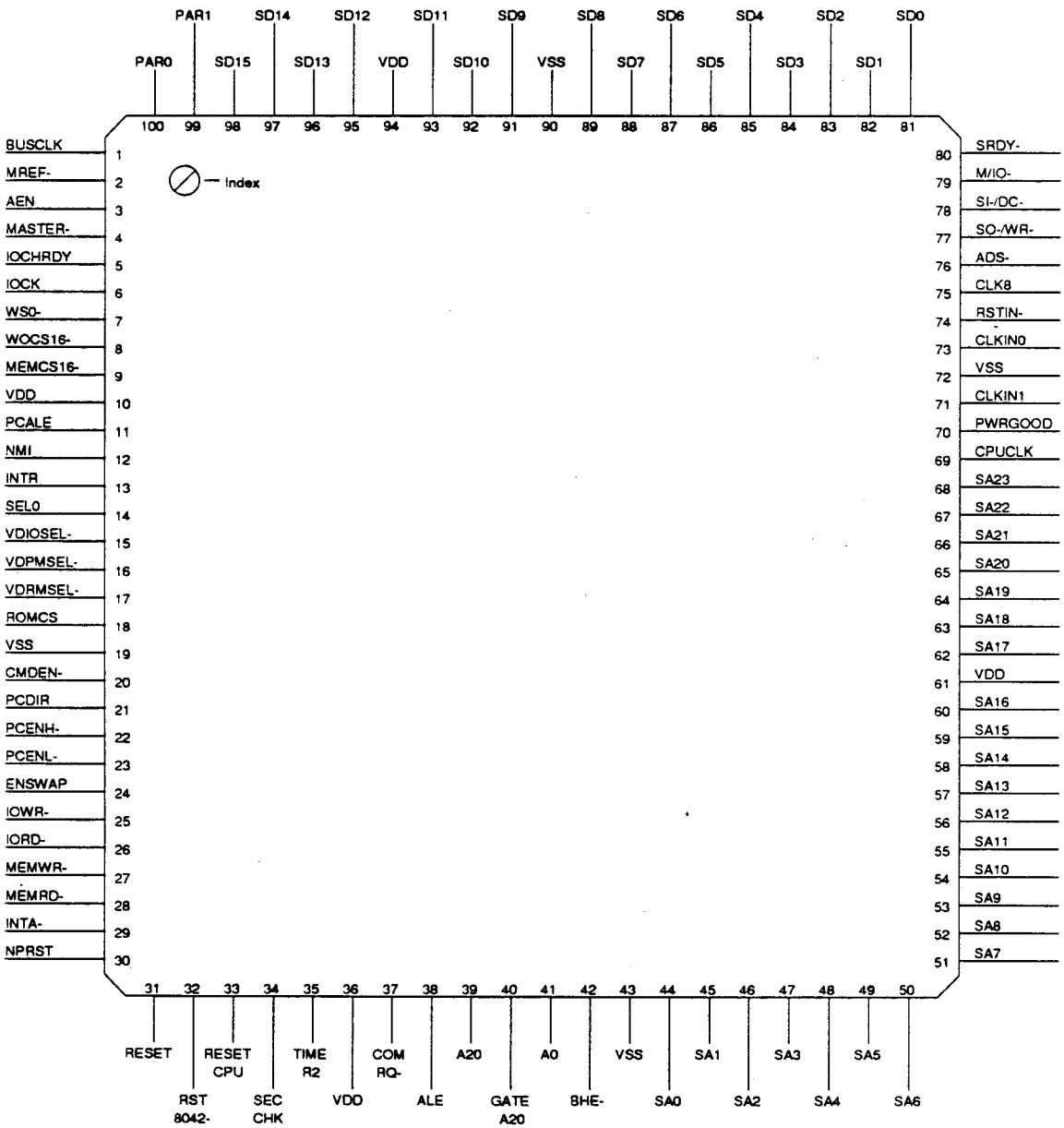
Table 1. OTI-051 Pin Description (Continued)

SYMBOL	PIN #	TYPE	NAME and FUNCTION
ENSWAP	24	O	ENABLE DATA SWAP: is an output to control the output enable of the data buffer for byte swap.
PCALE	11	O	PC ADDRESS LATCH ENABLE: is an active high pulse signal during TS of any bus cycle. It is similar to the ALE signal except during the DMA cycle this signal is active high throughout the cycle. It is synchronized to the 8 MHz BUSCLK.
IOCHRDY	5	I	I/O CHANNEL READY: is an active high ready signal from an I/O channel. Pulled low in active by a memory or I/O device to lengthen memory or I/O cycles. For every system clock cycle this signal is inactive, one wait state is added.
MASTER-	4	I	MASTER: this signal is used together with a DRQ line to gain control of the system.
MREF-	2	I	MEMORY REFRESH: is an active low signal indicating that a refresh cycle is going on. It is forced low when D/SRAM- is low to enable the self-refresh feature of the pseudo-static RAM during the SHUTDOWN mode.
AEN	3	I	ADDRESS ENABLE: is an active high signal during the DMA cycle to degate the I/O devices from the I/O channel to allow DMA transfers to take place.
SEL0	14	O	SELECT FUNCTION 0: is the special select status signal decoder for address range at the current cycle: **SEL0** — **FUNCTION** 0 — Nothing selected 1 — A15 - A10 = 0 (I/O)
VDIOSEL-	15	O	VIDEO I/O CHIP SELECT: is the active low chip select signal for on-board video I/O address space.
VDPMSEL-	16	O	VIDEO ROM CHIP SELECT: is the active low chip select signal for on-board video ROM address space.
VDRMSEL-	17	O	VIDEO RAM CHIP SELECT: is the active low chip select signal for on-board video RAM address space.
			***** SYSTEM INTERFACE *****
CLKIN0	73	I	CLOCK INPUT 0: is a 32 MHz TTL clock input with 50% duty cycle. It is used for: the system clock generation with the CPU running at 8 or 16 MHz, internal DMA control and memory refresh time.
CLKIN1	71	I	CLOCK INPUT 1: is an optional 25 or 40 MHz TTL clock input with 50% duty cycle. It is used for system clock generation with the CPU running at 10, 12.5 or 20 MHz.
BUSCLK	1	O	PC-BUS CLOCK: is a MOS driven clock signal for 80287 and the I/O channel. It has a 50% duty cycle.
CPUCLK	69	O	CPU CLOCK: is a 50% duty cycle MOS driven clock signal to the CPU. The frequency is programmable through I/O port 0019(Hex).
CLK8	75	O	8 MHz CLOCK: is a 50% duty cycle 8 MHz MOS driven clock signal to the memory controller for memory and refresh timing. It is also used by the 8042 keyboard controller.
RSTIN-	74	I	RESET INPUT: is an active low signal generated from the external RESET switch together with the RC circuitry. OTI-051 provides a Schmitt triggered input.

Table 1. OTI-051 Pin Description (Continued)

SYMBOL	PIN #	TYPE	NAME and FUNCTION
PWRGOOD	70	I	POWER GOOD: PWRGOOD comes from a power supply to indicate that power is stable. The signal is inactive if an under voltage condition occurs. The PWRGOOD signal has a turn-on delay that is in between 100 ms and 500 ms. OTI-051 provides a Schmitt trigger input for POWERGOOD.
RST8042-	32	I	RESET FROM 8042: is an active low signal from 8042 to reset the CPU.
RESET	31	O	RESET: is an active high signal synchronized to the system clock to reset the system.
RESETCPU	33	O	RESET CPU: is an active high output to reset the CPU.
NPRST	30	O	CO-PROCESSOR RESET: is an active high signal to reset the numerical co-processor.
			***** MISCELLANEOUS *****
PAR0 PAR1	100 99	I/O	PARITY BIT (0 - 1): are the memory (odd type) parity bits for even and odd bytes of the memory bank. Each parity bit is generated and written during the memory write operation. Each is checked and reported as an error to the system at the end of the memory read cycle. PAR0 is the memory parity bit for an even byte, PAR1 is the memory parity bit for an odd byte.
COMRQ-	37	I/O	COMMAND REQUEST: active low bidirectional signal. In the output phase, it sends a signal to OTI-053 indicating when to wakeup from the SHUTDOWN mode. In the input phase, it receives a request from OTI-053 to generate the PC memory cycle. The signal is in the output phase when AEN is HIGH and is in the input phase during other times.
IOCK	6	I/O	CHANNEL CHECK: part of port 61(Hex). An I/O channel condition will be reported to the CPU when this port is read.
TIMER2	35	I	TIMER 2 OUTPUT: status signal on 8254 timer channel 2. This signal comes from OTI-052.
NMI	12	O	NON-MASKABLE INTERRUPT: is an active high signal to the CPU indicating that an error has occurred in one of the following areas: - memory parity error - I/O channel check signal from the PC bus.
INTR	13	I	INTERRUPT: interrupt request from OTI-052 interrupt controller.
ROMCS	18	O	ROM CHIP SELECT: is an active low signal used to enable the ROM BIOS to output data on to the data bus.
SECCHK	34	I	SECURITY CHECK: is an active high input coming from the on-board jumper. Security check is enabled if this input is high. PS/2 compatible feature.
VDD	10,36,61,94		POWER: +5 V supply. 4 pins
VSS	19,43,72,90		GROUND: 4 pins

NOTE: OTI-051 would go into TEST mode under the following input pin combination: RSTIN-, PWRGOOD, MASTER - all at logic 0.



3.0 OTI-051 FUNCTIONAL DESCRIPTION

OTI-051 functions can be categorized as follows:

1. Command Cycle Control
2. Address and Data Path
3. Clock Generator and Reset Control
4. Memory and I/O Decoder and Buffer Control
5. System Ready Generator
6. Power Management
7. Miscellaneous
8. System Control and Status Registers

3.1 Command Cycle Control

Command Cycle Control contains a state machine that generates the CPU cycles:

- Memory Read/Write Cycle if memory access is outside of on-board system memory.
- I/O Read/Write Cycle.
- Interrupt Acknowledge Cycle.
- ROM BIOS Read Cycle.

In addition to these functions, Command Cycle Control also generates the ALE signal when it detects a change on the CPU Status lines: S0 - S1 and M/IO at TS time to mark the beginning of the CPU cycle.

The Command Cycle Control can be clocked by two different clock sources. Two different timing modes can be selected by programming indexed port 03(Hex). In the Synchronous mode, SYSCLK is used. The state machine is either clocked by CPUCLK/2 or CPUCLK/4. If indexed port 03(Hex) bit 0 (SPD0) is 1, then CPUCLK/4 is used. If SPD0 is 0, then CPUCLK/2 is used.

In the asynchronous mode, BUSCLK is used. The state machine would always be running at BUSCLK speed, independent of the CPU speed. In this mode, a very high speed CPU can be used and the system can still maintain AT-compatible bus timing. The command pulse width and command recovery time is independent of CPU speed. PCALE is synchronized to the 50% duty cycle BUSCLK on the PC-BUS. Commands are synchronized to the bus clock. The minimum command length and recovery time is referenced to BUSCLK.

In either mode, the command width and command recovery time can be adjusted by programming indexed port 01(Hex) for PC memory and indexed port 02(Hex) for I/O cycles.

3.1.1 Memory Read/Write Cycle

The state machine samples the CMDRQ- signal from the System Memory Control section at the end of the TS cycle. If the memory being accessed does not reside in either system memory or the EMS/Extended memory area, CMDRQ- is asserted. MRD- or MWR- command is active during the TC cycle. Normal command length is five 8 MHz clocks, but the user can program the speed control register (indexed port 03(Hex)) to reduce the command length to three 8 MHz clocks for fast PC- memory cycles.

If IOCHRDY is asserted low, the command will be extended. The command is terminated three 8 MHz clocks minimum after the IOCHRDY is asserted high.

If the current cycle is a 16 bit memory operation to 8 bit memory devices, the state machine performs a double memory cycle operation with the first cycle accessing the low byte (A0 is low) and the second cycle accessing the high byte (A0 is high). From the end of the first cycle to the beginning of the second cycle (i.e. RECOVERY TIME) is three 8 MHz clocks. For a memory read cycle, the low byte of data is stored and outputted to the CPU bus at the second cycle along with the high byte. If MEMCS16- is low and the current cycle is a 16 bit memory operation, then no double cycle is generated. The memory cycle would also be a 1 wait state command cycle.

PC Memory Wait State Control Register:Indexed Port 0001(Hex) R/W:

Bit	Function		
7-6	Additional Wait States for Memory Command width		
	bit 7	bit 6	
	1	1	3 additional wait states
	1	0	2 additional wait states
	0	1	1 additional wait state
	0	0	no additional wait state
5-4	Additional Wait States before Memory Command starts		
	bit 5	bit 4	
	1	1	3 additional wait states
	1	0	2 additional wait states
	0	1	1 additional wait state
	0	0	no additional wait state
3	FAST: for fast PC Memory command cycles. 0 - normal PC memory command width with number of wait states as programmed in bits 7 and 6 1 - normal PC memory command width as programmed in bits 7 and 6 minus 3 wait states		
2-0	Not used, read as 000.		

At Power On or Reset, the content of indexed port 01(Hex) is 00(Hex).

3.1.2 I/O Read/Write Cycle

The state machine generates and provides the timing for every I/O cycle. During the I/O cycle, the IORD- or IOWR- commands are asserted at the beginning of TC. Command length is fixed at five 8 MHz clocks and recovery time at three 8 MHz clocks.

If IOCHRDY is asserted low, the command will be extended. The command will be terminated three 8 MHz clocks minimum after the IOCHRDY is asserted high.

Similar to memory commands, if the current cycle is a 16 bit I/O operation to 8 bit I/O devices, the state machine will perform a double cycle with a recovery time of three 8 MHz clocks.

However, if IOCS16- is low, no double cycle will be generated, and the current cycle is a 1 wait state command cycle.

I/O Command Wait State Control Register: Indexed Port 0002(Hex) R/W:

Bit	Function		
7-6	Additional Wait States for I/O Command width		
	bit 7	bit 6	
	1	1	3 additional wait states
	1	0	2 additional wait states
	0	1	1 additional wait state
	0	0	no additional wait state
5-4	Additional Wait States before I/O Command starts		
	bit 5	bit 4	
	1	1	3 additional wait states
	1	0	2 additional wait states
	0	1	1 additional wait state
	0	0	no additional wait state
3-0	Not used, read as 0000.		

At Power On or Reset, the content of indexed port 02(Hex) is 00(Hex).

3.1.3 Interrupt Acknowledge Cycle

Two consecutive cycles of interrupt acknowledge (INTA-) are generated to an interrupt controller in response to an interrupt signal to the CPU. During the first cycle, the interrupt controller resolves the priority if there is more than one interrupt pending. In the second cycle, the interrupt controller outputs onto the 8 bit data bus (D0 - D7) the interrupt vector address pointing to the interrupt routine table. INTA- is asserted at the beginning of TC. IOCHRDY can also extend the duration of the cycle. The cycle will be terminated 3 clocks minimum after IOCHRDY is asserted high. The minimum period (if IOCHRDY is always high) of INTA- is two 8 MHz clocks. BUS HOLD Request to the CPU is blocked between the two INTA- cycles to assure the execution of the second INTA- cycle.

3.1.4 ROM BIOS Read Cycle

The state machine generates the MRD- command if there is a memory access between 0E0000 and 0FFFFF memory space. MRD- is asserted at the middle of TS with 1-4 user programmable wait states. The user can select shadow ROM implementation for zero wait state ROM cycles.

Memory Wait State Control Register: Indexed Port 001B(Hex) W/R:

Bit	Function		
7-4	CROM & PSRAM Control		
3-2	Number of Wait states in ROM cycle		
	bit 3	bit 2	
	1	1	4 wait states
	1	0	3 wait states
	0	1	2 wait states
	0	0	1 wait state
1	Enable/Disable - Page Mode Memory Cycle.		
0	Not Used		

At Power On or Reset, the content of indexed port 1B(Hex) is 0D(Hex).

3.2 Address and Data Path

OTI-051 is connected directly to the address and data bus of the CPU. OTI-051 latches the address bus internally to form an address bus LA(0-23). The CPU data bus is connected to the transceiver internally to form the 16 bit data bus: LD(0-15).

- SA to LA during CPU or Coprocessor access time.
- 8 bit data registers, both input and output are connected to LD(0-7). It is used to latch the read data from an 8 bit device at the first cycle of a 16 bit operation.
- 8 bit data transceiver connected between LD(0-7) and LD(8-15). It is used to swap the data path between the low byte and high byte to access to an 8 bit internal device. During a 16 bit operation to a 16 bit device, this transceiver is disabled.

If an 80286 is used, ALE is generated during the 2nd phase of TS. If an 80386SX is used, ALE is generated at the 1st phase of TS. ALE is active high and the pulse width is one CPUCLK. (one phase)

3.3 Clock Generator and Reset Control

3.3.1 Clock Generator

OTI-051 supports system speeds ranging from 8 MHz, 10 MHz, 12.5 MHz, 16 MHz and up to 20 MHz.

Two clock inputs are available for users:
CLKIN0: 32 MHz
CLKIN1: 25 MHz, 40 MHz

CLKIN0 is required. OTI-051 uses CLKIN0 to derive the 8 MHz internal clock for asynchronous bus timing and CPU power save mode. It also uses CLKIN0 for 16 MHz system operation. CLKIN1 is optional. The user can input a 25 MHz clock for 12.5 MHz system operation, or a 40 MHz clock for 10 MHz or 20 MHz system operation. During power-up, the system defaults to 8 MHz operation. Different clock inputs and system speeds can be selected by programming indexed port 03(Hex).

The Clock Generator provides clocks to the CPU, Memory Controller, DMA controller, and the rest of the system. It can be broken down to 2 blocks based on their functions:

- Multiplexer and Deglitching Circuit based on CLKIN0, and the presence of CLKIN1.
- Dividers: by 2, by 4 or by 8.

The Speed Control Register is an indexed I/O port used to change the speed of the CPU clock.

OTI-051 also generates an 8 MHz 50% duty cycle clock output. This clock is used by OTI-053 for memory refresh timing and RAS pulse width timing. The 8042 keyboard controller also uses this clock signal.

3.3.2 Reset Control

There are several conditions that will generate a system reset:

- At power on, the power supply provides a POWERGOOD signal. It indicates proper operation of the power supply and gives advance warning when power is turned off.
- At reset switch, RSTIN-, an active low pulse signal. OTI-051 provides a Schmitt trigger input so that an RC circuit can be used to establish a reset pulse of proper duration.
- At mode switching from Protected Mode to Real Mode by writing to either port 64(Hex) or port 92(Hex) for a fast reset. Only the CPU is reset in this case and no system reset is issued.
- When the CPU executes a shutdown instruction. Only the CPU is reset in this case and no system reset is issued.

During a system reset, OTI-051 generates an active high pulse signal synchronized to the CPUCLK to reset the CPU and system.

During a CPU reset, OTI-051 only generates a RESET signal to the CPU but not to the system. The RESET signal generated is active for the number of clocks to satisfy the requirements of the CPU. During system reset, OTI-051 also generates NPRST to reset the co-processor. OTI-051 also responds to the I/O WRITE instruction to port F1(Hex). When port F1 is written to with 00, NPRST is generated.

Depending on the type of co-processor installed, the NPRST would remain active for the appropriate number of clocks to reset the co-processor.

3.4 Memory and I/O Decoder and Buffer Control

This section provides the decoder for the devices on the memory and I/O spaces in the system and also internal and external buffer enable and direction controls for memory and I/O channels (PC). It also generates a status signal (e.g. SEL0 to OTI-052) as the address range status information for OTI-052 to control and enable the current cycle:

SEL0	FUNCTION
0	Not used [1]
1	A15 - A10 = 0 (I/O) [2]

Note:
1. A15 - A10 during a CPU I/O cycle (DMA cycle is not included) are not 0's or
2. A15 - A10 during a CPU I/O cycle (DMA cycle is not included) are 0's

3.5 System Ready Generator

System Ready will be active only at the end of the CPU or co-processor cycle. There are 2 sources that generate a system ready to the CPU to end the cycle:

- Memory Control if the access is in the system or EMS memory range. System ready will be generated during TC and ended at TS or TI time for a period of 1 system clock.
- Command Generator that generates the cycle besides the system memory. System ready will be generated at the rising edge of the last TC and ended at the rising edge of TS or TI time for a period of 1 system clock.
- During the co-processor I/O cycle, OTI-051 generates SRDY- to terminate the I/O cycle.

3.6 Power Management

Three modes of power saving operations:

SHUTDOWN Mode - CPU clock is stopped, OTI-053 takes over the bus. OTI-053 generates REFRESH CYCLES. DMA requests are blocked.

SLEEP Mode - CPU is running at 2 MHz, OTI-053 takes over the bus. OTI-053 generates REFRESH CYCLES. DMA requests are blocked. When the system wakes up, the CPU continues to run without reset.

SLOW Mode - CPU runs at 4 MHz and DMA and REFRESH cycles are served in the same manner as in normal system speed.

The 3 different CPU power-off modes can be selected by programming indexed port 03(Hex). The CPU can be awakened from the SHUTDOWN or SLEEP mode through an interrupt (INTR) from the interrupt controller. Once OTI-051 receives the INTR signal, it activates the CMDRQ- signal to OTI-053 indicating that it is time to release the HOLD signal to the CPU.

3.7 Miscellaneous

3.7.1 Memory Parity Check and Generation

Memory parity is generated by OTI-051 during a system memory write. During a system memory read, OTI-051 also checks the parity bit against the memory data. The parity error information is latched into port 61(Hex).

3.7.2 Timeout Counter

A 16-bit counter is provided for the implementation of a watchdog timer. The user can program the counter to determine how long one wants to wait for any cycle to finish before terminating the cycle. When the maximum count is reached, OTI-051 will terminate the present cycle automatically, generate an NMI, set indexed port 0E(Hex) bit 0 and latch the I/O address into port 0E(Hex). The timeout counter helps in preventing system hang when an I/O device is not functioning properly.

3.7.3 System Control and Status Registers

SYSCNLB: System Control Port B is an 8 bit I/O read/write port used to enable/disable the parity check, and some peripherals:

SYSCNLB: I/O Port 0061 R/W:

Bit	Function
7	R Memory parity check
6	R I/O Channel Check
5	R Timer 2 output
4	R Toggles with each memory refresh request on a read operation
3	R/W DIS/EN- IOCHCK signal. When set to 1, this bit disables IOCHCK from generating an NMI. When cleared to 0, an NMI is generated when IOCHCK goes active.
2	R/W DIS/EN- memory parity check. When set to 1, this bit disables parity error generation caused by system memory including the EMS memory from generating an NMI. When cleared to 0, an NMI is generated when a memory parity error is sensed.
1	R/W EN/DIS- Beeper Data output. This bit gates the output of timer 2. It is used to disable the timer's sound source or modify its output. When set to 1, this bit enables the output, and when cleared, it forces the output to zero.
0	R/W EN/DIS- Timer 2 Gate. This line is routed to the timer input at gate 2. When this bit is cleared to 0, the timer operation is halted. This bit and bit 1 control the operation of the timer's sound source.

At Power On or Reset, SYSCNTL = 00.

NMICTL: NMI Control Register is an 8 bit I/O write only port used to enable/disable an NMI to the CPU:

NMICTL: I/O Port 0070 W:

Bit	Function
7	DIS/EN- NMI to the CPU.
6-0	Not used. Reserved as 0's.

At Power On or Reset, NMICTL is set disabled (bit 7 = 1).

SYSCTLA: System Control Port A is an 8 bit I/O read and write port used to control the security lock and Gate A20.

SYSCNLA: I/O Port 0092 R/W:

Bit	Function
7-4	Reserved
3	Security Lock Latch
2	Reserved = 0
1	Alternate Gate A20
0	Reserved

At Power On or Reset, SYSCNLA reads as 00.

4.0 ELECTRICAL CHARACTERISTICS

4.1 A.C. Characteristics

A.C. Characteristics: TA=0 deg C to 70 deg C, VDD=5V+/-5%, VSS=0V

Table 2. AC Characteristics of OTI-051

SYMBOL	PARAMETER	MIN	MAX	UNIT	LOADING CAPACITANCE
t1	CLKIN0 Period	31		ns	
t1a	CLKIN0 HIGH Time	12		ns	
t1b	CLKIN0 LOW Time	12		ns	
t2	CLKIN1 Period	25		ns	
t2a	CLKIN1 HIGH Time	10		ns	
t2b	CLKIN1 LOW Time	10		ns	
t3	CPUCLK Period	25		ns	CL=70 pF
t3a	CPUCLK HIGH Time	10		ns	CL=70 pF
t3b	CPUCLK LOW Time	10		ns	CL=70 pF
t4	BUSCLK to PCALE		45	ns	CL=200 pF
t5	BUSCLK to COMMAND		35	ns	CL=50 pF
t6	Read Valid Data		100	ns	CL=100 pF
t7	COMMAND Pulse Width	650		ns	
t8	INTAN Pulse Width	310		ns	
t9	IOCHRDY from COMMAND Active		520	ns	
t10	IOCHRDY to COMMAND Inactive	240		ns	
t11	Read Data HOLD Time	10		ns	CL=100 pF
t12	LA Address from SA Address		25	ns	CL=100 pF
t13	IOCS16N SETUP Time	20		ns	
t14	IOCS16N, MEMCS16N HOLD Time		15	ns	
t15	IOCHRDY from I/O Active		20	ns	
t16	MEMCS16N SETUP Time	20		ns	
t17	IOCHRDY from MEMORY Active		35	ns	
t18	PC Address from PCALE		25	ns	CL=200 pF
t19	ALE from CPUCLK		25	ns	CL=20 pF
t20	PAR0, PAR1 from SD		35	ns	CL=100 pF
t21	SRDYN Active from CPUCLK		12	ns	CL=50 pF

Table 2. AC Characteristics (Continued)

SYMBOL	PARAMETER	MIN	MAX	UNIT	LOADING CAPACITANCE
t22	SRDYN Inactive from CPUCLK		35	ns	CL=50 pF
t23	PWRGOOD, RSTINN SETUP Time		20	ns	See Note
t24	RESET from CPUCLK		20	ns	CL=200 pF
t25	RESETCPU from CPUCLK		10	ns	CL=20 pF
t26	NPRST from CPUCLK		10	ns	CL=20 pF
t27	VDXXSELN Valid from ALE		50	ns	CL=100 pF
t28	ROMCSN Valid from ALE		50	ns	CL=20 pF
t29	A20 Valid from SA20		20	ns	CL=30 pF
t30	A0 Valid from SA0		25	ns	CL=30 pF
t31	SEL0 Valid to COMMAND	45		ns	CL=15 pF
t32	PCDIR Valid from S1 & S0		45	ns	CL=15 pF
t33	PCDIR Inactive from BUSCLK		35	ns	CL=15 pF
t34	PCENHN, PCENLN, ENSWAP Active from Read COMMAND		20	ns	CL=15 pF
t35	PCENHN, PCENLN, ENSWAP Inactive from BUSCLK		35	ns	CL=15 pF
t36	PCENHN, PCENLN, ENSWAP Active from COMRQN during Write		50	ns	CL=15 pF

NOTE: SETUP time is only for testing purposes.

4.2 D.C. Characteristics

D.C. Characteristics: TA=0 deg C to 70 deg C,VDD=5V+/-5%,VSS=0V

Table 3. DC Characteristics of OTI-051

SYMBOL	PARAMETER	MIN	MAX	UNIT	CONDITION
VOH	Output HIGH Voltage	2.4		V	IOH=400 µA
VOL1	Output LOW Voltage		0.45	V	IOL=20 mA, Note 1
VOL2	Output LOW Voltage		0.45	V	IOL=16 mA, Note 1
VOL3	Output LOW Voltage		0.45	V	IOL=10 mA, Note 1
VOL4	Output LOW Voltage		0.45	V	IOL= 8 mA, Note 1
VOL5	Output LOW Voltage		0.45	V	IOL= 4 mA, Note 1
VOL6	Output LOW Voltage		0.45	V	IOL= 2 mA, Note 1
VIH	Input HIGH Voltage	2.0	VDD+0.5	V	TTL
VIL	Input LOW Voltage	- 0.5	0.8	V	TTL
VIS	Schmitt Input HIGH	2.4	VDD+0.5	V	Schmitt, Note 2
ILI	Input Leakage Current	- 10	10	µA	
OLI	Output Leakage Current	- 10	10	µA	
ICC	Operating Supply Current		30	mA	Input=VDD or VSS No Output Load
CI	Input Capacitance		8	pF	
CO	Output Capacitance		8	pF	
CIO	I/O Capacitance		16	pF	

NOTES:

1. Output Current (IOL) Capabilities:

20 mA:	PCALE, RESET
14 mA:	CPUCLK
8 mA:	A20, A0, SRDYN, PAR0, PAR1
4 mA:	BUSCLK, VDIOSELN, VDPMSELN, VDRMSELN, ROMCSN, IOWRN, IORDN, MEMWRN, MEMRDN, CLK8, SD0-SD15
2 mA:	NMI, SEL0, CMDENN, PCDIR, PCENHN, PCENLN, ENSWAP, RESETCPU, ALE, COMRQN

2. Input Structures:

Schmitt triggered:	PWRGOOD, RSTINN
TTL:	all others
Input with pullup:	BHEN, S0, S1, MIO, SRDYN, SD0-15

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5.0 OTI-051 TIMING DIAGRAMS

FIGURE 1-1

8 BIT PC CYCLE TIMING DIAGRAM

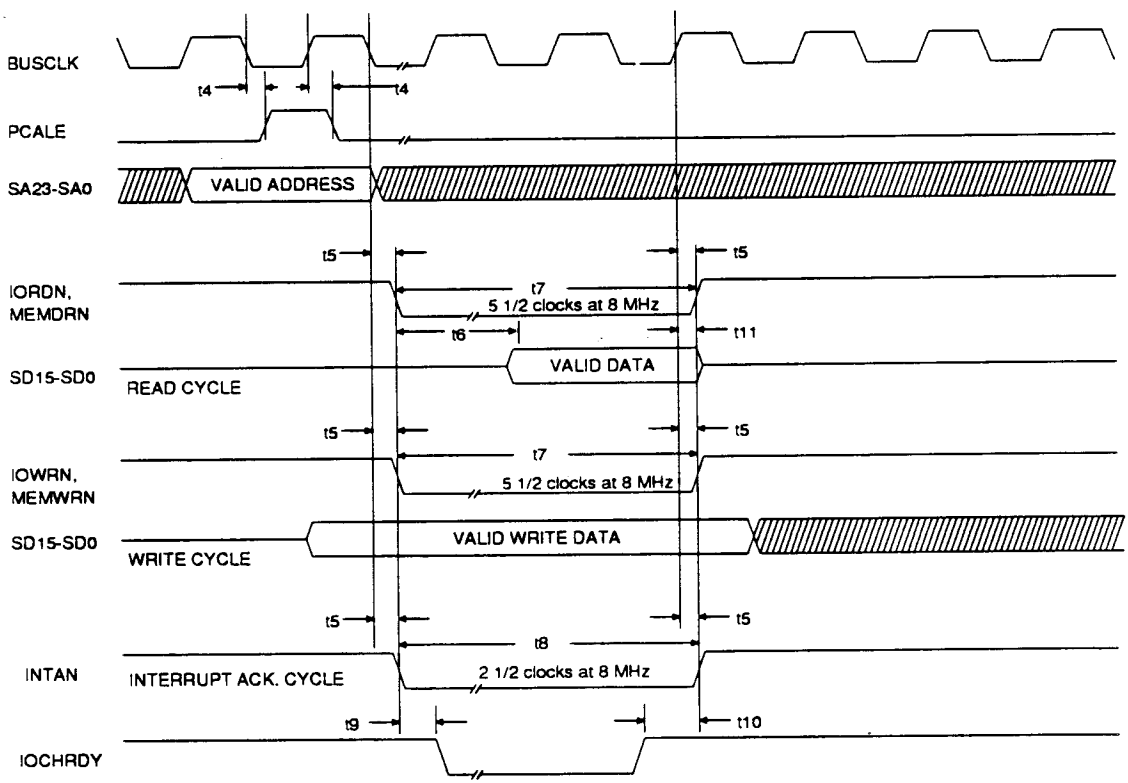


FIGURE 1-2

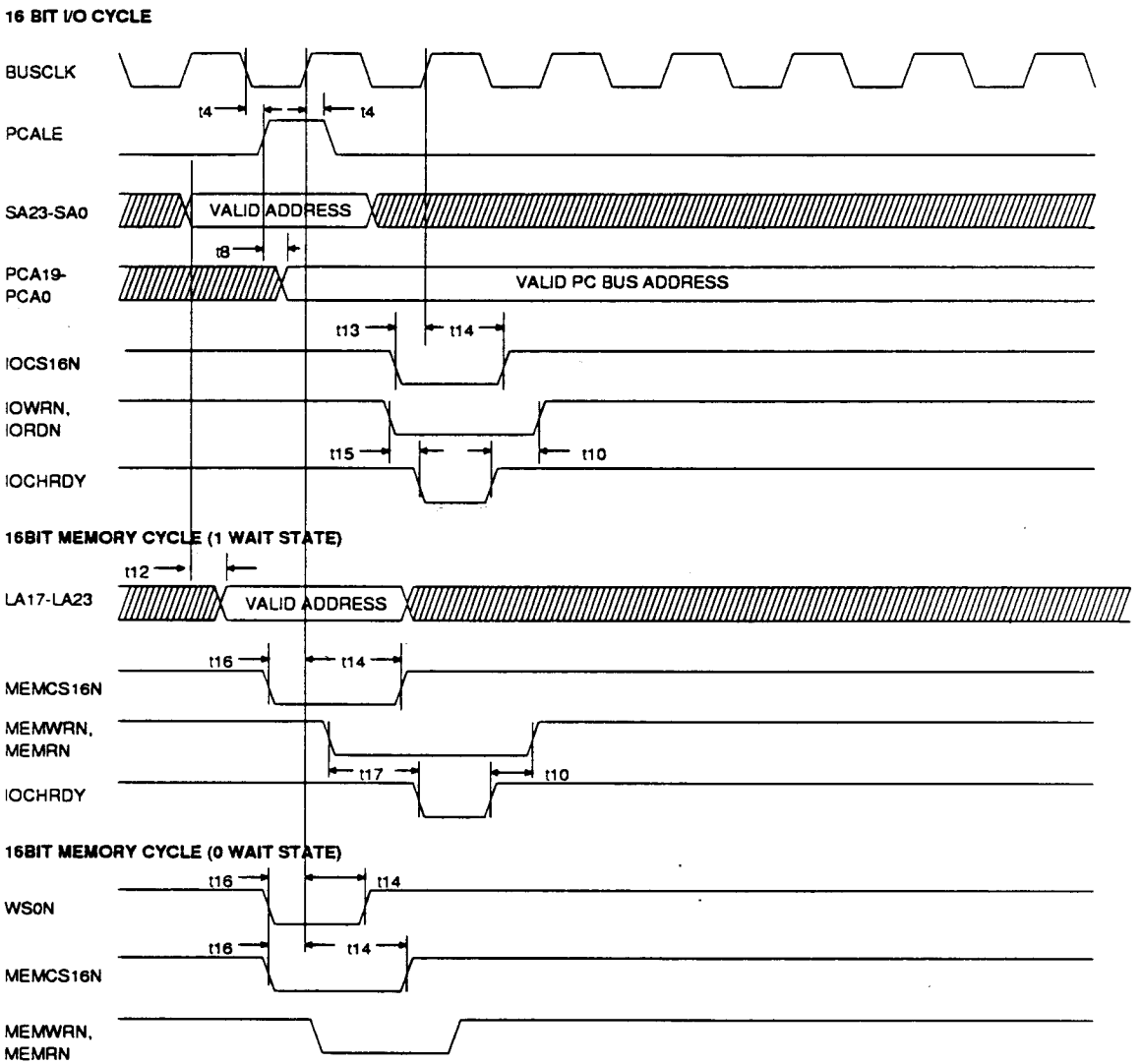
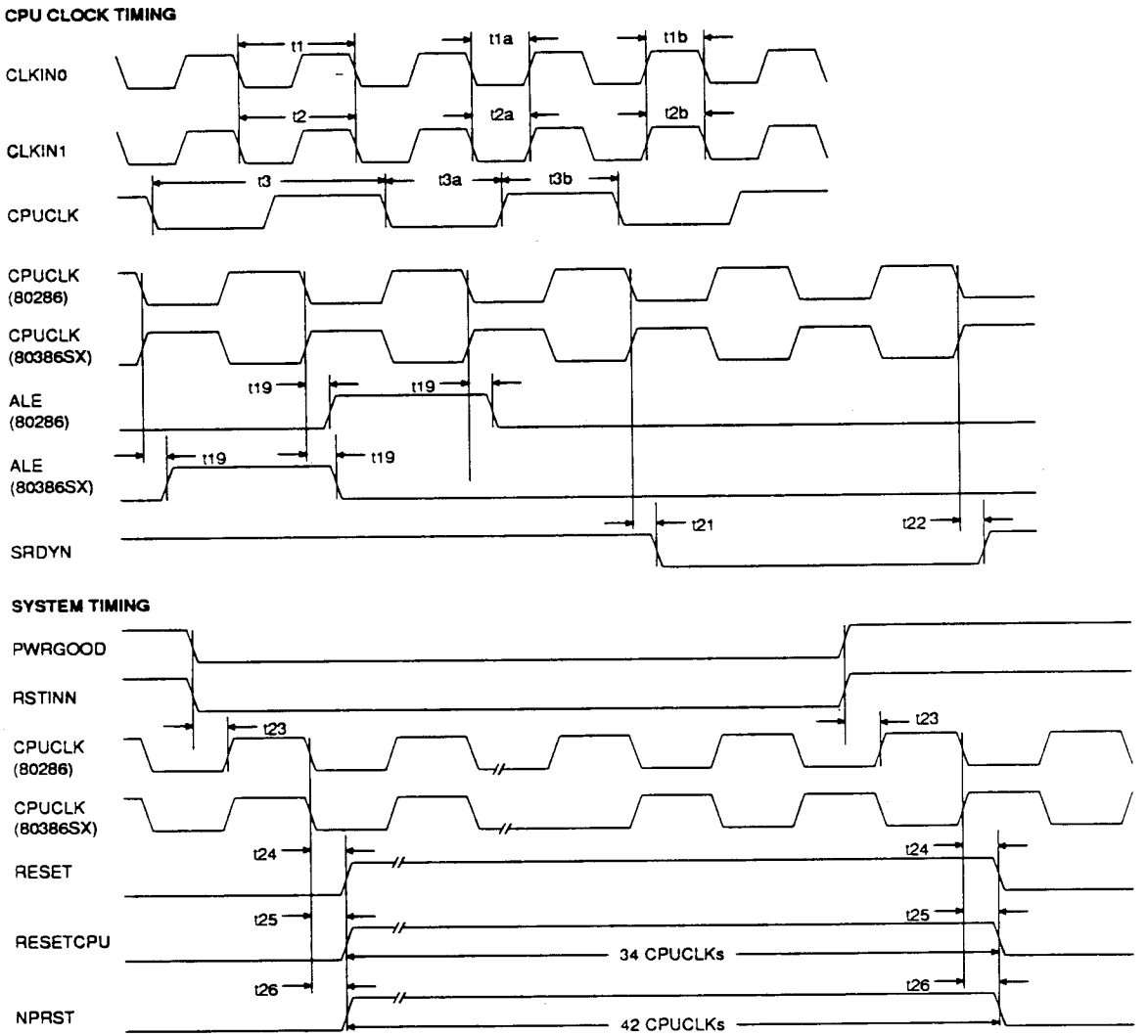
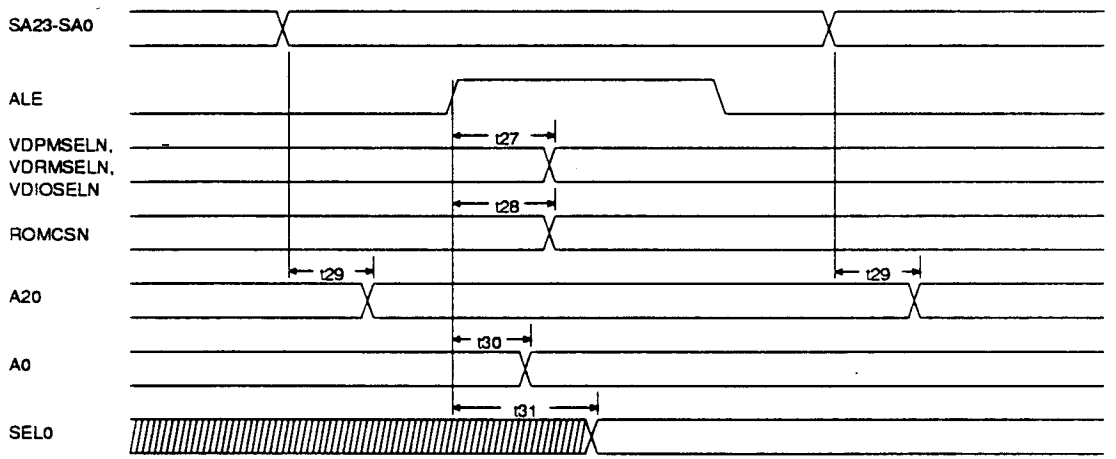


FIGURE 1-3

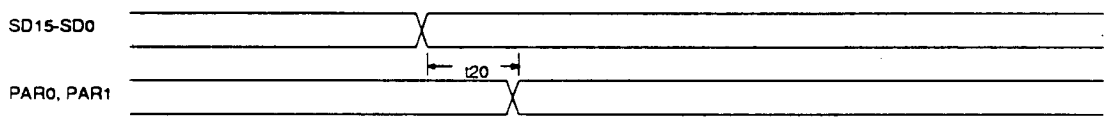


FIGURES 1-4 & 1-5

ADDRESS & CHIP SELECT TIMING



PARITY GENERATION TIMING



COMMAND & DATA BUFFER CONTROL TIMING