COUGAR II 82C491/82C493
i486 DIRECT MAPPED CACHE "AT" CHIP SET
(25, 33 and 50MHz Timing Spec included)

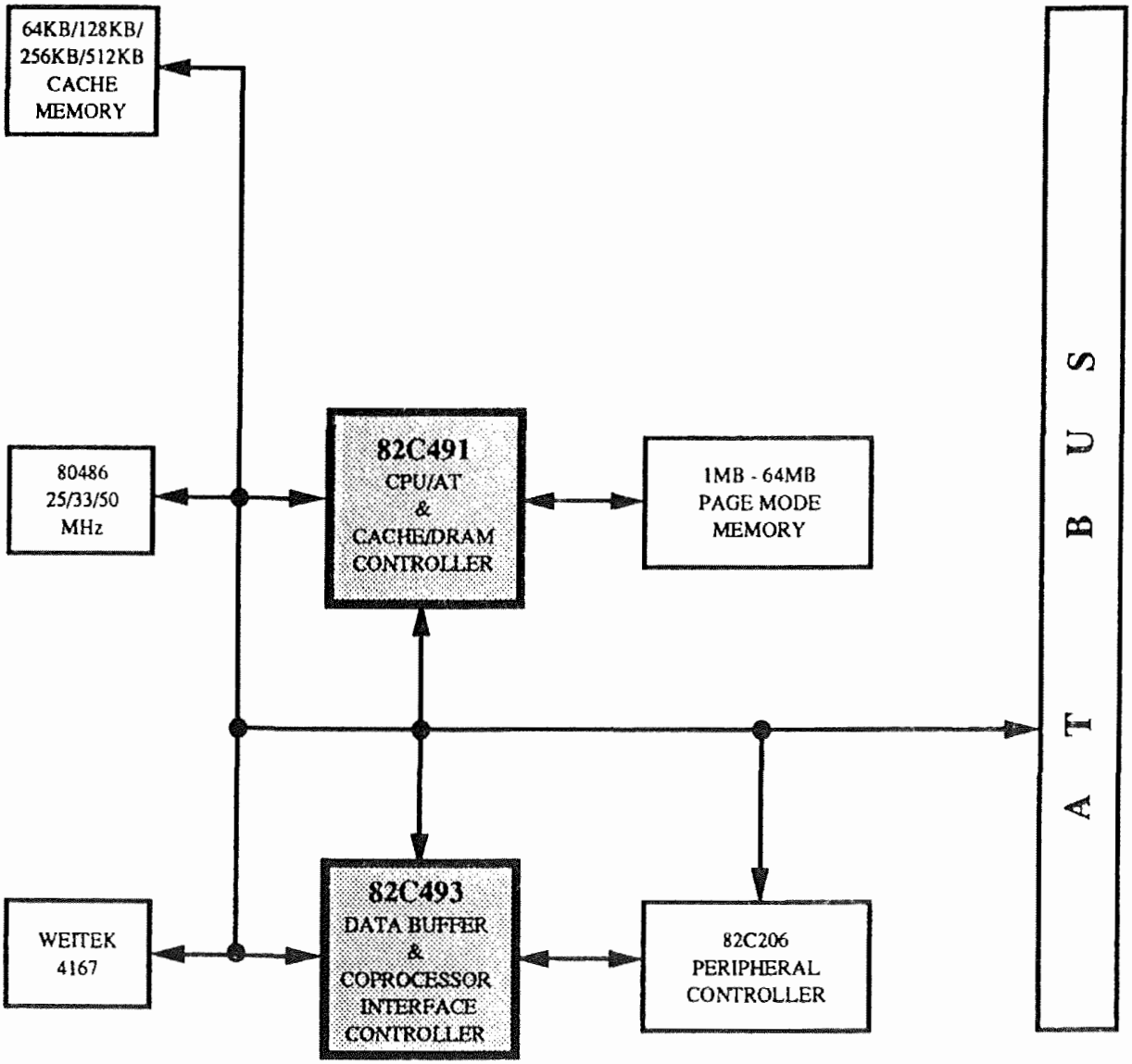
* 100% IBM PC/AT Compatible
* Designed to work at 25, 33 and 50MHz on a 486 based system
* Flexible architecture to support 64KB, 128KB, 256KB and 512KB Burst Mode Cache Subsystems
* Secondary Cache Support Logic on Chip
* Up to 64MB DRAM memory support with Page Mode
* Unlimitted DRAM configurations - Mixing 256K, 1M and 4M devices
* Shadow RAM and 256KB Memory Remapping
* Software Programmable DRAM Wait States
* Single Phase Clock Scheme
* Four blocks of non-cacheable memory area
* Fast Reset and Gate A20 to optimize OS/2
* Support Port 92 Fast Gate A20
* Synchronous AT Bus Clock Generation
* Weitek 4167 Coprocessor support
* Concurrent Refresh and AT Refresh Option
* Software Turbo Clock Switching
* Less than 20 components plus memory to implement an AT/486 system
* 1.0 Micron Low Power, High Speed CMOS Technology

The COUGAR II Chip Set provides high integration and a low cost solution for a 25, 33, 50MHz 486/AT based system design. Its flexible architecture allows Burst Mode Direct Mapped Cache Implementation with 64KB/128KB/256KB/512KB Cache. The COUGAR II Chip Set combined with 82C206 or compatible peripheral controller offer a 100% PC/AT compatible system using less than 20 components plus memory devices. The 82C491 and 82C493 are both available in the 160-pin Plastic Quad Flat-pack package. The 1.0µ high speed, low power CMOS Technology allows for substantial chip set stability when running at 33 and 50MHz.

The Chip Set consists of 82C491, and the 82C493. The 82C491 includes 486 CPU control, AT Bus Control, Direct Mapped Cache Control, Page Mode DRAM Control, Synchronous AT Bus Clock Generation, and Clock Switching Logic. The 82C493 contains a data bus conversion logic which performs the conversion necessary between the 8, 16 and 32-bit data paths.

The COUGAR II Chip Set provides very flexible cache based system implementation and a Page Mode DRAM memory to improve performance during read miss cycles. System performance is further enhanced by allowing Refresh and CPU cache hit cycles to occur concurrently without holding the CPU during Refresh cycle.

The COUGAR II is designed to be 100% compatible with the IBM PC/AT. With its optimized Cache and DRAM design, enhanced features like Shadow RAM BIOS and Concurrent Refresh; a high performance/low cost 486/AT can be implemented.



82C491 CPU/AT AND DRAM CONTROLLER

1.0 Overview

The 82C491 contains the Memory Controller, AT Bus Controller, CPU Controller, and clock generation circuitry. The Cache and DRAM Controllers are the main factors affecting the performance/cost ratio of the system. The 80486 has an on-chip 8K cache but a supplemental secondary cache can be easily built by using the 82C491 internal Burst Mode Direct Mapped Controller to reduce read cycle access time if the requested data is not currently stored in the on-chip cache. A Page Mode DRAM Controller further increases the performance by compensating for the time spent during the read miss cycle.

The 82C491 interfaces directly with the 80486 and implements the state machines required for controlling all bus accesses. The AT Bus Clock is synchronous with the processor clock and generated through a clock divider to insure that the system is 100% IBM compatible.

2.0 Functional Description

The 82C491 has the following function modules:

* **Reset and Shutdown Logic**
* **Clock Generation and Switching Logic**
* **CPU and AT Bus Control**
* **Master, DMA and Refresh Arbitration Logic**
* **Port B Register and NMI Logic**
* **OS/2 Optimization Logic**
* **Cache Controller Logic supporting Burst Mode**
* **DRAM Controller Logic**

2.1 Reset and Shutdown

The system contains four different resets: RESET1 is derived from the power-good signal at the power supply. Some power supplies have glitches on this signal, therefore, a de-bounce circuit is required before tying it to the RESET1 pin. RESET1 will generate both RESET3 (CPU Reset) and RESET4 (System Reset) for power-on initialization. This can only happen at system power-on. RESET2 is generated from the keyboard controller; it triggers RESET3 to reset the CPU either to perform a shutdown or to activate a software reset. It can also be generated by programming the internal register. RESET3 is activated for power-on, shutdown and for changing the CPU from protect mode back to real mode. RESET4 is activated when the entire system is reset.

2.2 Clock Generation

The 82C491 uses a single oscillator to generate the CPU and AT Bus clocks. The oscillator input should be the speed of the CPU. The AT Bus Clock is divided between 2 and 6. The output clock not only drives the CPU, but also, feedback to itself. The reason for this is to avoid any clock skew due to chip delay. This 50MHz clock is divided by 6 to make it approximately an 8MHz clock. A 16MHz clock will be used for AT Bus peripherals by dividing by 2 again which makes it 8MHz.

2.3 CPU and AT Bus Control

The CPU starts a cycle by asserting ADS- if the M/IO-, D/C- and W/R- signals plus address code turn out to be a local memory, LOCRAM- will assert LOW and the memory cycle begins. Otherwise, an AT Bus cycle will begin. ROM cycle is considered to be an AT Bus cycle because it is fixed at 8MHz and does not vary in relation to the CPU's speed. Therefore, a 200 nanosecond access time ROM will be sufficient. Shadow RAM is supported to increase the performance. Since the CPU is running at its maximum speed, and the AT Bus is running at 8MHz, synchronization is required. A DRAM does not need this handshaking because it is running at the same frequency as the CPU, thus, everything is synchronized. For the AT Bus cycle, ALE is where the AT Bus starts and the synchronized CPU ready is where it ends. This synchronization overhead can be significant when the AT Bus cycle is continuously accessed. The 82C491 synchronizes ALE with an option by switching the phase of the AT clock, not the signal itself, therefore, increasing the speed.

2.4 Master, DMA and Refresh

The Master Device uses the same pin as DMA for bus arbitration, and Refresh operates from a different pin so that it is easy to identify. The Master Device or DMA can be identified by the signals AEN8- and AEN16-. When either one is asserted LOW, it is a DMA cycle. The 82C491 supports both AT and Concurrent Refresh. No hold signal is sent back to the CPU in Concurrent Refresh. The AT Bus needs the full time to refresh as DRAMs do not need as much time. The 82C491 keeps track of when the DRAM refresh is finished, then allowing the CPU to start its next instruction parallel to AT Bus Refresh. If the CPU needs to access the AT Bus, it must wait until refresh is completed.

2.5 Port B and NMI

A parity error detected from 82C493 will cause 82C491 to generate NMI to the CPU. NMI can also be generated through software. The 82C491 provides access to the Port B register defined for a PC/AT. The chart below illustrates bit definition:

Bit Definition Chart			
Address	**Bits**	**Function**	**Description**
61H	7	Read Only	System Memory Parity Check
	6	Read Only	IO Channel Check
	5	Read Only	Timer 2 Output
	4	Read Only	Refresh Detection
	3	Read/Write	0: Enable IO Channel Check 1: Disable IO Channel Check
	2	Read/Write	0: Enable System Memory Parity Check 1: Disable System Memory Parity Check
	1	Read/Write	Speaker Data
	0	Read/Write	Timer 2 Gate

2.6 OS/2 Optimization

When running OS/2, 8742 needs to be programmed to activate the signal GATE A20 before entering Protected Mode. When it returns from the Protected Mode, some types of software use RESET2 by programming 8742 again. The Keyboard Controller is a very slow device, thus, the system is slowed down dramatically. 82C491 supports the fast Gate A20 and fast Reset to speed up performance.

2.7 Cache Control Logic

2.7.1 Introduction

The 82C491 has a Burst Mode Direct Mapped Cache Controller inside to support a "0" wait 80486 Microprocessor. It stores a copy of frequently accessed data/code from main memory in a "0" wait local Cache RAM. With this Cache Controller almost all critical paths are relocated to relatively small Cache RAMs (SRAM) and DRAM timing is no longer a major issue. Total cost is also decreased as expensive high speed DRAMs are not required.

Cache design issues: Our goal is to design a cache which has the best cost/performance ratio in the industry, therefore, availability, price, stability and manufacturability are all integral parts of our design. A Direct Mapped along with Post Write Cache is implemented in 82C491. The following sections will discuss in detail, the issues mentioned above.

2.7.2 Direct Map and Write Through

When cache size is small (<=16K), a 2/4 way set associative cache usually has a higher hit rate as compared to a Direct Mapped Cache. This is the reason why a CPU with on-chip-cache has a small 2/4 way Set Associative Cache (for example the Intel 486 or Motorola 680X0). However, as cache size becomes larger (>=32K), the hit rate differential between Direct Mapped and Set Associative Cache becomes unnoticeable.

2/4 way Set Associative Cache which needs a fast TAG/DATA RAM may cause low IC yield and high price when a TAG RAM is integrated into a chip set. From the cost/performance point of view, Direct Mapped Cache is the preferred architecture.

Direct Mapped Write through cache is the most straight forward and easiest to debug cache (less coherent problem).

2.7.3 TAG RAM

2.7.3.1 Introduction

The 82C491 needs external SRAM and Comparator to implement TAG RAM. The reason why we don't integrate TAG RAM into our chipset is YIELD which will translate into price. Internal TAG RAM can trigger a yield problem. When Intel announced their high speed CPU (50MHz, 50MHz.....). It will be some time before the Chip Set manufacturers to develop a cache controller to match the speed of the new CPU. Using an external TAG RAM will enable manufacturers to evolve into the higher speed CPU by using a higher speed, external SRAM.

2.7.3.2 External TAG RAM/DATA RAM Speed

The speeds of the external TAG RAM and Data RAM are listed below:

CPU	TAG RAM	CACHE DATA RAM
486-25MHz	25ns	35ns
486-33MHz	20ns	20ns
486-50MHz	15ns	15ns

2.7.4 Line Size

The 82C491 supports 128-bit line size only. A 64KB/256KB data cache can be achieved by using 8Kx8/32Kx8 SRAM in two banks.

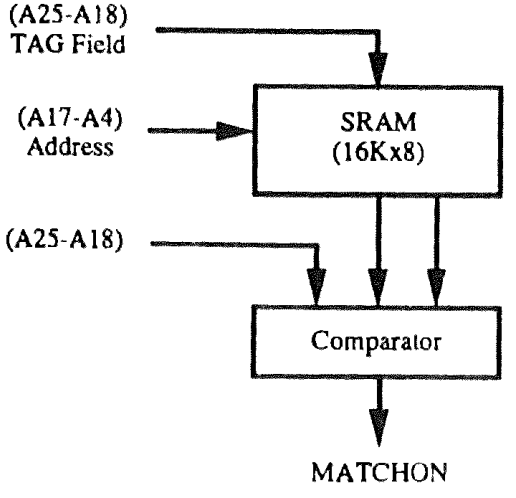
2.7.5 Examples of TAG RAM/DATA RAM Design

Example 1: Design a 64K Cache

TAG RAM: Three 4Kx4
Address to TAG RAM: A15-A4
TAG Field: A25-A16 (Data input to TAG RAM)
Cacheable Range: 64 MByte (A25-A4)
Data RAM: 2 Banks of SRAM, 8Kx8x4 each bank.
Cache Size: 4Kx4x4 = 64K

Example 2: Design a 256K Cache

TAG RAM: Two 16Kx4 SRAM (Total size: 16Kx8)
Address to TAG RAM: A17-A4
Tag Field: A25-A18 (Data input to TAG RAM)
Cacheable Range: 64 MByte (A25-A4)
Data RAM: 2 banks SRAM, 32Kx8x4 each bank.
Cache Size: 16Kx4x4 = 256K



2.8 DRAM Control Logic

2.8.1 Introduction

The DRAM Control Logic is designed and optimized for the 486 CPU. Unlike most systems with an external Cache Controller, the 82C491 DRAM Controller is tightly coupled with the on-chip Cache Controller. When CPU Address becomes available, both controllers operate in parallel. At the time when the Cache Controller discovers it is a read miss or write cycle, the DRAM Controller is ready to generate RAS (Page Miss) or CAS (Page Hit) right away!

To optimize memory performance, the DRAM Controller has built-in support for Page Mode. When larger capacity of the DRAM is installed, the size of the page will increase linearly to increase the hit rate.

The DRAM Controller supports up to 4 banks of DRAM with sizes up to 64MByte and three types of DRAM are supported: 256K, 1M and 4M.

2.8.2 DRAM Bank Configuration

The local DRAM System can be configured into 1 to 4 banks of DRAM. There is no limitation on the configuration of DRAM as long as no previous banks are empty. The DRAM Banks have to be filled in the following order: Bank0 -> Bank1 -> Bank2 -> Bank3. (See Table A below).

2.8.3 DRAM Speed and Wait State

In order to work with different types of DRAM speed, 82C491 supports wait state for memory read cycle as well as memory write cycle. For read cycle, a configuration of 0 to 4 wait state is available: R0WT, R1WT, R2WT, R3WT, and R4WT. For write cycle, the 82C491 supports: W0WT, W1WT and W2WT. (See Table B on next page)

TABLE A

Bank0	Bank1	Bank2	Bank3	Total Memory Size	Page Size
256K	NONE	NONE	NONE	1M	2K
256K	256K	NONE	NONE	2M	4K
256K	256K	256K	NONE	3M	6K
256K	256K	256K	256K	4M	8K
1M	256K	NONE	NONE	5M	6K
256K	256K	1M	NONE	6M	8K
256K	256K	256K	1M	7M	10K
1M	1M	NONE	NONE	8M	8K
1M	1M	256K	NONE	9M	10K
256K	256K	1M	1M	10M	12K
1M	1M	1M	NONE	12M	12K
1M	1M	1M	256K	13M	14K
1M	1M	1M	1M	16M	16K
256K	4M	NONE	NONE	17M	10K
256K	256K	4M	NONE	18M	12K
256K	256K	256K	4M	19M	14K
1M	4M	NONE	NONE	20M	12K
256K	1M	4M	NONE	21M	14K
256K	256K	1M	4M	22M	16K
1M	1M	4M	NONE	24M	16K
256K	1M	1M	4M	25M	18K
1M	1M	1M	4M	28M	20K
4M	4M	NONE	NONE	32M	16K
256K	4M	4M	NONE	33M	18K
256K	256K	4M	4M	34M	20K
1M	4M	4M	NONE	36M	20K
256K	1M	4M	4M	37M	22K
1M	1M	4M	4M	50M	24K
4M	4M	4M	NONE	48M	24K
256K	4M	4M	4M	49M	26K
1M	4M	4M	4M	52M	28K
4M	4M	4M	4M	64M	32K

Table A : Partial Possible DRAM Configurations

The 82C491 has a built-in Cache Controller, and the hit rate is fairly high (99% for a 64K SRAM). Most of the memory read cycle will be hit, and the data is accessed from the SRAM instead of the DRAM, so the DRAM wait state penalty becomes insignificant!

2.8.4 Row and Column Address

Table C, below, illustrates row/column address for different types of DRAM. For easy de-bugging, all row and column addresses are continuous, no scramble is needed.

2.9 DMA and Master Access DRAM Logic

The DMA Master can access the local DRAM through 82C491. When HLDAOUT and XMEMR/XMEMW become active, a memory read/write cycle will be performed. To guarantee cache coherence, the SRAM data will be updated when a memory write hit occurs.

2.10 Refresh Logic

In order to alleviate refresh penalty, 82C491 supports "Concurrent Refresh" in addition to normal AT Refresh. Traditional AT Refresh will send a HOLD to stop the CPU, then, after receiving HLDA from the CPU, refresh will begin. Concurrent Refresh can execute the refresh cycle concurrently with the CPU as long as there is no DRAM conflict. (i.e. we enhance performance by allowing refresh to work on the DRAM and the CPU to work on the Cache RAM at the same time.) To quiet refresh noise on the Motherboard, all RAS are staggered during refresh cycle.

2.11 Shadow RAM

For those BIOS Call Intensive Application Softwares, it is not efficient to run BIOS Call in low speed ROM. Moving all ROM contents to a high speed DRAM will largely improve the performance of a BIOS Call intensive program.

82C491 allows all Motherboard ROM and Adapter Card ROM to be shadowed on the Motherboard DRAM as long as they are resident in (C0000-CFFFF), (D0000-DFFFF), (E0000-EFFFF), or (F0000-FFFFF) range. If the Adapter ROM is on the Motherboard, it can still be shadowed.

TABLE B

CPU SPEED	DRAM SPEED	DRAM WAIT STATE
486-25MHZ	100NS (CMOS)	(W0WT, R2WT)
486-33MHZ	80NS (CMOS)	(W0WT, R3WT)
486-50MHZ	80NS (CMOS)	(W2WT, R4WT)

Table B: Wait States/DRAM Speeds

TABLE C

DRAM Configuration	Row Address	Column Address
256K Page Mode	(A19-A11)	(A10-A2)
1M Page Mode	(A21-A12)	(A11-A2)
4M Page Mode	(A23-A13)	(A12-A2)

Table C : Row/Column Address for Different Types of DRAM

3.0 Configuration Registers

The 82C491 has internal registers used for system configuration and internal control. These areas are accessed through IO Ports 22H and 23H. Each access to an internal register is accomplished by first, writing its index into Port 22H. This index is then used to gate the appropriate internal register and the control data is accessed through Port 23H.

There are eighteen configuration registers in 82C491. The definitions of these registers are as follows:

TABLE D
Clock Control

Index	Bits	Values and Functions	Default
10H	1:0	AT Bus Clock Select 00: ATCLK = CLK/6 01: ATCLK = CLK/4 10: Reserved 11: ATCLK = CLK/2	00
	2	Reserved	0
	3	Reserved	0
	4	Extended IO Decode Enable 0: Disable Extended IO Decode 1: Enable Extended IO Decode	0
	5	Refresh Selection 0: AT Type Refresh 1: Concurrent Refresh	0
	7:6	Reserved	00

CACHE and DRAM Interleave Configuration

Index	Bits	Values and Functions	Default
11H	0	0: Set valid# output to 1 to flush cache 1: Set valid# output to 0.	0
	1	0: Disable External Cache 1: Enable External Cache	0
	2	0: Normal Operation 1: Enable direct SRAM access. Once set to one, all access to address from 040000 to 07FFFF will be forced to SRAM access. This feature is designed for power-on SRAM checking and diagnostic checking.	0
	3	0: Remapped 256K is non-cacheable 1: Remapped 256K is cacheable (See Reg 15H)	0
	4	Reserved	0
	5	Reserved	0
	6	Should be "1" when External CACHE gets enabled.	0
	7	Reserved. Must be 0 for proper operation.	0

Registers 12H, 13H and 14H are related to shadow RAM. The definitions and applications are as follows:

Index	Bits	Values and Functions	Default
12H	0	RAM at C0000H-CFFFFH 0: Read/Write 1: Read Only	0
	1	Access ROM/RAM at C0000H-CFFFFH 0: Accessed on-board ROM 1: Access Shadow RAM enabled in 16K blocks. (Please refer to Reg 13H) For the disabled blocks, access will be passed to the AT Bus.	1
	2	RAM at D0000H-DFFFFH 0: Read/Write 1: Read Only	0
	3	Access ROM/RAM at D0000H-DFFFFH. 0: Accessed on-board ROM 1: Access Shadow RAM enabled in 16K blocks. (Please refer to Reg 13H). For the disabled blocks, access will be passed to the AT Bus.	1
	4	RAM at E0000H-EFFFFH 0: Read/Write 1: Read Only	0
	5	Access ROM/RAM at E0000H-EFFFFH. 0: Accessed on-board ROM. 1: Access Shadow RAM enabled in 16K blocks. (Please refer to Reg 14H). For the disabled blocks, access will be passed to the AT Bus.	1
	6	Access ROM/RAM at F0000H-FFFFFH (System BIOS ROM) 0: Read from ROM, Write to RAM 1: Read from Shadow RAM, Write will be protected (will not be written into RAM)	0
	7	Reserved.	0

Shadow RAM 16K Map (Block C, D)

Index	Bits	Values and Functions	Default
13H	0	RAM at C0000H-C3FFFH 0: Disabled. Access to this area will be passed to the AT Bus. 1: Enable access to this area RAM	0
	1	RAM at C4000H-C7FFFH 0: Disabled. Access to this area will be passed to the AT Bus. 1: Enable access to this area RAM	0

Shadow RAM 16K Map (Block C, D) (Continued)

Index	Bits	Values and Functions	Default
13H	2	RAM at C8000H-CBFFFH 0: Disabled. Access to this area will be passed to the AT Bus. 1: Enable access to this area RAM.	0
	3	RAM at CC000H-CFFFFH 0: Disabled. Access to this area will be passed to the AT Bus. 1: Enable access to this area RAM.	0
	4	RAM at D0000H-D3FFFH 0: Disabled. Access to this area will be passed to the AT Bus. 1: Enable access to this area RAM.	0
	5	RAM at D4000H-D7FFFH 0: Disabled. Access to this area will be passed to the AT Bus. 1: Enable access to this area RAM.	0
	6	RAM at D8000H-DBFFFH 0: Disabled. Access to this area will be passed to the AT Bus. 1: Enable access to this area RAM.	0
	7	RAM at DC000H-DFFFFH 0: Disabled. Access to this area will be passed to the AT Bus. 1: Enable access to this area RAM.	0

Shadow RAM 16K Map (Block E)

Index	Bits	Values and Functions	Default
14H	0	RAM at E0000H-E3FFFH 0: Disabled. Access to this area will be passed to the AT Bus. 1: Enable access to this area RAM.	0
	1	RAM at E4000H-E7FFFH 0: Disabled. Access to this area will be passed to the AT Bus. 1: Enable access to this area RAM.	0
	2	RAM at E8000H-EBFFFH 0: Disabled. Access to this area will be passed to the AT Bus. 1: Enable access to this area RAM.	0
	3	RAM at EC000H-EFFFFH 0: Disabled. Access to this area will be passed to the AT Bus. 1: Enable access to this area RAM.	0
	5:4	Version Number. (0,0) for Current Vers.	0
	6	Reserved.	0
	7	Must be "1" to work.	

To shadow System ROM BIOS on the Motherboard (Block F) the following steps must be followed:

1) Set Reg12 Bit6 to 0 (it is default to 0 after reset.
2) Read ROM Data into CPU Register.
3) Write the data stored in the CPU register to RAM.
4) If not complete, return to Step 2. Otherwise, go on to the next step.
5) Set Reg12 Bit6 to 1 to write protect Shadow RAM.

Since 82C491 allows for the Adapter ROM (on block C,D,E) to be either on the Motherboard or on the Adapter Card, shadowing them is slightly different. Below are two examples of how to shadow ROM on Block C:

Case A: Adapter ROM is on Adapter Card.

1) Set REG13 Bits 0, 1, 2, 3 to 0 to disable RAM; set REG12 Bit 0 to 0 to make RAM Read/Write; and set REG12 Bit 1 to 1 to access adapter ROM on the AT Bus.
2) Read the ROM Data from the adapter card to the CPU register.
3) Enable Shadow RAM by writing a 1 to REG13H Bit 0, Bit 1, Bit 2, and Bit 3. Then write 1 to REG12H Bit 1 to enable RAM access.
4) Write the data stored in the CPU register to Shadow RAM.
5) If not complete, go back to step 1; otherwise, go on to the next step.
6) Disable unused RAM by writing 0 to REG13 Bit 0, Bit 1, Bit 2 or Bit 3. Then make Shadow RAM read only by writing 1 to REG12 Bit 0.

Case B: Adapter ROM is on the Motherboard.

1) Set REG13 Bits 0, 1, 2, & 3 to 0 to disable RAM; set REG12 Bit 0 to 0 to make RAM Read/Write; and set REG12 Bit 1 to 0 to access on-board ROM.

TABLE D
256KB Remap Location

Index	Bits	Values and Functions	Default
15H	4:0	00001 1MB 00010 2MB 00011 3MB 00100 4MB 00101 5MB 00110 6MB 00111 7MB 01000 8MB 01001 9MB 01010 10MB 01011 11MB 01100 12MB 01101 13MB 01110 14MB 01111 15MB 10000 16MB	00001
	5	0: Disable Remap 1: Enable Remap	0
	6	Fast Gate A20 0: Disable 1: Enable	0
	7	Reserved	0
		NOTE: We only allow 256K*1, 1M*1 to be remapped, and the maximum remap address is 16MB.	

2) Read the ROM Data to CPU register.

3) Enable Shadow RAM by writing 1 to REG13H Bits 0, 1, 2 & 3; and write 1 to REG12 Bit 1 to enable RAM access.

4) Write the data stored in the CPU register to the Shadow RAM.

5) If not complete, go back to step 1. Otherwise, go on the next step.

6) Disable the unused RAM by writing 1 to REG13 Bit 0, 1, 2 or 3. Then make Shadow RAM read only by writing 1 to REG12 Bit 0.

If the Motherboard DRAM on blocks A, B, D, and E are not utilized, it will never be accessed and is, therefore, obsolete. By allowing remapping of the top address to those unused locations, we can gain an additional 256K in memory space. i.e. if the total memory size is 16M, then the top address becomes 16M + 256K instead of simply 16M. Blocks A and B are assigned to the Video RAM which is usually located on the Adapter Card. The Motherboard DRAM space on blocks A and B are available for remapping.

DRAM Bank Configuration (Continued)

Index	Bits	Values and Functions	Default
16H	1:0	Bank0 DRAM Type 00: None 01: 256K 10: 1M 11: 4M	01
	3:2	Bank1 DRAM Type 00: None 01: 256K 10: 1M 11: 4M	00
	5:4	Bank2 DRAM Type 00: None 01: 256K 10: 1M 11: 4M	00
	7:6	Bank3 DRAM Type 00: None 01: 256K 10: 1M 11: 4M	00

DRAM Configuration

Index	Bits	Values and Functions	Default
17H	1:0	Write Cycle Wait States 00: 0WT 01: 1WT 10: 2WT 11: Reserved	10
	4:2	Read Cycle Wait States 000: 0WT 001: 1WT 010: 2WT 011: 3WT 100: 4WT 101: Reserved 110: Reserved 111: Reserved	100
	5	Reserved	0
	6	Enable Page Mode 0: Disable Page Mode 1: Enable Page Mode	0
	7	Reserved	0

SRAM/DRAM Configuration

Index	Bits	Values and Functions	Default
18H	7:0	Reserved for 386	00000000

Fast Reset Control

Index	Bits	Values and Functions	Default
19H	0	Fast CPU Reset. 0: Disable Keyboard Reset Emulation 1: Enable Keyboard Reset Emulation	0
	1	Fast Reset.Control 0: A fast Reset will activate a RESET2 immediately. 1: A fast Reset will activate a RESET2 only after a HALT instruction has been detected.	0
	7:2	Reserved	000000

Cacheable Shadow RAM Select

1AH	3	Cacheable Shadow RAM block C 0: Disable 1: Enable	0

Non-Cacheable Block0 Address Register

20H	7:0	Non-Cacheable Address A25 to A18.	00000000

Non-Cacheable Block 0 Address/Size Register

Index	Bits	Values and Functions	Default
21H	3:0	Non-Cacheable Address A17 to A14	0000
	7:4	B7 B6 B5 B4 0 0 0 0 Disabled 0 0 0 1 16KB 0 0 1 0 32KB 0 0 1 1 64KB 0 1 0 0 128KB 0 1 0 1 256KB 0 1 1 0 512KB 0 1 1 1 1MB 1 0 0 0 2MB 1 0 0 1 4MB 1 0 1 0 8MB 1 0 1 1 16MB 1 1 0 0 32MB 1 1 0 1 64MB	0000

Non-Cacheable Block 1 Address Register

Index	Bits	Values and Functions	Default
22H	7:0	Non-Cacheable Address A25 to A18	00000000
23H	3:0	Non-Cacheable Address A17 to A14	0000
	7:4	B7 B6 B5 B4 0 0 0 0 Disabled 0 0 0 1 16KB 0 0 1 0 32KB 0 0 1 1 64KB 0 1 0 0 128KB 0 1 0 1 256KB 0 1 1 0 512KB 0 1 1 1 1MB 1 0 0 0 2MB 1 0 0 1 4MB 1 0 1 0 8MB 1 0 1 1 16MB 1 1 0 0 32MB 1 1 0 1 64MB	0000

Non-Cacheable Block 2 Address Register

Index	Bits	Values and Functions	Default
24H	7:0	Non-Cacheable Address A25 to A18	00000000

Non-Cacheable Block 2 Address/Size Register

Index	Bits	Values and Functions	Default
25H	3:0	Non-Cacheable Address A17 to A14	0000
	7:4	B7 B6 B5 B4	0000
		0 0 0 0 Disabled	
		0 0 0 1 16KB	
		0 0 1 0 32KB	
		0 0 1 1 64KB	
		0 1 0 0 128KB	
		0 1 0 1 256KB	
		0 1 1 0 512KB	
		0 1 1 1 1MB	
		1 0 0 0 2MB	
		1 0 0 1 4MB	
		1 0 1 0 8MB	
		1 0 1 1 16MB	
		1 1 0 0 32MB	
		1 1 0 1 64MB	

Non-Cacheable Block 3 Address Register

26H	7:0	Non-Cacheable Address A25 to A18	0000000

Non-Cacheable Block 3 Address/Size Register

Index	Bits	Values and Functions	Default
27H	3:0	Non-Cacheable Address A17 to A14	0000
	7:4	B7 B6 B5 B4	0000
		0 0 0 0 Disabled	
		0 0 0 1 16KB	
		0 0 1 0 32KB	
		0 0 1 1 64KB	
		0 1 0 0 128KB	
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