

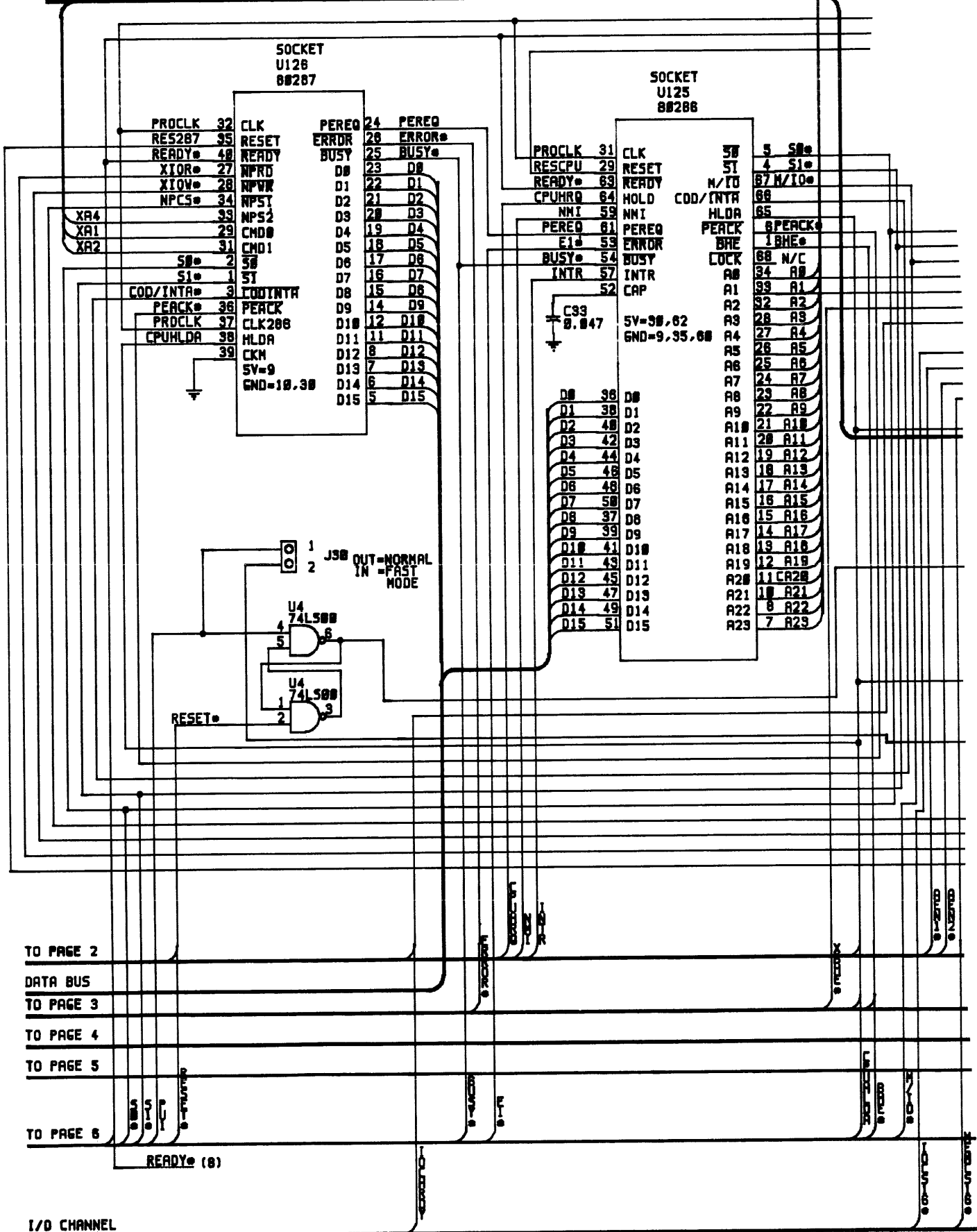


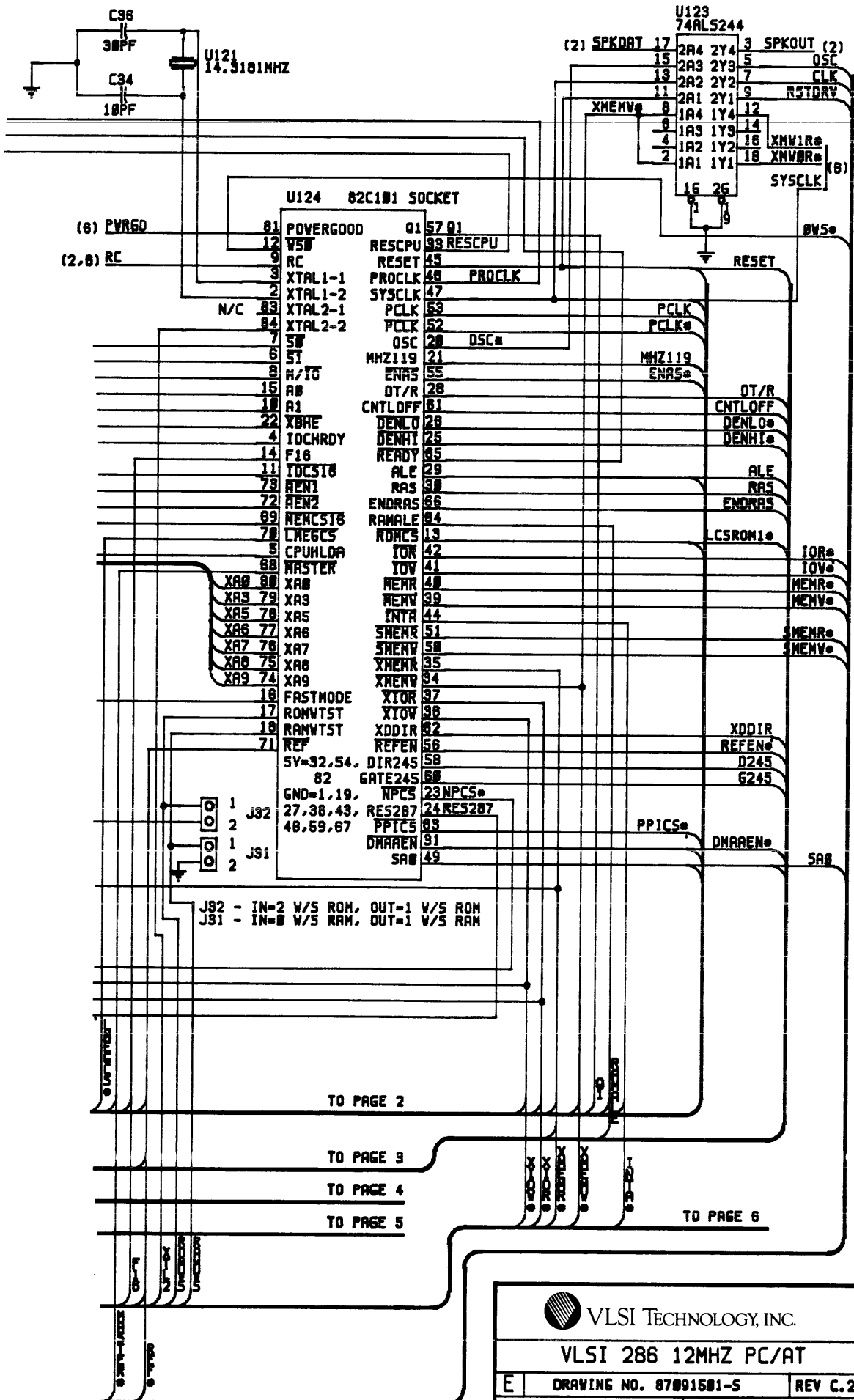
VLSI TECHNOLOGY, INC.


12 MHz PC/AT-COMPATIBLE SCHEMATICS

ADR BUS

XA BUS





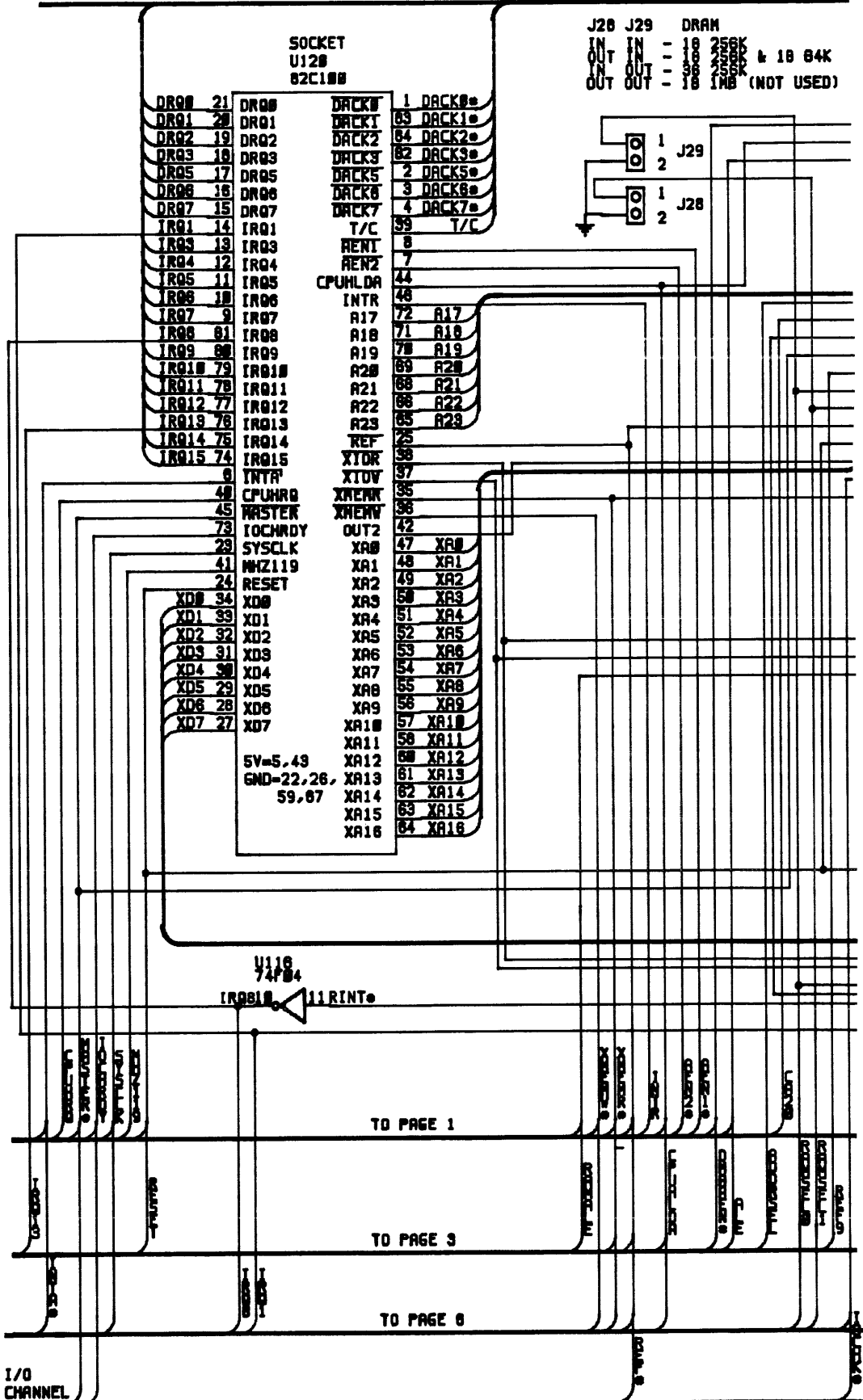

VLSI TECHNOLOGY, INC.
VLSI 286 12MHZ PC/AT
E DRAWING NO. 87091501-S REV C.2
DATE: 6/1/88 SHEET 1 OF 8

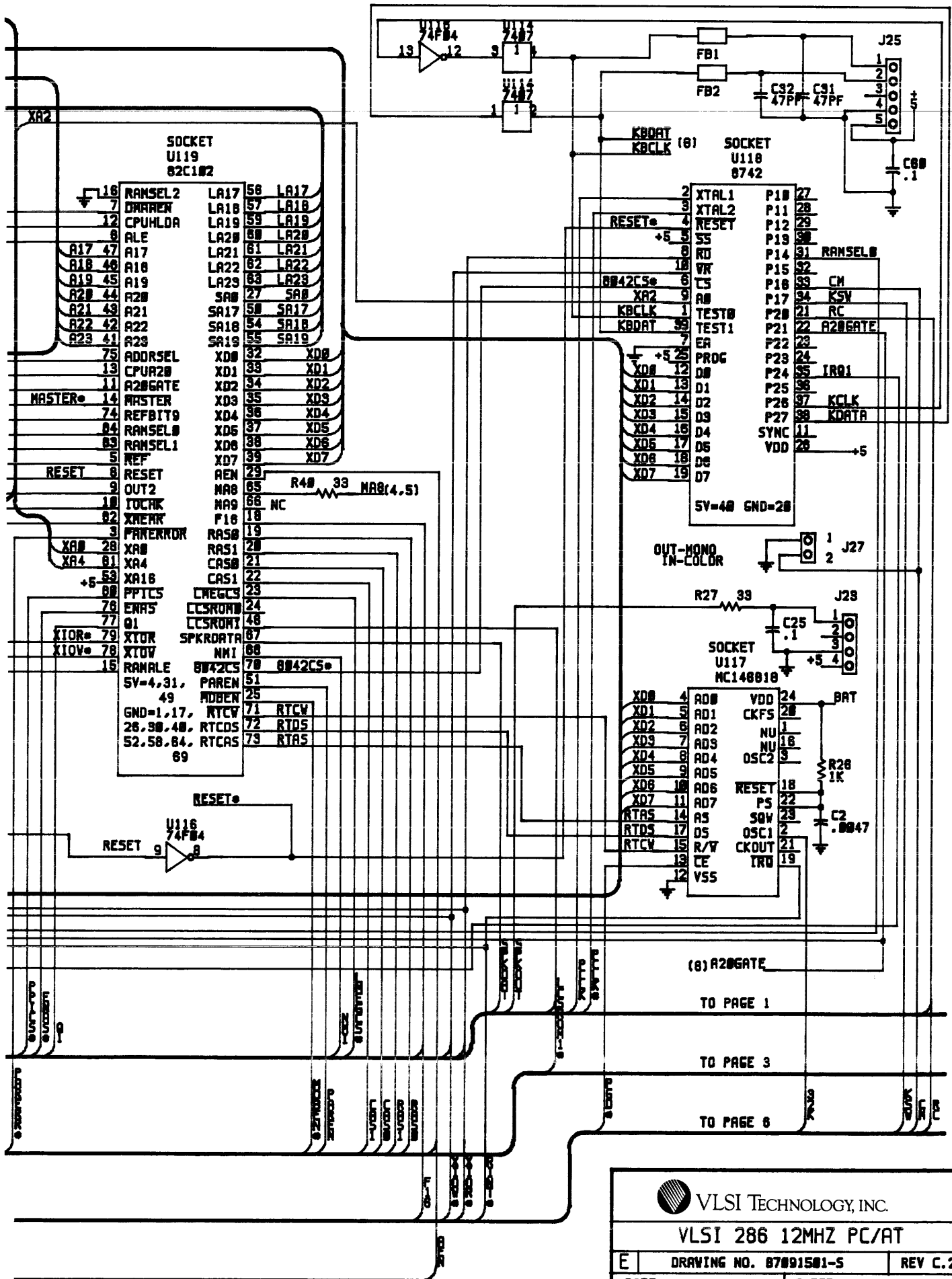
XA BUS


XD BUS

ADR BUS

I/O CHANNEL






VLSI TECHNOLOGY, INC.
VLSI 286 12MHZ PC/AT

E	DRAWING NO. 87891501-5	REV C.2
DATE:	6/1/88	SHEET 2 OF 8

I/O CHANNEL

ADR BUS

SOCKET U113 82C103

A1	20	A1	SA0	53	SA0
A2	19	A2	SA1	52	SA1
A3	18	A3	SA2	51	SA2
A4	17	A4	SA3	50	SA3
A5	16	A5	SA4	48	SA4
A6	15	A6	SA5	47	SA5
A7	14	A7	SA6	46	SA6
A8	13	A8	SA7	45	SA7
A9	9	A9	SA8	49	SA8
A10	8	A10	SA9	42	SA9
A11	7	A11	SA10	41	SA10
A12	6	A12	SA11	40	SA11
A13	5	A13	SA12	38	SA12
A14	4	A14	SA13	37	SA13
A15	3	A15	SA14	36	SA14
A16	2	A16	SA15	35	SA15
		A16	SA16	34	SA16
23		CPUHLDA			
22		ALE	XA1	89	XA1
28		REFEN	XA2	82	XA2
25		REF	XA3	81	XA3
30		REFBITS9	XA4	80	XA4
27		ADDRSEL	XA5	79	XA5
29		ERROR	XA6	78	XA6
32		SBHE	XA7	77	XA7
28		RESET	XA8	76	XA8
24		DARREN	XA9	74	XA9
10		RAMALE	XA10	73	XA10
12		BRE	XA11	72	XA11
66		XBRE	XA12	71	XA12
55		BALE	XA13	70	XA13
			XA14	69	XA14
			XA15	68	XA15
			XA16	67	XA16
		SV=1.31, 44.58	MA0	57	MA0R
			MA1	58	MA1R
			MA2	59	MA2R
			MA3	60	MA3R
			MA4	61	MA4R
			MA5	62	MA5R
			MA6	63	MA6R
			MA7	64	MA7R
			IRQ13	64	

SV=1.31, 44.58
 GND=11, 21, 33, 39, 49, 54, 85, 75

TO PAGE 1

TO PAGE 2

TO PAGE 8

I/O CHANNEL

SD BUS

XD BUS

SOCKET U112 82C104

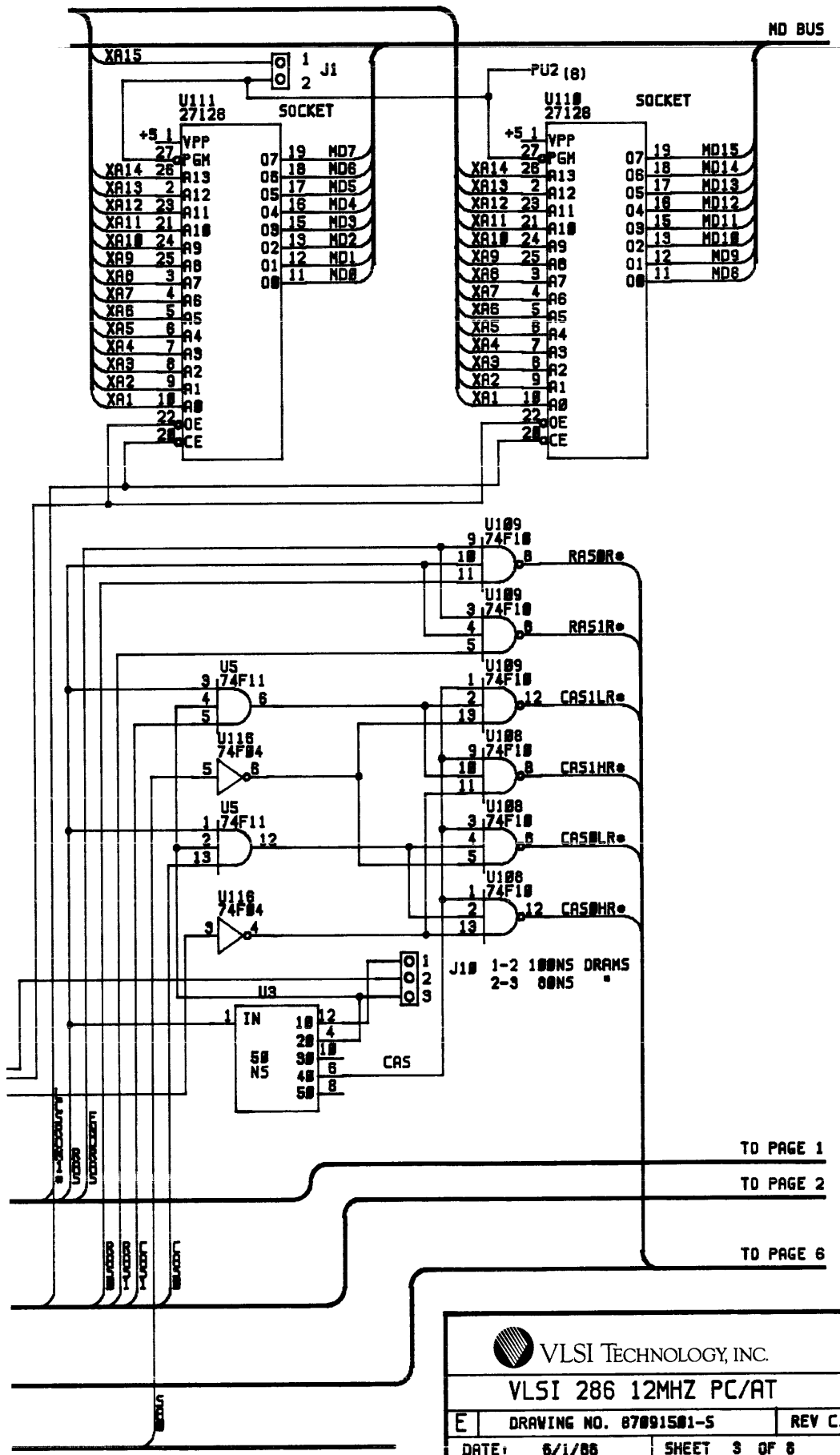
DATA BUS

D0	82	D0	SD0	42	SD0
D1	84	D1	SD1	41	SD1
D2	2	D2	SD2	40	SD2
D3	4	D3	SD3	39	SD3
D4	7	D4	SD4	37	SD4
D5	9	D5	SD5	36	SD5
D6	11	D6	SD6	35	SD6
D7	13	D7	SD7	34	SD7
D8	83	D8	SD8	44	SD8
D9	1	D9	SD9	45	SD9
D10	3	D10	SD10	46	SD10
D11	5	D11	SD11	47	SD11
D12	8	D12	SD12	49	SD12
D13	10	D13	SD13	50	SD13
D14	12	D14	SD14	51	SD14
D15	14	D15	SD15	52	SD15


MD0	55	MD0	MD0	
MD1	56	MD1	MD1	
MD2	57	MD2	MD2	
MD3	58	MD3	MD3	
MD4	59	MD4	MD4	
MD5	60	MD5	MD5	
MD6	61	MD6	MD6	
MD7	62	MD7	MD7	
MD8	64	MD8	MD8	
MD9	65	MD9	MD9	
MD10	66	MD10	MD10	
MD11	67	MD11	MD11	
MD12	68	MD12	MD12	
MD13	69	MD13	MD13	
MD14	70	MD14	MD14	
MD15	71	MD15	MD15	
XD0	73	XD0	XD0	
XD1	74	XD1	XD1	
XD2	75	XD2	XD2	
XD3	76	XD3	XD3	
XD4	77	XD4	XD4	
XD5	78	XD5	XD5	
XD6	79	XD6	XD6	
XD7	80	XD7	XD7	
MDPIN0	28	R7	33	MDPIN0
MDPIN1	29	R8	33	MDPIN1

SV=43, 54, 81
 GND=6, 33, 38, 48, 53, 63, 72

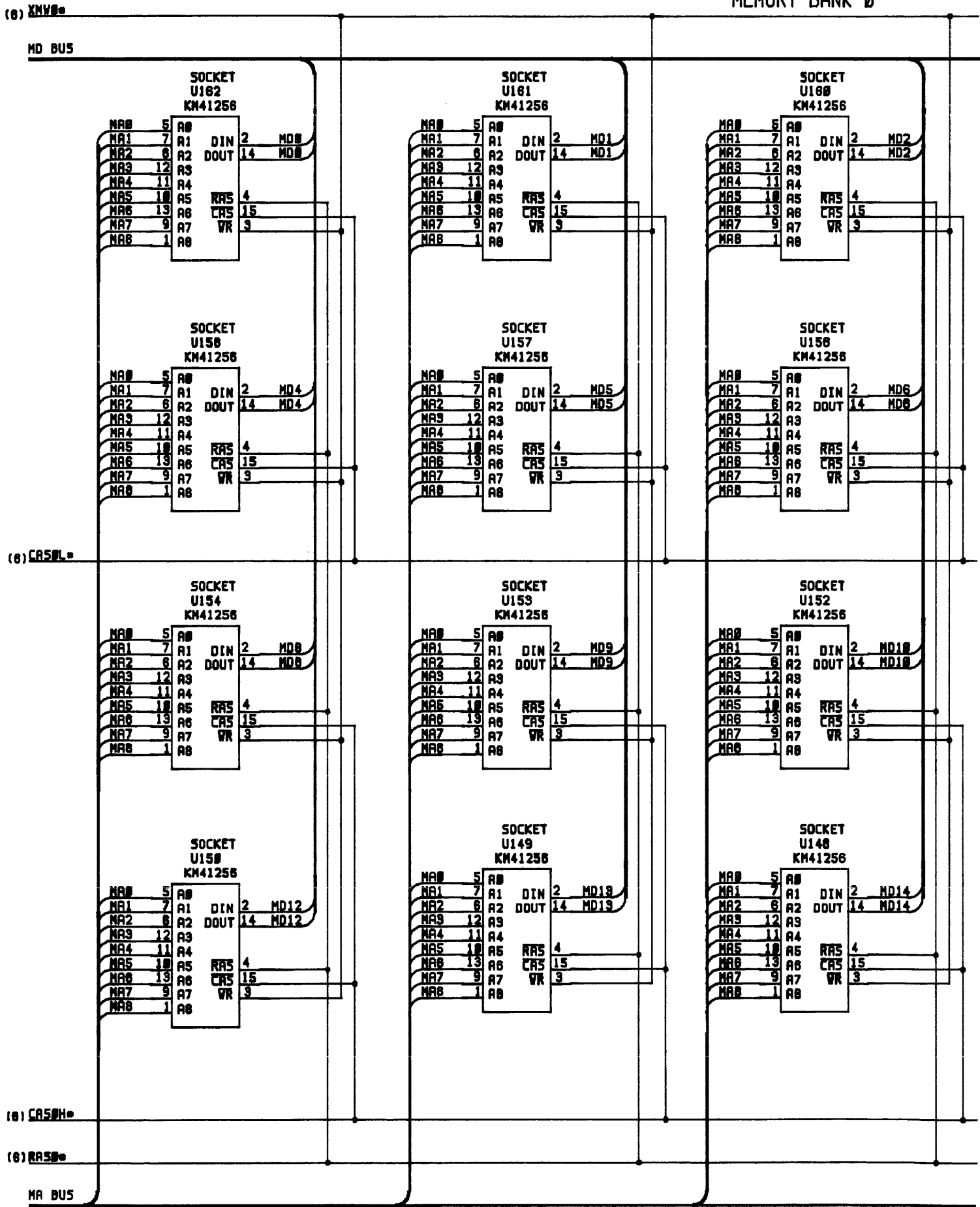
J1 = OUT - 27128 EPROMS
 J1 = IN - 27258 "

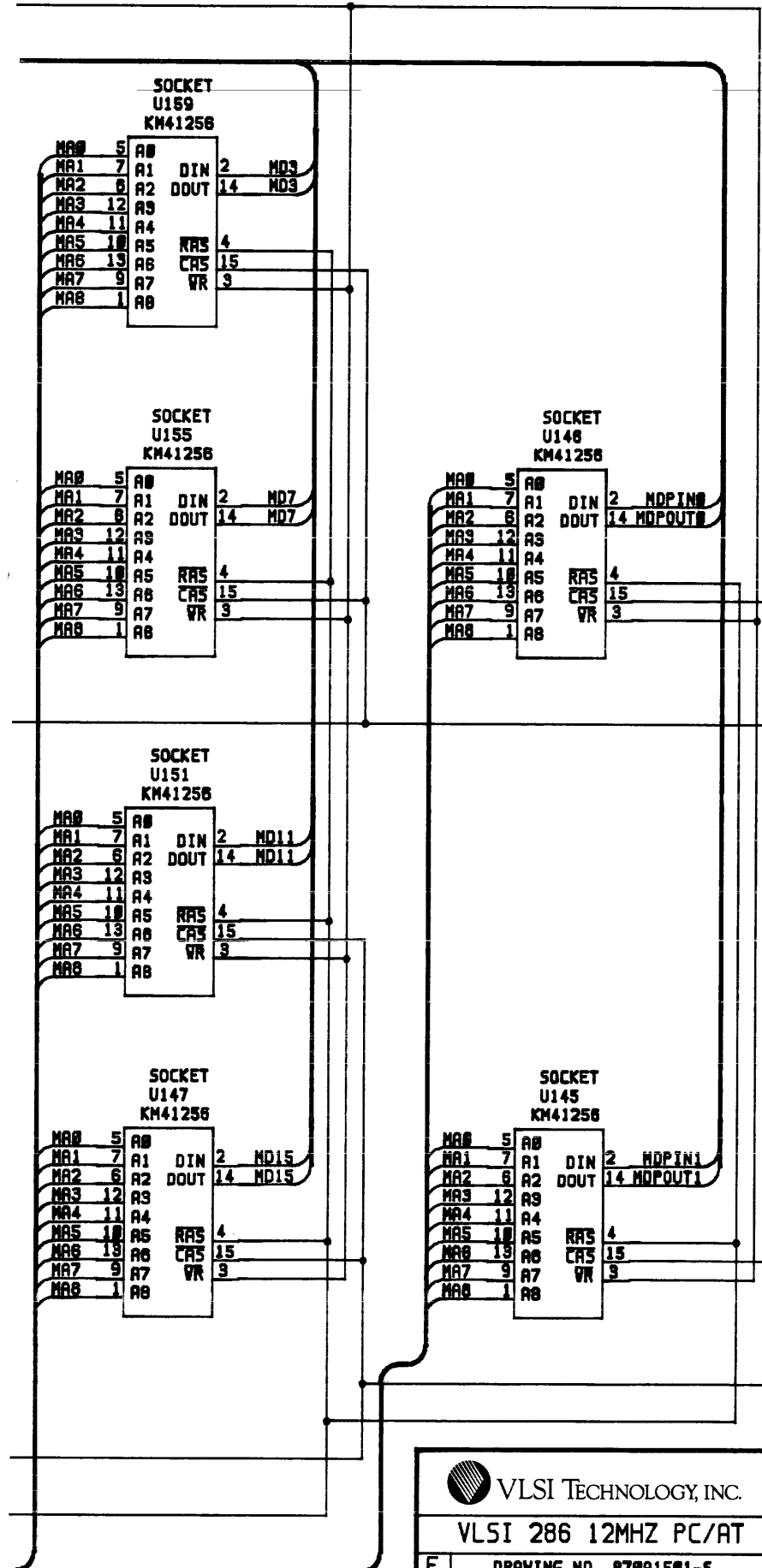


TO PAGE 1
 TO PAGE 2
 TO PAGE 6

 VLSI TECHNOLOGY, INC.		
VLSI 286 12MHZ PC/AT		
E	DRAWING NO. 87091501-5	REV C.2
DATE: 6/1/86	SHEET 3 OF 6	

MEMORY BANK 0





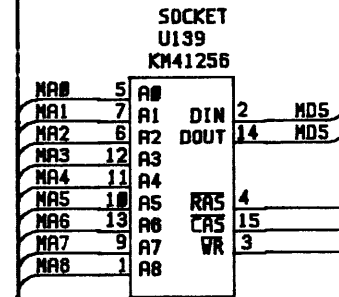
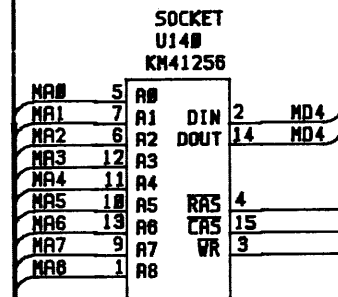
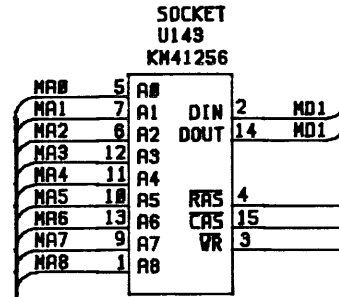
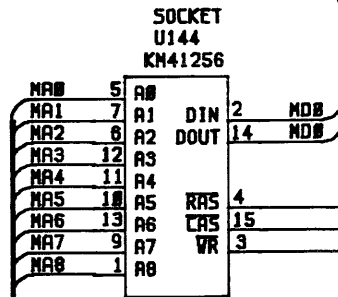
VLSI TECHNOLOGY, INC.

VLSI 286 12MHZ PC/AT

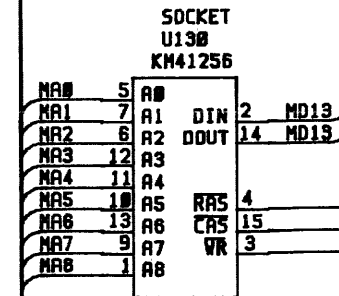
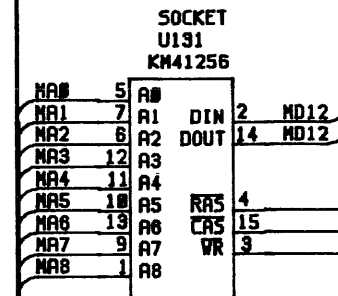
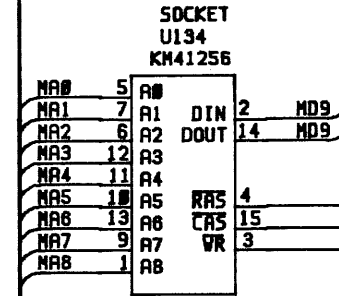
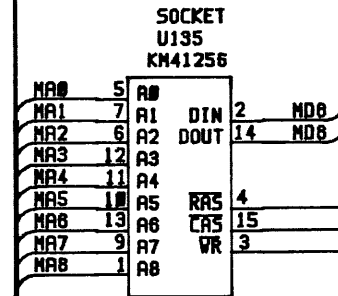
E	DRAWING NO. 87091501-5	REV C.2
DATE:	6/1/88	SHEET 4 OF 8

(6) XMV1e

MD BUS



(6) CAS1L

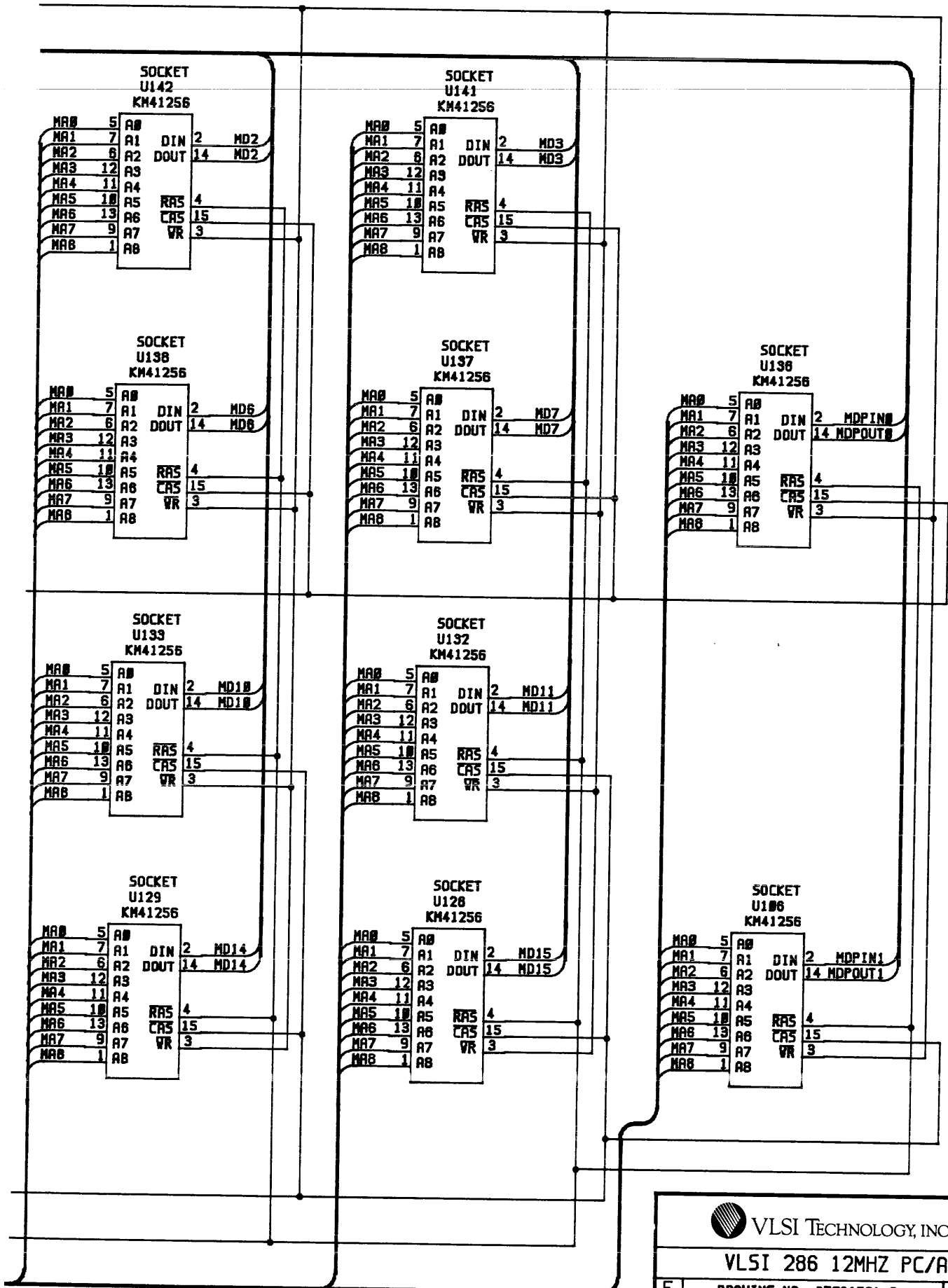


(6) CAS1M

(6) CAS1e

MA BUS

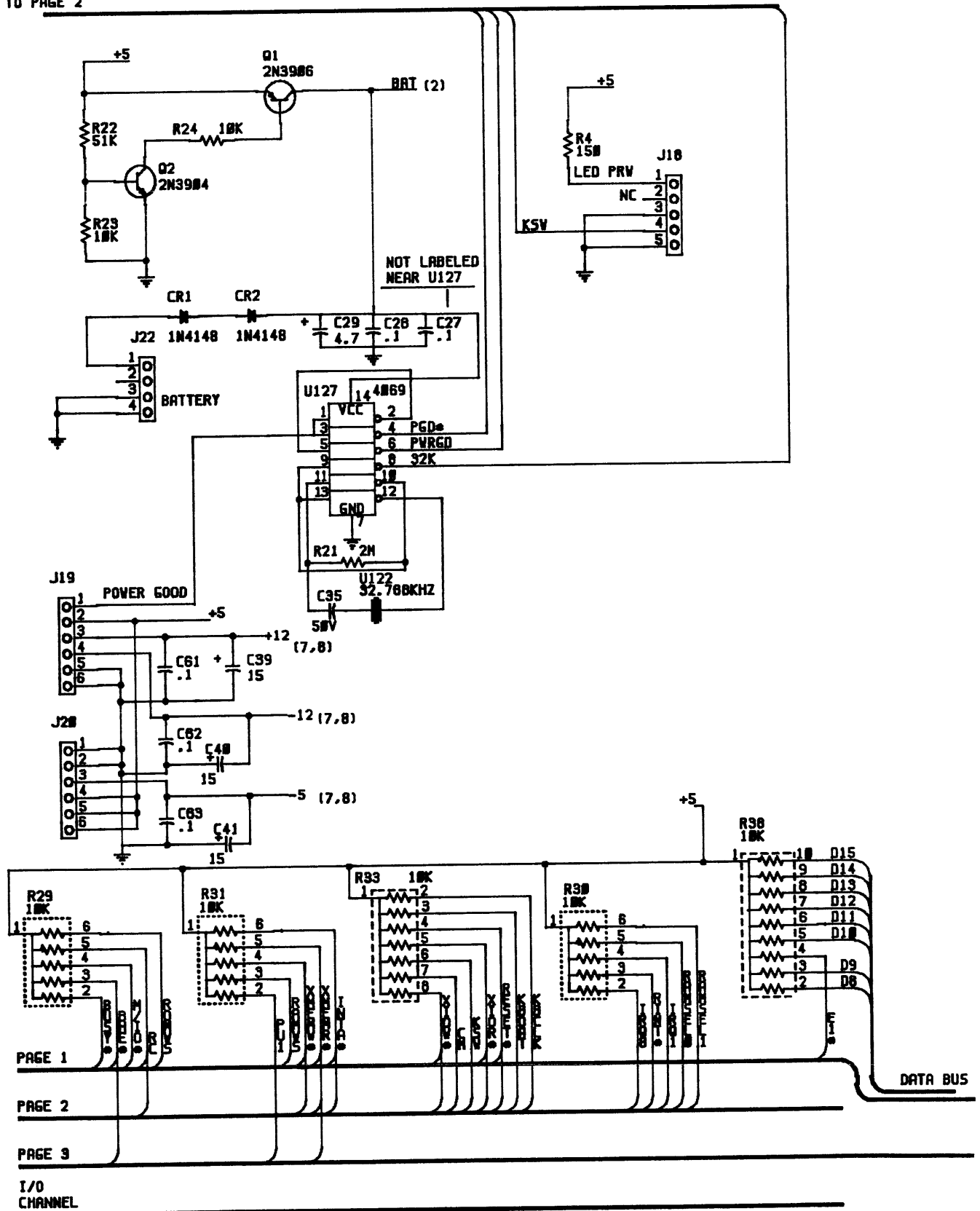
MEMORY BANK 1

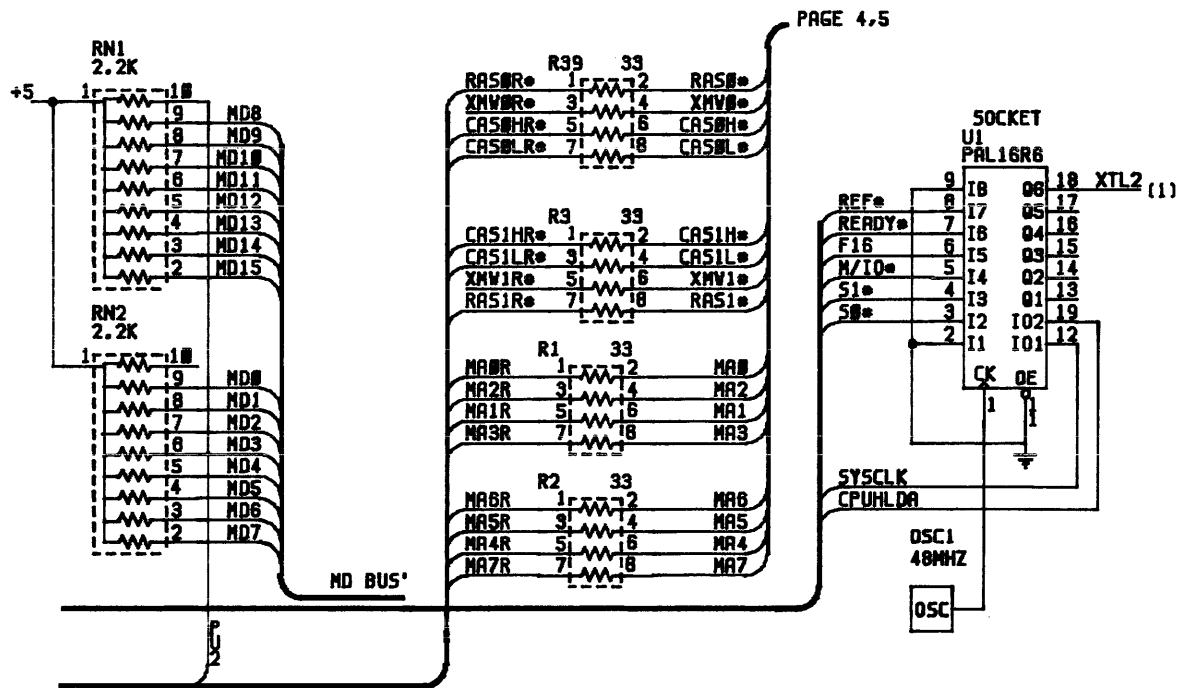
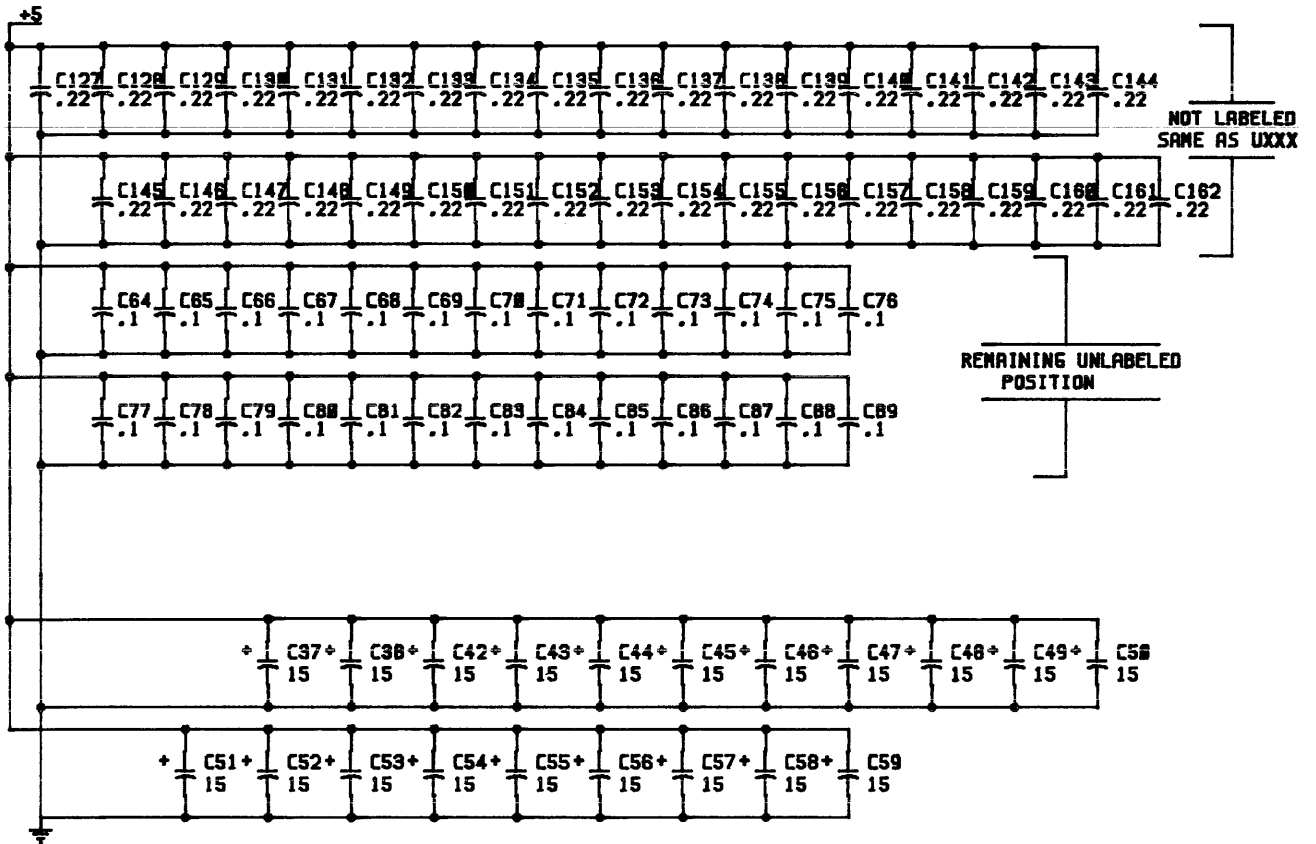


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VLSI 286 12MHZ PC/AT

E	DRAWING NO. 87091501-5	REV C.2
DATE: 8/1/88	SHEET 5 OF 8	





VLSI TECHNOLOGY, INC.

VLSI 286 12MHZ PC/AT

E	DRAWING NO. 87091501-5	REV C.2
DATE: 6/1/88	SHEET 6 OF 8	

J2
A B

IOCHK*	1	GND
SD7	2	RSTDRV
SD6	3	+5
SD5	4	IRQ9
SD4	5	-5
SD3	6	DRQ2
SD2	7	-12
SD1	8	ØV5*
SDØ	9	+12
IOCHRDY	10	GND
AEN	11	SMEMV*
SA19	12	SMEMR*
SA18	13	IOV*
SA17	14	IOR*
SA16	15	DACK3*
SA15	16	DRQ3
SA14	17	DACK1*
SA13	18	DRQ1
SA12	19	REF*
SA11	20	CLK
SA10	21	IRQ7
SA9	22	IRQ6
SA8	23	IRQ5
SA7	24	IRQ4
SA6	25	IRQ3
SA5	26	DACK2*
SA4	27	T/C
SA3	28	BALE
SA2	29	+5
SA1	30	OSC
SAØ	31	GND

J3
A B

IOCHK*	1	GND
SD7	2	RSTDRV
SD6	3	+5
SD5	4	IRQ9
SD4	5	-5
SD3	6	DRQ2
SD2	7	-12
SD1	8	ØV5*
SDØ	9	+12
IOCHRDY	10	GND
AEN	11	SMEMV*
SA19	12	SMEMR*
SA18	13	IOV*
SA17	14	IOR*
SA16	15	DACK3*
SA15	16	DRQ3
SA14	17	DACK1*
SA13	18	DRQ1
SA12	19	REF*
SA11	20	CLK
SA10	21	IRQ7
SA9	22	IRQ6
SA8	23	IRQ5
SA7	24	IRQ4
SA6	25	IRQ3
SA5	26	DACK2*
SA4	27	T/C
SA3	28	BALE
SA2	29	+5
SA1	30	OSC
SAØ	31	GND

J11
C D

SBHE*	1	NEMC516*
LA23	2	IOCS16*
LA22	3	IRQ1Ø
LA21	4	IRQ11
LA2Ø	5	IRQ12
LA19	6	IRQ15
LA18	7	IRQ14
LA17	8	DACKØ*
MEMR*	9	DRQØ
MEMV*	10	DACK5*
SDØ	11	DRQ5
SD9	12	DACKØ*
SD1Ø	13	DRQ6
SD11	14	DACK7*
SD12	15	DRQ7
SD13	16	+5
SD14	17	MASTER*
SD15	18	GND

I/O
CHANNEL

J4
A B

IOCHK*	1	GND
SD7	2	RSTDRV
SD8	3	+5
SD5	4	IR09
SD4	5	-5
SD3	6	DR02
SD2	7	-12
SD1	8	#V5*
SD0	9	+12
IOCHRDY	10	GND
AEN	11	SMEMV*
SA19	12	SMEMR*
SA18	13	IOV*
SA17	14	IOR*
SA16	15	DACK3*
SA15	16	DR03
SA14	17	DACK1*
SA13	18	DR01
SA12	19	REF*
SA11	20	CLK
SA10	21	IR07
SA9	22	IR06
SA8	23	IR05
SA7	24	IR04
SA6	25	IR03
SA5	26	DACK2*
SA4	27	T/C
SA3	28	BALE
SA2	29	+5
SA1	30	OSC
SA0	31	GND

J5
A B


IOCHK*	1	GND
SD7	2	RSTDRV
SD8	3	+5
SD5	4	IR09
SD4	5	-5
SD3	6	DR02
SD2	7	-12
SD1	8	#V5*
SD0	9	+12
IOCHRDY	10	GND
AEN	11	SMEMV*
SA19	12	SMEMR*
SA18	13	IOV*
SA17	14	IOR*
SA16	15	DACK3*
SA15	16	DR03
SA14	17	DACK1*
SA13	18	DR01
SA12	19	REF*
SA11	20	CLK
SA10	21	IR07
SA9	22	IR06
SA8	23	IR05
SA7	24	IR04
SA6	25	IR03
SA5	26	DACK2*
SA4	27	T/C
SA3	28	BALE
SA2	29	+5
SA1	30	OSC
SA0	31	GND

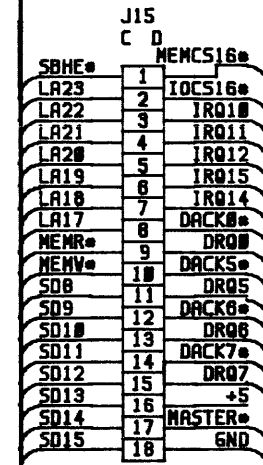
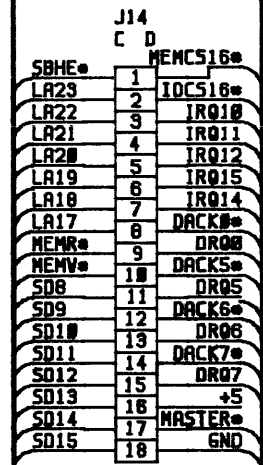
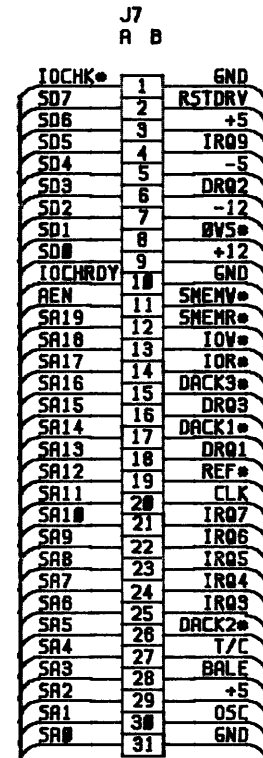
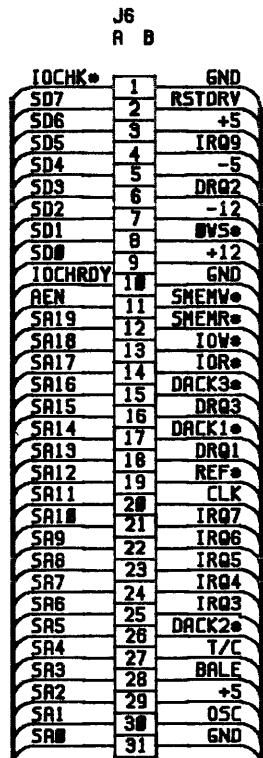
J12
C D

SBHE*	1	MEMCS16*
LA23	2	IOCS16*
LA22	3	IR010
LA21	4	IR011
LA20	5	IR012
LA19	6	IR015
LA18	7	IR014
LA17	8	DACK0*
MEMR*	9	DR00
MEMV*	10	DACK5*
SD8	11	DR05
SD9	12	DACK6*
SD10	13	DR06
SD11	14	DACK7*
SD12	15	DR07
SD13	16	+5
SD14	17	MASTER*
SD15	18	GND

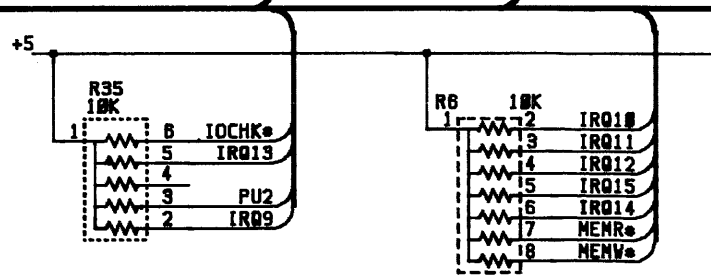
J13
C D

SBHE*	1	MEMCS16*
LA23	2	IOCS16*
LA22	3	IR010
LA21	4	IR011
LA20	5	IR012
LA19	6	IR015
LA18	7	IR014
LA17	8	DACK0*
MEMR*	9	DR00
MEMV*	10	DACK5*
SD8	11	DR05
SD9	12	DACK6*
SD10	13	DR06
SD11	14	DACK7*
SD12	15	DR07
SD13	16	+5
SD14	17	MASTER*
SD15	18	GND

 VLSI TECHNOLOGY, INC.		
VLSI 286 12MHZ PC/AT		
E	DRAWING NO. 07091501-5	REV C.2
DATE:	6/1/88	SHEET 7 OF 8



I/O CHANNEL



J8
A B

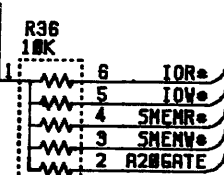
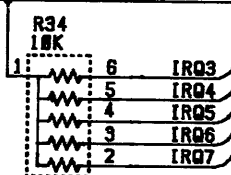
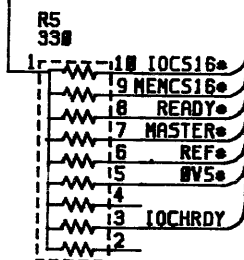
IOCHK*	1	GND
SD7	2	RSTDRV
SD6	3	+5
SD5	4	IR09
SD4	5	-5
SD3	6	DR02
SD2	7	-12
SD1	8	#V5*
SD0	9	+12
IOCHRDY	10	GND
AEN	11	SMEHV*
SA19	12	SMEMR*
SA18	13	IOV*
SA17	14	IOR*
SA16	15	DACK3*
SA15	16	DR03
SA14	17	DACK1*
SA13	18	DR01
SA12	19	REF*
SA11	20	CLK
SA10	21	IR07
SA9	22	IR06
SA8	23	IR05
SA7	24	IR04
SA6	25	IR03
SA5	26	DACK2*
SA4	27	T/C
SA3	28	BALE
SA2	29	+5
SA1	30	OSC
SA0	31	GND

J9
A B


IOCHK*	1	GND
SD7	2	RSTDRV
SD6	3	+5
SD5	4	IR09
SD4	5	-5
SD3	6	DR02
SD2	7	-12
SD1	8	#V5*
SD0	9	+12
IOCHRDY	10	GND
AEN	11	SMEHV*
SA19	12	SMEMR*
SA18	13	IOV*
SA17	14	IOR*
SA16	15	DACK3*
SA15	16	DR03
SA14	17	DACK1*
SA13	18	DR01
SA12	19	REF*
SA11	20	CLK
SA10	21	IR07
SA9	22	IR06
SA8	23	IR05
SA7	24	IR04
SA6	25	IR03
SA5	26	DACK2*
SA4	27	T/C
SA3	28	BALE
SA2	29	+5
SA1	30	OSC
SA0	31	GND

J16
C D

SBHE*	1	MEMCS16*
LA23	2	IOCS16*
LA22	3	IR010
LA21	4	IR011
LA20	5	IR012
LA19	6	IR015
LA18	7	IR014
LA17	8	DACK0*
MEMR*	9	DR00
MEMV*	10	DACK5*
SD8	11	DR05
SD9	12	DACK6*
SD10	13	DR08
SD11	14	DACK7*
SD12	15	DR07
SD13	16	+5
SD14	17	MASTER*
SD15	18	GND



7

 VLSI TECHNOLOGY, INC.		
VLSI 286 12MHZ PC/AT		
E	DRAWING NO. 07091501-5	REV C.2
DATE:	6/1/88	SHEET 8 OF 8