Winbond Electronics Corp.

I/O COUPLER

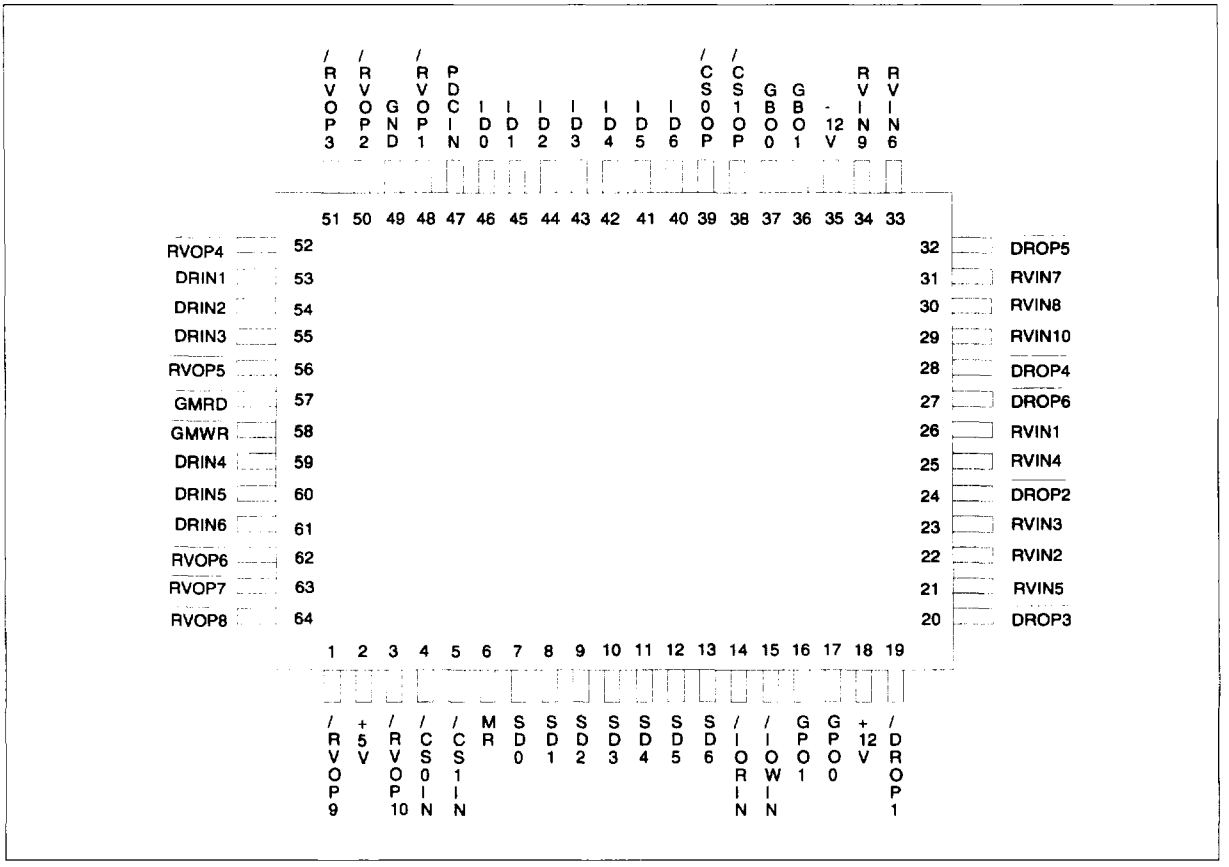
GENERAL DESCRIPTION

The W83758F is an I/O-coupler chip that includes six line drivers (1488), ten line receivers (1489), two timers (556), an IDE control signal buffer (74244), and an IDE data bus transceiver (74245). It also supports a power-down control circuit to reduce power consumption. This chip is intended for use with a super I/O controller, and it is specifically designed to match the pin assignments of the Winbond Super I/O series. With this chip, engineers can easily design an all-in-one I/O circuit for personal computer systems without using any other TTL ICs.

FEATURES

- Six line drivers (1488), ten line receivers (1489), two timers (556), IDE control signal buffer (74244), and IDE data bus transceiver (74245)
- Supports two RS232 serial ports and game port control logic
- Power-down control function available
- Four power supplies needed: 0V, +5V, +12V, and -12V
- 64-pin QFP package

PIN CONFIGURATION



PIN DESCRIPTION

Power Pins

PIN NO.	SYMBOL	I/O	DESCRIPTION
49	GND	-	Ground
2	+5V	-	+5V Power
18	+12V	-	+12V Power
35	-12V	-	-12V Power

Line Driver

PIN NO.	SYMBOL	I/O	DESCRIPTION
53	DRIN1	I	Driver input 1
54	DRIN2	I	Driver input 2
55	DRIN3	I	Driver input 3
59	DRIN4	I	Driver input 4
60	DRIN5	I	Driver input 5
61	DRIN6	I	Driver input 6
19	$\overline{\text{DROP1}}$	O	Driver output 1
24	$\overline{\text{DROP2}}$	O	Driver output 2
20	$\overline{\text{DROP3}}$	O	Driver output 3
28	$\overline{\text{DROP4}}$	O	Driver output 4
32	$\overline{\text{DROP5}}$	O	Driver output 5
27	$\overline{\text{DROP6}}$	O	Driver output 6

Line Receiver

PIN NO.	SYMBOL	I/O	DESCRIPTION
26	RVIN1	I	Receiver input 1
22	RVIN2	I	Receiver input 2
23	RVIN3	I	Receiver input 3
25	RVIN4	I	Receiver input 4
21	RVIN5	I	Receiver input 5
33	RVIN6	I	Receiver input 6
31	RVIN7	I	Receiver input 7
30	RVIN8	I	Receiver input 8

Line Receiver, continued

PIN NO.	SYMBOL	I/O	DESCRIPTION
34	RVIN9	I	Receiver input 9
29	RVIN10	I	Receiver input 10
48	$\overline{\text{RVOP1}}$	I/O	During normal operation, this pin works as receiver output #1. During power-on reset, this pin is used to select power-down control (PDC) mode enable level. When $\overline{\text{RVOP1}}$ is set to high at power on, PDC is high active. When $\overline{\text{RVOP1}}$ is set to low at power on, PDC is low active.
50	$\overline{\text{RVOP2}}$	O	Receiver output 2
51	$\overline{\text{RVOP3}}$	O	Receiver output 3
52	$\overline{\text{RVOP4}}$	O	Receiver output 4
55	$\overline{\text{RVOP5}}$	O	Receiver output 5
62	$\overline{\text{RVOP6}}$	O	Receiver output 6
63	$\overline{\text{RVOP7}}$	O	Receiver output 7
64	$\overline{\text{RVOP8}}$	O	Receiver output 8
1	$\overline{\text{RVOP9}}$	O	Receiver output 9
3	$\overline{\text{RVOP10}}$	O	Receiver output 10

Game Port

PIN NO.	SYMBOL	I/O	DESCRIPTION
17	GPO0	I/O	Game port RC constant (open drain)
16	GPO1	I/O	Game port RC constant (open drain)
37	GBO0	I	Game port button input
36	GBO1	I	Game port button input
57	$\overline{\text{GMRD}}$	I	Game port read This pin is internally OR-gated with $\overline{\text{IORIN}}$, so the game port works even if this pin is connected to game port chip select signal $\overline{\text{GMCS}}$.
58	$\overline{\text{GMWR}}$	I	Game port write This pin is internally OR-gated with $\overline{\text{IOWIN}}$, so the game port works even if this pin is connected to game port chip select signal $\overline{\text{GMCS}}$.

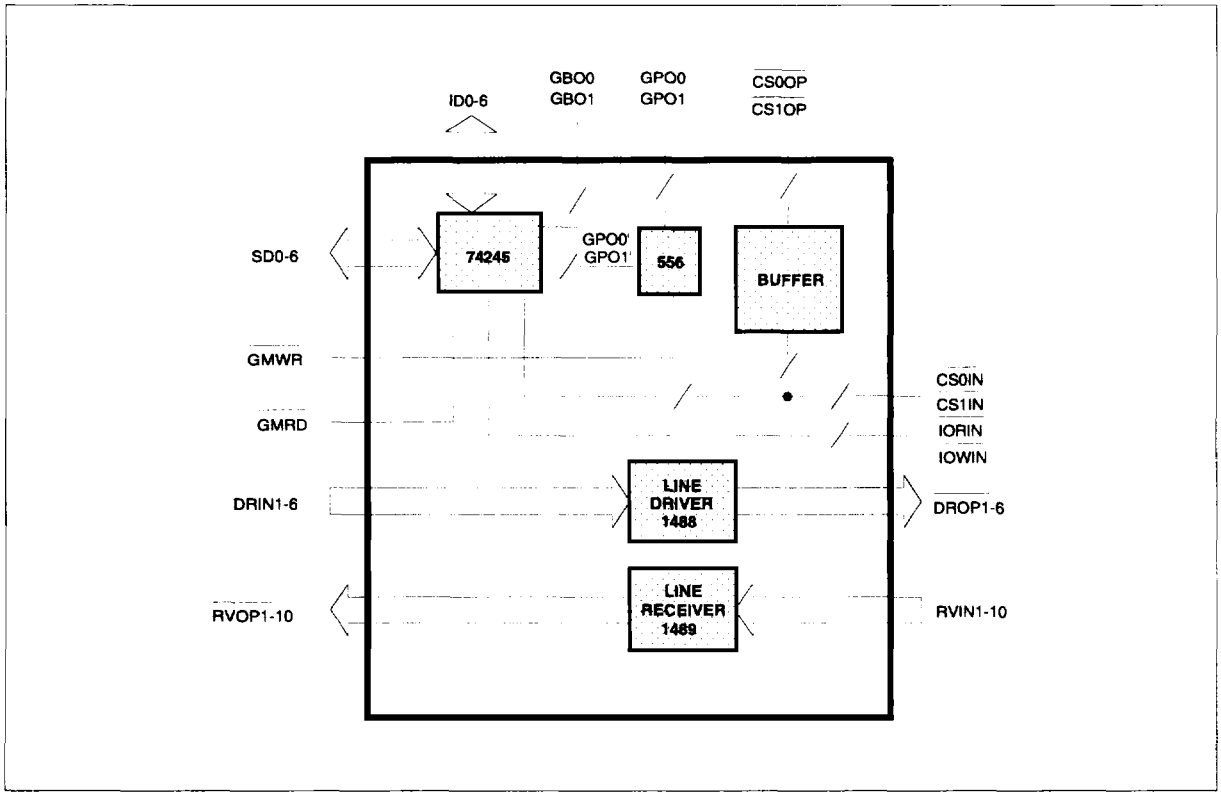
Control Signals

PIN NO.	SYMBOL	I/O	DESCRIPTION
6	MR	I	Master reset signal input
14	$\overline{\text{IORIN}}$	I	I/O read signal input (from host system)
15	$\overline{\text{IOWIN}}$	I	I/O write signal input (from host system)
4	$\overline{\text{CS0IN}}$	I	IDE select signal 0 input (this pin must be pulled high if it is not connected to IDE select signal 0)
5	$\overline{\text{CS1IN}}$	I	IDE select signal 1 input (this pin must be pulled high if it is not connected to IDE select signal 1)
39	$\overline{\text{CS0OP}}$	O	IDE select signal 0 output
38	$\overline{\text{CS1OP}}$	O	IDE select signal 1 output
47	PDCIN	I	This pin is used to enable/disable the power down function. The active level of this pin depends on how pin $\overline{\text{RVOP1}}$ is programmed at power-on. If $\overline{\text{RVOP1}}$ is set high at power on, for example, then setting PDCIN to high will cause the W83758F to enter power-down mode.

Data Bus

PIN NO.	SYMBOL	I/O	DESCRIPTION
7	SD0	I/O	System data bit 0
8	SD1	I/O	System data bit 1
9	SD2	I/O	System data bit 2
10	SD3	I/O	System data bit 3
11	SD4	I/O	System data bit 4
12	SD5	I/O	System data bit 5
13	SD6	I/O	System data bit 6
46	ID0	I/O	IDE data bit 0
45	ID1	I/O	IDE data bit 1
44	ID2	I/O	IDE data bit 2
43	ID3	I/O	IDE data bit 3
42	ID4	I/O	IDE data bit 4
41	ID5	I/O	IDE data bit 5
40	ID6	I/O	IDE data bit 6

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Block 74245

The IDE low byte data bits (except for bit 7) are connected to the host data bus via this transceiver. The transceiver is controlled by $\overline{\text{IORIN}}$ to read from the IDE data bus and by $\overline{\text{IOWIN}}$ to write to the bus.

This transceiver also functions as a buffer for reading game port buttons GBO0 and GBO1 and the status of block 556 output signals GPO0' and GPO1' on bits 4, 5, 0, and 1, respectively.

Block 556

This block contains two independent 555-type timing circuits for generating two separate one-shot signals, which may be used to measure the RC inputs of the game port. The $\overline{\text{GMWR}}$ signal is the trigger signal of block 556.

Line Driver Block 1488

This block contains six line drivers that are designed to serve as an interface between data terminal equipment and data communications equipment in conformance with the specifications of EIA standard No. RS-232C. The power requirements are +12V, 0V, and -12V.

Line Receiver Block 1489

This block contains ten line receivers that are designed to serve as an interface between data terminal equipment and data communications equipment in conformance with the specifications of EIA standard no. RS-232C. The power requirements are +12V, 0V, and -12V.

Buffer Block

This block consists of buffers for IDE select signals.

Power-Down Control Mode

When pin PDCIN is set active (active high or low is determined by $\overline{\text{RVOP1}}$ at power-on reset), the W83758F enters power-down mode and all output buffers (SD0-SD6, $\overline{\text{RVOP1}}$-$\overline{\text{RVOP10}}$, $\overline{\text{DROP1}}$-$\overline{\text{DROP6}}$) enter tri-state to reduce power consumption.

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
Power Supply Voltage	GND, Vcc	-0.3 to 7.0	V
	Vss, VDD	-14 to 14	
Input Voltage	Low Voltage	-0.5 to 7.0	V
	High Voltage	-12 to 12	
Operating Temperature		0 to 70	°C
Storage Temperature		-55 to +150	°C

DC CHARACTERISTICS

Ta= 0 to +70° C, Vcc= 5V, VDD= 12V, Vss= -12V, GND= 0V

PARAMETER	SYMBOL	MIN.	MAX.	NOTES
Input low voltage	VIL(TTL)	-0.3V	+0.6V	MR, $\overline{\text{GMRD}}$, $\overline{\text{GMWR}}$, $\overline{\text{IORIN}}$, $\overline{\text{IOWIN}}$, $\overline{\text{CS0IN}}$, $\overline{\text{CS1IN}}$
Input high voltage	VIH(TTL)	+2.4V	Vcc+0.3V	MR, $\overline{\text{GMRD}}$, $\overline{\text{GMWR}}$, $\overline{\text{IORIN}}$, $\overline{\text{IOWIN}}$, $\overline{\text{CS0IN}}$, $\overline{\text{CS1IN}}$
Input low voltage	VIL (CMOS)	-0.3V	0.2 Vcc	DRIN1-6, GBO0, GBO1, GPO0, GPO1, SD0-6, PDCIN, ID0-6
Input high voltage	VIH (CMOS)	+3.9 V	Vcc+0.3V	DRIN1-6, GBO0, GBO1, GPO0, GPO1, SD0-6, PDCIN, ID0-6
Input low voltage	VIL (HI-V)	Vss	GND	RVIN1-10
Input high voltage	VIH (HI-V)	2V	VDD	RVIN1-10
Output low voltage	VOL	-	0.4V	$\overline{\text{CS0OP}}$, $\overline{\text{CS1OP}}$, $\overline{\text{RVOP1}}$-10

DC characteristics, continued

PARAMETER	SYMBOL	MIN.	MAX.	NOTES
Output high voltage	VOH	+2.4V	-	$\overline{CS0OP}$, $\overline{CS1OP}$, $\overline{RVOP1}$-10
Output low voltage	VOL (HI-V)	Vss	-2V	$\overline{DROP1}$-6
Output high voltage	VOH (HI-V)	+2V	VDD	$\overline{DROP1}$-6

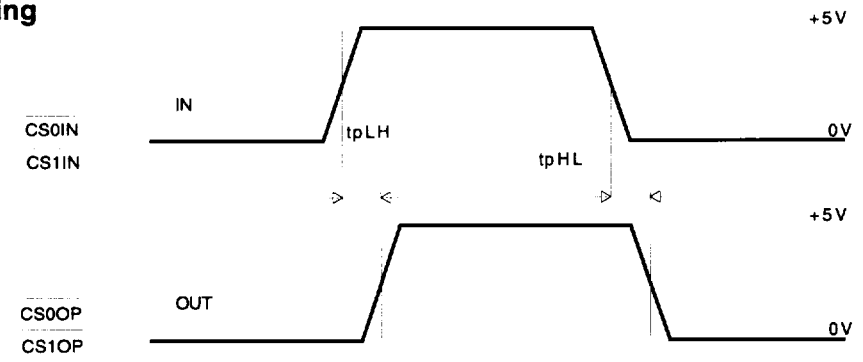
SYMBOL	CURRENT LEVEL					
	MAX.		MIN.		TYP.	
	IIL	IIH	IOL	IOH	IOL	IOH
MR	-20 µA	3 µA	-	-	-	-
$\overline{CS0IN}$, $\overline{CS1IN}$	-20 µA	3 µA	-	-	-	-
$\overline{IOWIN}$, $\overline{IORIN}$	-20 µA	3 µA	-	-	-	-
PDCIN	-20 µA	3 µA	-	-	-	-
$\overline{GMWR}$, $\overline{GMRD}$	-20 µA	3 µA	-	-	-	-
GBO0, GBO1	-20 µA	3 µA	-	-	-	-
RVIN1-10	-1mA	3 µA	-	-	-	-
GPO0, GPO1	-	-	1.5 mA	-	2 mA	-
$\overline{CS0OP}$, $\overline{CS1OP}$	-	-	7mA	5.5 mA	10 mA	9 mA
ID0-6	-	-	7mA	5.5 mA	11mA	9 mA
SD0-6	-	-	7mA	5 mA	10 mA	8 mA
$\overline{RVOP1}$-10	-	-	2 mA	2 mA	3 mA	3 mA
$\overline{DROP1}$-6	-	-	10 mA	10 mA	18 mA	18 mA

AC CHARACTERISTICS

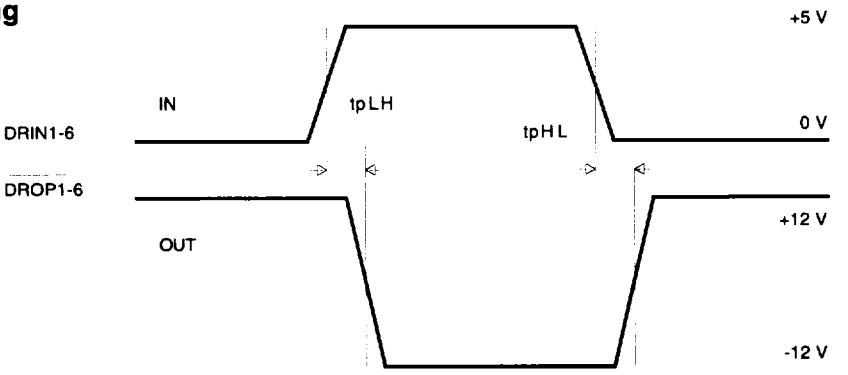
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
1488 tpLH	DRIN1-6	-	60	90	nS
1488 tpHL	$\overline{\text{DROP1}}$-6	-	60	90	nS
1489 tpLH	RVIN1-10	-	60	90	nS
1489 tpHL	$\overline{\text{RVOP1}}$-10	-	60	90	nS
tpLH	MR	-	50	70	nS
tpLH	$\overline{\text{CS0IN}}$, $\overline{\text{CS1IN}}$, $\overline{\text{IORIN}}$, $\overline{\text{IOWIN}}$	-	70	120	nS
tpHL	$\overline{\text{CS0OP}}$, $\overline{\text{CS1OP}}$	-	70	120	nS
tD	SD0-6	-	90	120	nS
tisLH	ID to SD	-	80	130	nS
tisHL	ID to SD	-	60	110	nS
tsiLH	SD to ID	-	60	110	nS
tsiHL	SD to ID	-	45	95	nS

TMING WAVEFORMS

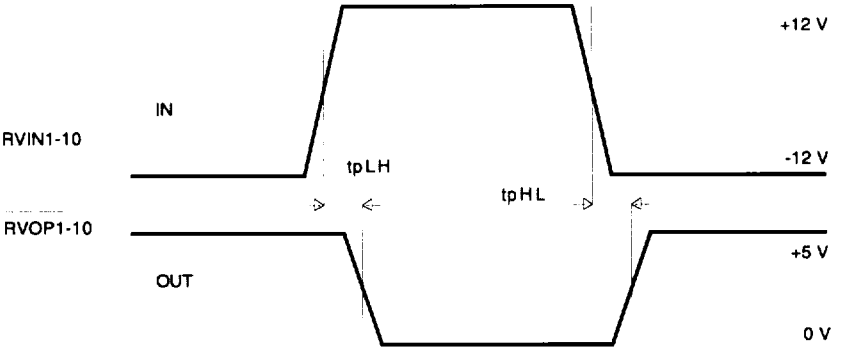
Buffer Timing



Driver Timing

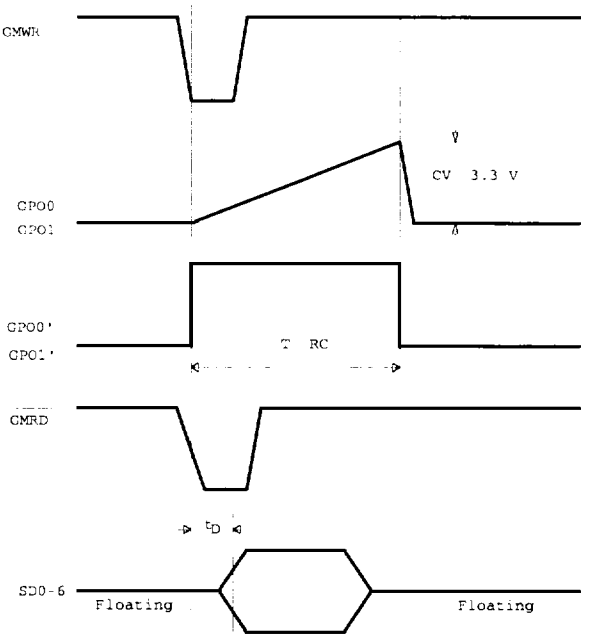


Receiver Timing



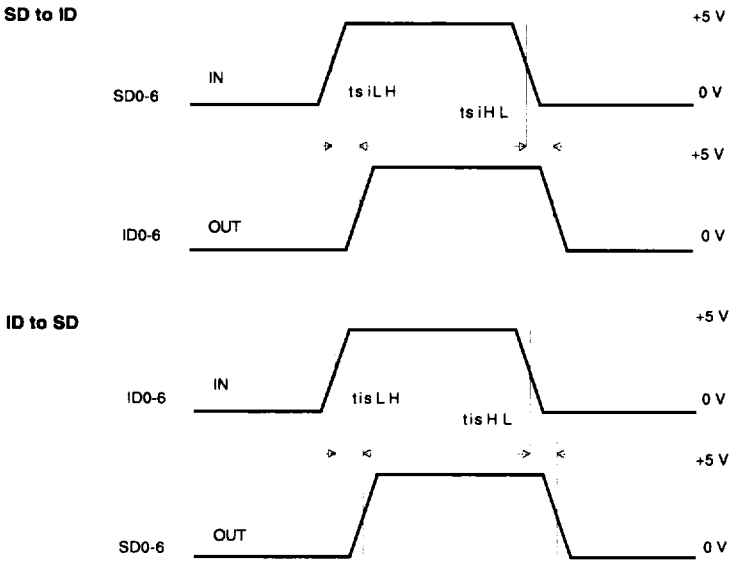
Timing waveforms, continued

Timer Timing

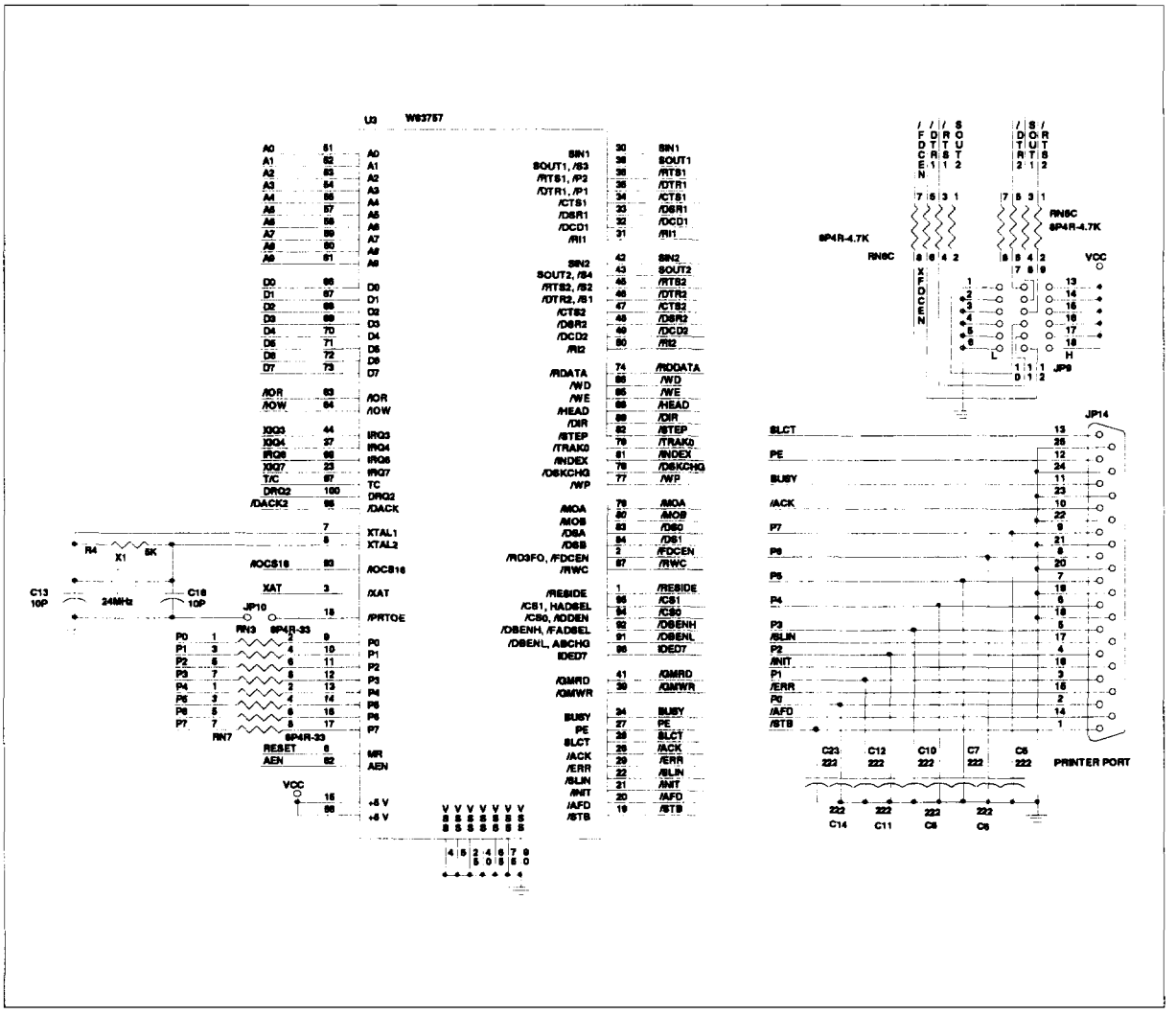


Data Valid

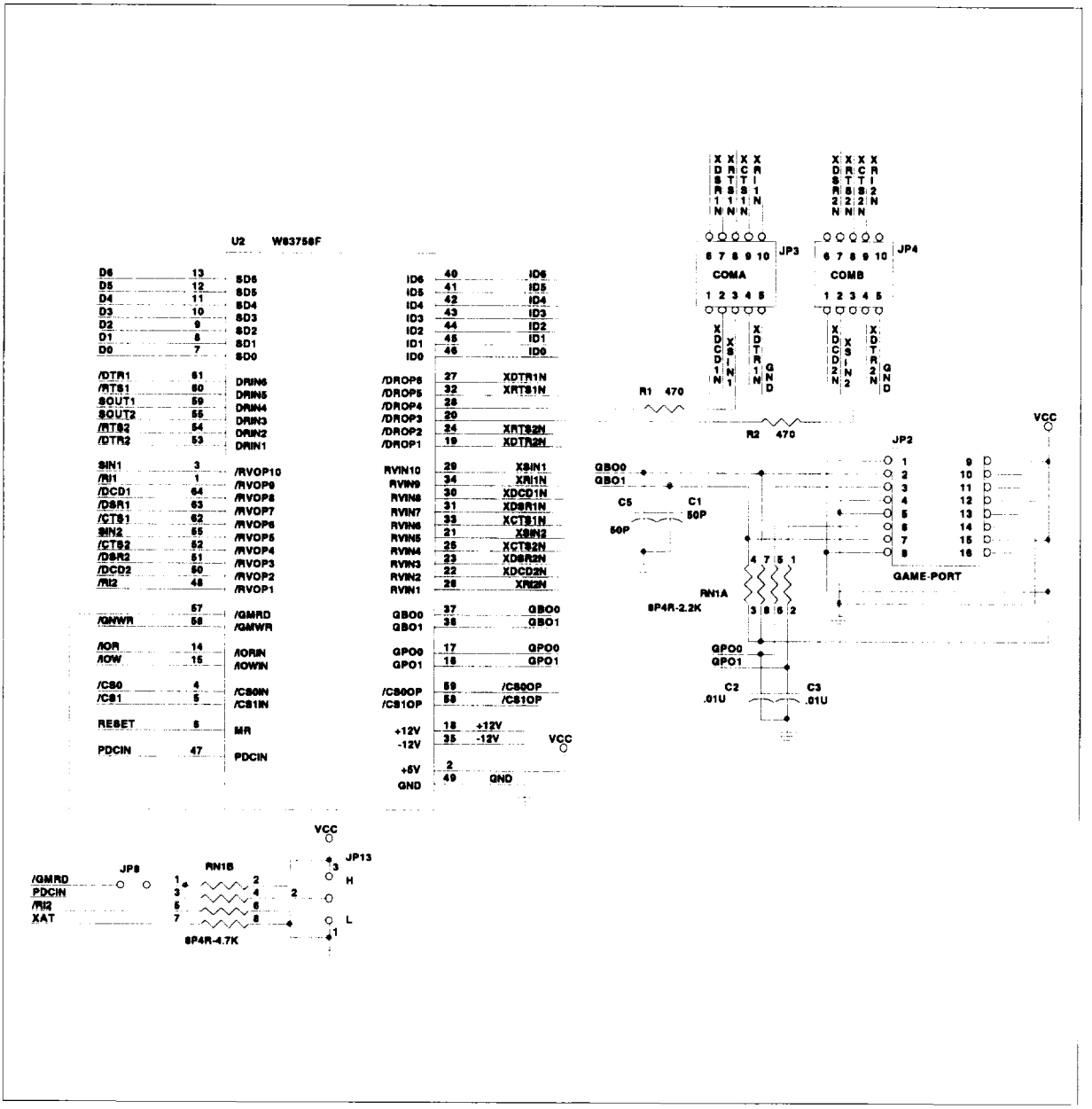
IDE Buffer Timing



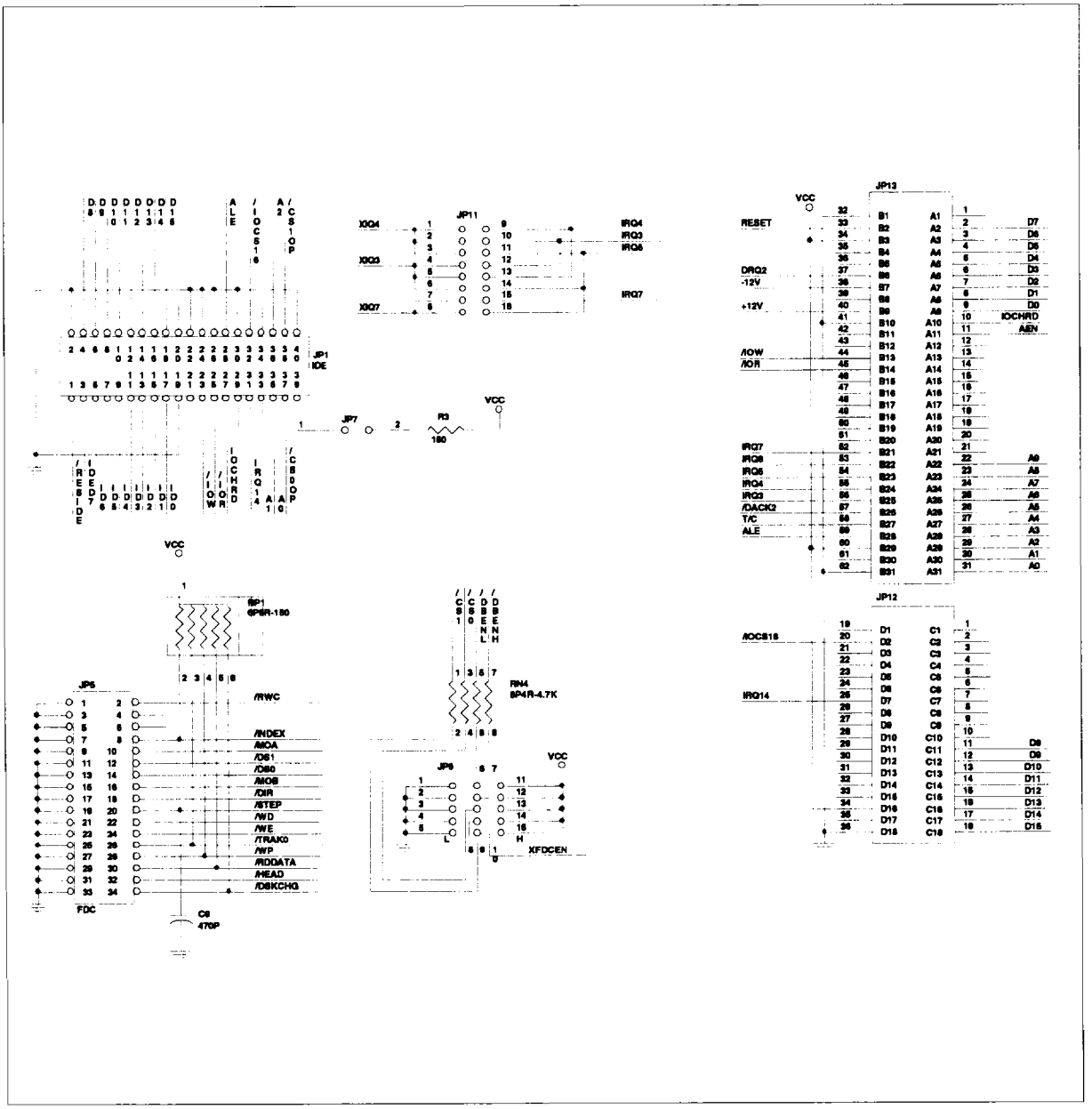
APPLICATION CIRCUIT



Application circuit, continued



Application circuit, continued



Application circuit, continued

JP1 IDE CONNECTOR

JP2 GAME PORT

JP3 RS232-1 (COMA)

JP4 RS232-2 (COMB)

JP5 FDD CONNECTOR

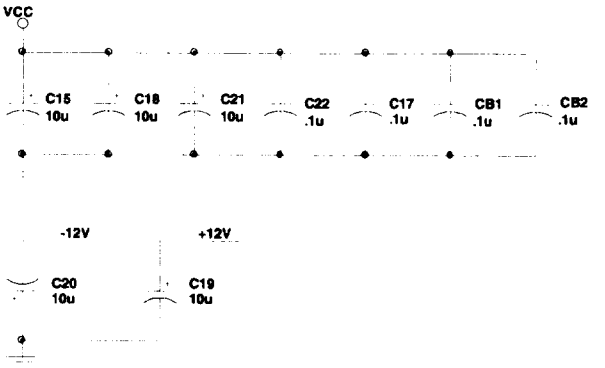
JP7 LED CONNECTOR

JP8 SHORT - GAME PORT ENABLE
OPEN - GAME PORT DISABLE

JP10 SHORT - PRINTER AS O/P PORT
OPEN - PRINTER AS I/O PORT

JP12 H PDC DISABLE
L PDC ENABLE

JP14 PRINTER PORT



JP6
1 ABCHG
H AB CHG MODE
L NORMAL
2 FADSEL
H 3F0-3F7
L 370-377
3 IDE
H DISABLE
L ENABLE
4 HADSEL
H 3F6,3F7,1F0-1F7
L 376,377,170-177
5 FDC
H DISABLE
L ENABLE

JP9

1	2	RS232-1 (COMA)
L	L	COM4 (2E8H)
L	H	COM1 (3F8H)
H	L	COM3 (3E8H)
H	H	DISABLE

3	4	RS232-2 (COMB)
L	L	COM3 (3E8H)
L	H	COM2 (2F8H)
H	L	COM4 (2E8H)
H	H	DISABLE

5	6	PRINTER
L	L	LPT3 (3BCH)
L	H	LPT2 (278H)
H	L	LPT1 (378H)
H	H	DISABLE

JP11

1	2	3	RS232-1 (COMA)
ON			IRQ4
	ON		IRQ3
		ON	IRQ5

4	5	6	RS232-2 (COMB)
ON			IRQ3
	ON		IRQ4
		ON	IRQ5

7	8	PRINTER
ON		IRQ7
	ON	IRQ5

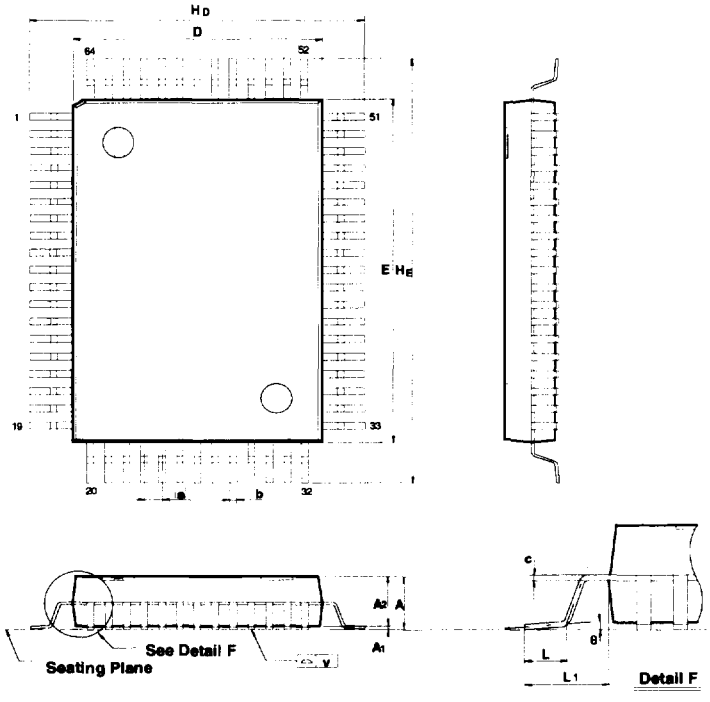
DEFAULT :
JP8 SHORT
JP10 SHORT
JP11 1,4,7 SHORT
(COMA-IRQ4;COMB-IRQ3;PRT-IRQ7)
JP13 H

JP6 :
1 L
2 H
3 L
4 H
5 L

JP9 :
1 L
2 H
3 L
4 H
5 H
6 L

PACKAGE DIMENSIONS

68-pin QFP



Symbol	Dimension in inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.130	—	—	3.30
A_1	0.004	—	—	0.10	—	—
A_2	0.107	0.112	0.117	2.73	2.85	2.97
b	0.014	0.016	0.020	0.35	0.40	0.50
c	0.004	0.006	0.010	0.10	0.15	0.25
D	0.546	0.551	0.556	13.87	14.00	14.13
E	0.782	0.787	0.792	19.87	20.00	20.13
e	0.033	0.039	0.045	0.85	1.00	1.15
H_D	0.728	0.740	0.752	18.49	18.80	19.10
H_E	0.964	0.976	0.988	24.49	24.80	25.10
L	0.039	0.047	0.055	1.00	1.20	1.40
L_1	0.087	0.094	0.103	2.21	2.40	2.62
y	—	—	0.004	—	—	0.10
θ	0°	—	12°	0°	—	12°

Notes:

1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeters
4. General appearance spec. should be based on final visual inspection spec.

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Note: All data and specifications are subject to change without notice.

Publication Release Date: November 1994
Revision A2