VT6306
PCI 1394a Integrated Host Controller

1394a OHCI Link Layer Controller with Integrated 400 Mbit 3-Port PHY for the PCI Bus

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VIA TECHNOLOGIES, INC.

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REVISION HISTORY

Document Release	Date	Revision	Initials
1.0	11/1/00	Initial public release (no technical changes from internal 8/29/00 revision 0.4)	DH
1.11	10/30/01	Updated Application Schematics Diagram from VT5350C to VT5471B Fixed cross reference links and Functional Description heading levels Fixed formatting of revision number cross reference in page footer	AT / DH

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PCI 1394A INTEGRATED HOST CONTROLLER

1394A OHCI HOST CONTROLLER WITH INTEGRATED 3-PORT 400 MBIT PHY FOR THE PCI BUS

- **Single Chip PCI Host Controller for IEEE 1394-1995 and IEEE 1394a Draft 4.0**
- **Embedded 1394 Link Core**
  - 32 bit CRC generator and checker for receive and transmit data
  - On-chip isochronous and asynchronous receive and transmit FIFOs for packets (2K for general receive plus 2K for isochronous transmit plus 2K for asynchronous transmit)
  - 8 isochronous transmit / receive contexts
  - 3-deep physical post-write queue
  - 2-deep physical response queue
  - Dual buffer mode enhancements
  - Skip Processing enhancements
  - Block Read Request handling
  - Ack_tardy processing
- **OHCI Compliant Programming Interface**
  - Compliant with 1394 Open HCI Specifications v1.0 and v1.1
  - Descriptor based isochronous and asynchronous DMA channels for receive / transmit packets
- **32-Bit Power-Managed PCI Bus Interface**
  - Compliant with PCI specification v2.2
  - High-performance bus mastering support
  - Byte alignment to run in little-endian (x86/PCI) environment
  - Compliant with PCI Bus Power Management Specification v1.1
  - Supports power states D0, D1, D2, D3hot, and D3cold
  - Supports CardBus interface
- **Supports I2C EEPROM and 4-Wire Serial ROM with GUID PROM Shadow to EEPROM**

- **Integrated 400 Mbit 3-Port PHY**
  - Supports provisions of IEEE 1394-1995 Standard for High Performance Serial Bus and the P1394a Supplement 4.0.
  - Fully interoperable with IEEE Std 1394-1995 devices
  - Full P1394a Supplement Support includes:
    - Arbitrated short reset,
    - Enhanced priority arbitration,
    - Connection debounce,
    - Multispeed packet concatenation,
    - Ack accelerated arbitration,
    - Fly-by concatenation,
    - Per port disable, suspend, resume, through register write and remote command packet,
    - Remote access packet
    - Boundary node short reset
    - No phy_ID wrap past 63
  - –Provides three 1394a fully compliant cable ports at 100/200/400 Mbit per second
  - Host notification of PHY LinkOn events
  - Logic performs bus initialization and arbitration functions
  - Encode and decode functions included for data-strobe bit-level encoding
  - Incoming data resynchronized to local clock.
  - 24.576 MHz crystal oscillator and PLL provide TX/RX data at 100/200/400 Mbps and Link-Layer Controller clock at 49.152 MHz.
  - Cable power presence monitoring.
  - Programmable node power class information for system power management
  - Fully Compliant P1394a 4.0 PHY register map
  - Separate TPBIAS for each port
  - Cable ports monitor line conditions for active connection to remote node
  - Automatic power down inactive circuit and logic for low power application
  - Self power up reset and pinless PLL to reduce passive component counts on system
  - Automatic configuration to single-port, two-port, and three-port applications; unused ports power down automatically
  - Dedicated power supply pins separate from link core
  - 2KV ESD protection
- **3.3V Power Supply with 5V Tolerant Inputs**
- **0.35um, Low Power CMOS Process**
- **128-Pin PQFP Package (VT6306) and 128-Pin LQFP Package (VT6306L) Available**
- **PCB Reference Designs & Schematics Available**

OVERVIEW

The VT6306 IEEE 1394 OHCI Host Controller provides high performance serial connectivity. It implements the Link and Phy layers for IEEE 1394-1995 High Performance Serial Bus and 1394a Draft 4.0. It is compliant with 1394 Open HCI 1.0 and 1.1 with DMA engine support for high performance data transfer via a 32-bit bus master PCI host bus interface.

The VT6306 supports 100, 200 and 400 Mbit/sec transmission via an integrated 3-port PHY. The VT6306 services two types of data packets: asynchronous and isochronous (real time). The 1394 link core performs arbitration requesting, packet generation and checking, and bus cycle master operations. It also has root node capability and performs retry operations.

The VT6306 is ready to provide industry-standard IEEE 1394 peripheral connections for desktop and mobile PC platforms. Support for the VT6306 is built into Microsoft Windows 98, Windows ME, and Windows 2000.

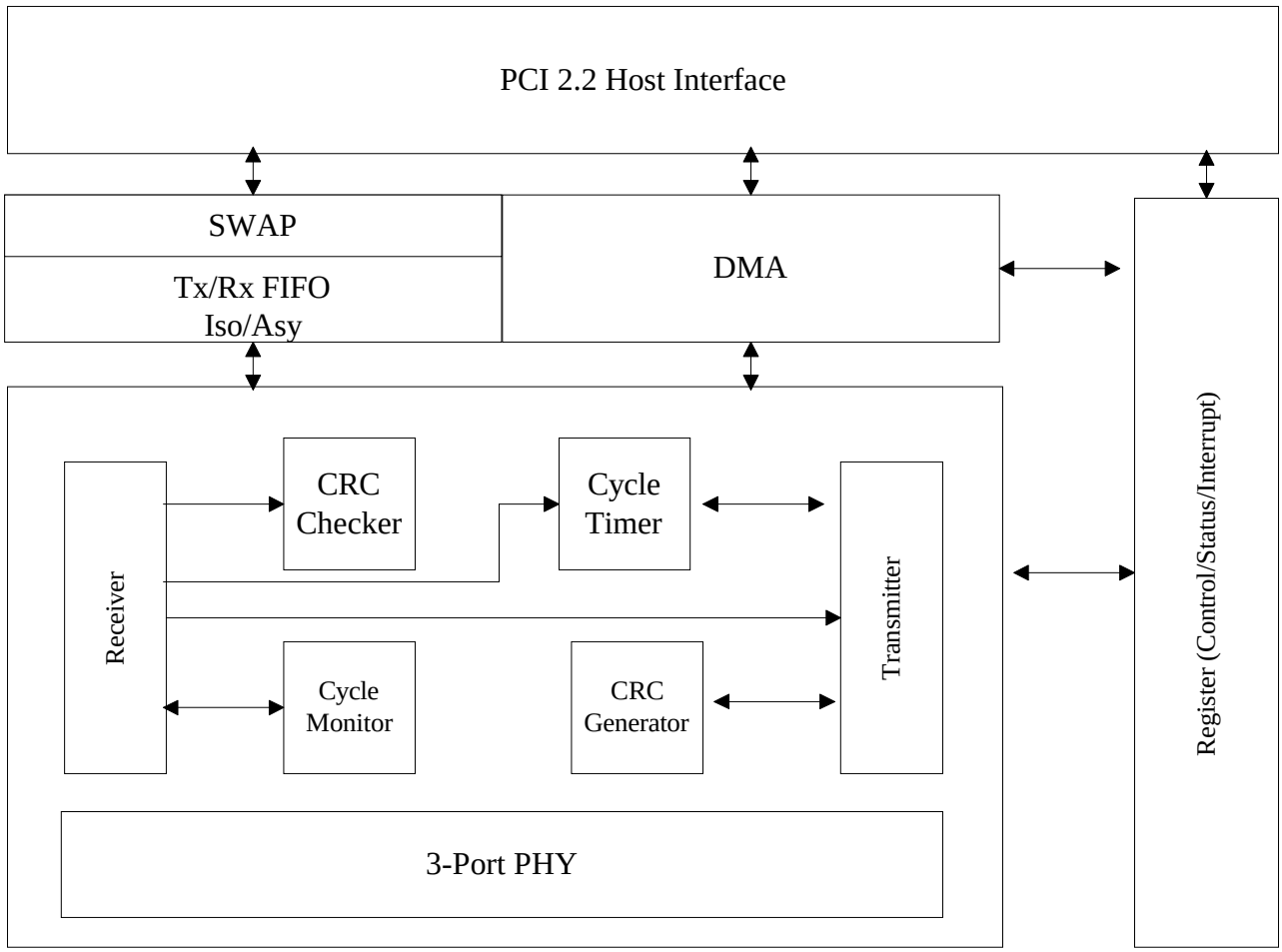


Figure 1. VT6306 Chip Block Diagram

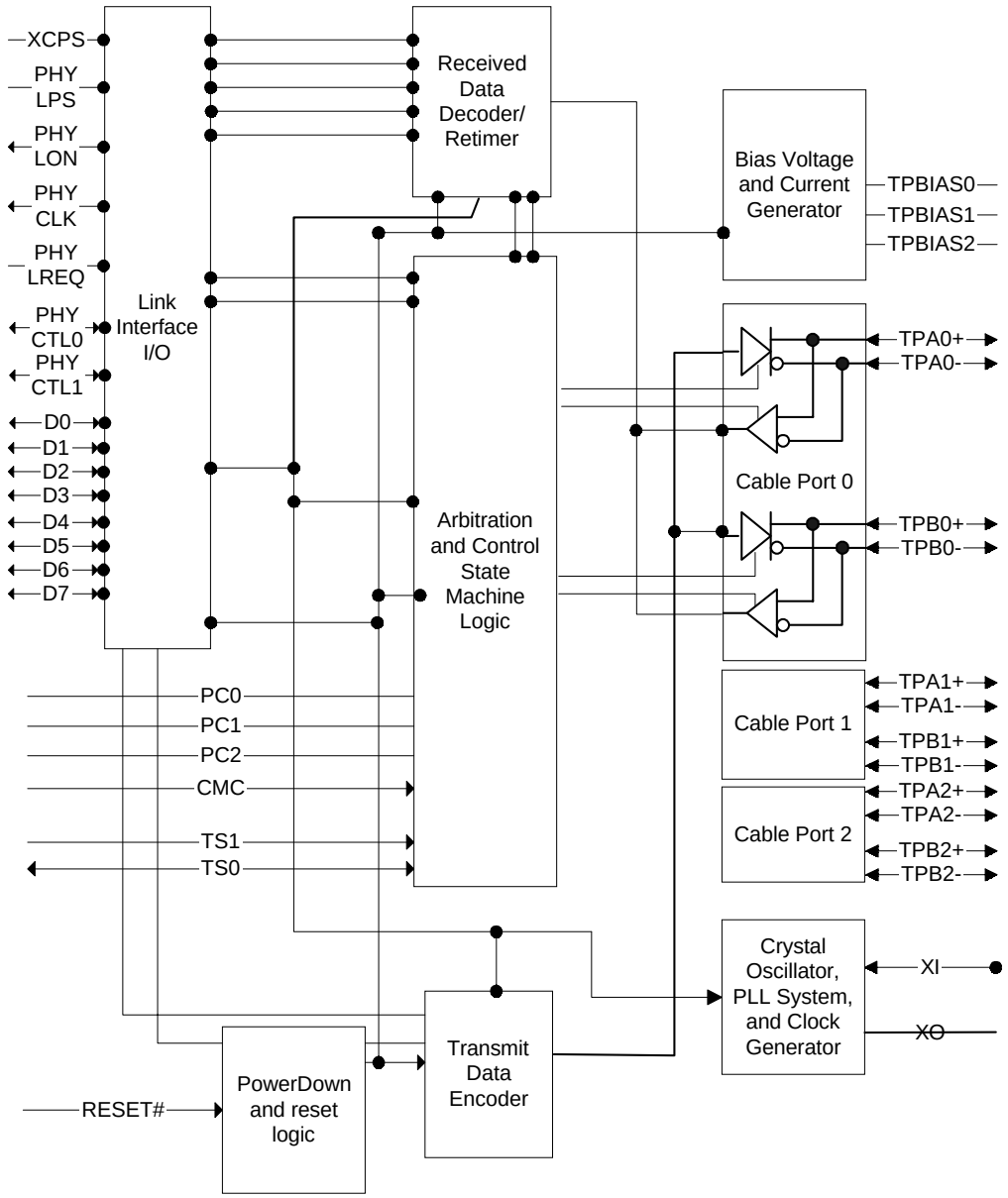


Figure 2. VT6306 Internal PHY Block Diagram

PINOUTS

Pin Diagram

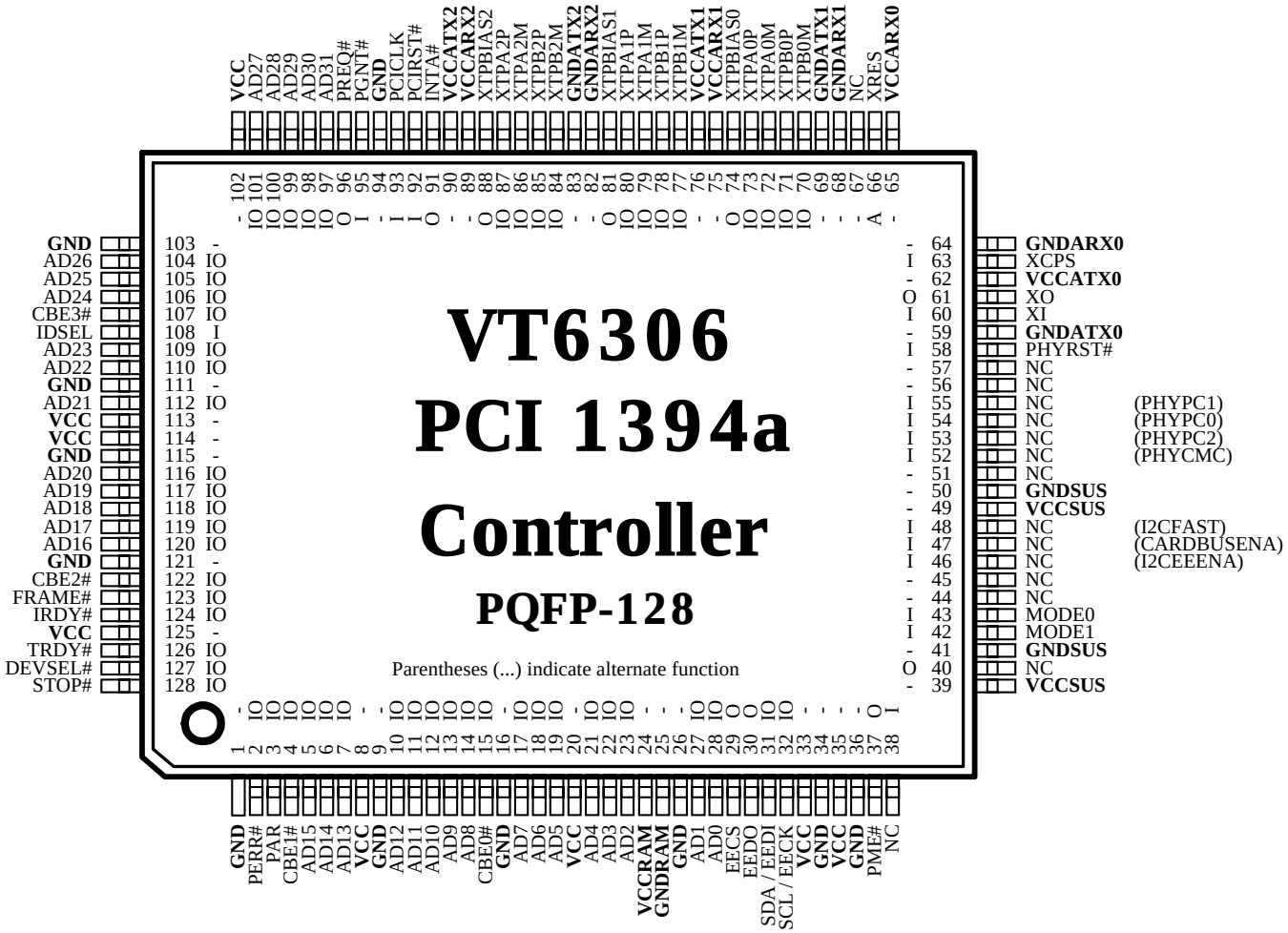


Figure 3. VT6306 Pin Diagram (Top View)

Pin List

Figure 4. VT6306 Pin List (Alphabetical Order)

Pin		Pin Name	Pin		Pin Name	Pin		Pin Name	Pin		Pin Name
28	IO	AD00	47	I	CARDBUSENA	48	I	I2CFAST	**102**	**P**	**VCC**
27	IO	AD01	15	IO	CBE0#	108	I	IDSEL	**113**	**P**	**VCC**
23	IO	AD02	4	IO	CBE1#	91	O	INTA#	**114**	**P**	**VCC**
22	IO	AD03	122	IO	CBE2#	124	IO	IRDY#	**125**	**P**	**VCC**
21	IO	AD04	107	IO	CBE3#	43	I	MODE0	**65**	**P**	**VCCARX0**
19	IO	AD05	127	IO	DEVSEL#	42	I	MODE1	**75**	**P**	**VCCARX1**
18	IO	AD06	32	IO	EECK / SCL / EEFAST	38	-	NC	**89**	**P**	**VCCARX2**
17	IO	AD07	29	O	EECS / EEAUTO#	40	-	NC	**62**	**P**	**VCCATX0**
14	IO	AD08	31	IO	EEDI / SDA	44	-	NC	**76**	**P**	**VCCATX1**
13	IO	AD09	30	O	EEDO	45	-	NC	**90**	**P**	**VCCATX2**
12	IO	AD10	123	IO	FRAME#	51	-	NC	**24**	**P**	**VCCRAM**
11	IO	AD11	**1**	**P**	**GND**	56	-	NC	**39**	**P**	**VCCSUS**
10	IO	AD12	**9**	**P**	**GND**	57	-	NC	**49**	**P**	**VCCSUS**
7	IO	AD13	**16**	**P**	**GND**	67	-	NC	63	I	XCPS
6	IO	AD14	**26**	**P**	**GND**	3	IO	PAR	60	I	XI
5	IO	AD15	**34**	**P**	**GND**	93	I	PCICLK	61	O	XO
120	IO	AD16	**36**	**P**	**GND**	92	I	PCIRST#	66	A	XRES
119	IO	AD17	**94**	**P**	**GND**	2	O	PERR#	72	IO	XTPA0M
118	IO	AD18	**103**	**P**	**GND**	95	I	PGNT#	73	IO	XTPA0P
117	IO	AD19	**111**	**P**	**GND**	52	I	PHYCMC	79	IO	XTPA1M
116	IO	AD20	**115**	**P**	**GND**	54	I	PHYPC0	80	IO	XTPA1P
112	IO	AD21	**121**	**P**	**GND**	55	I	PHYPC1	86	IO	XTPA2M
110	IO	AD22	**64**	**P**	**GNDARX0**	53	I	PHYPC2	87	IO	XTPA2P
109	IO	AD23	**68**	**P**	**GNDARX1**	58	I	PHYRST#	70	IO	XTPB0M
106	IO	AD24	**82**	**P**	**GNDARX2**	37	O	PME#	71	IO	XTPB0P
105	IO	AD25	**59**	**P**	**GNDATX0**	96	O	PREQ#	77	IO	XTPB1M
104	IO	AD26	**69**	**P**	**GNDATX1**	128	IO	STOP#	78	IO	XTPB1P
101	IO	AD27	**83**	**P**	**GNDATX2**	126	IO	TRDY#	84	IO	XTPB2M
100	IO	AD28	**25**	**P**	**GNDRAM**	**8**	**P**	**VCC**	85	IO	XTPB2P
99	IO	AD29	**41**	**P**	**GNDSUS**	**20**	**P**	**VCC**	74	O	XTPBIAS0
98	IO	AD30	**50**	**P**	**GNDSUS**	**33**	**P**	**VCC**	81	O	XTPBIAS1
97	IO	AD31	46	I	12CEEENA	**35**	**P**	**VCC**	88	O	XTPBIAS2

Pin Descriptions

Table 1. Pin Descriptions

PCI Bus Interface				
Signal Name	**Pin #**	**I/O**	**Power**	**Signal Description**
AD[31:0]	97-101, 104-106, 109-110, 112, 116-120, 5-7, 10-14, 17-19, 21-23, 27-28	IO	**VCC**	**Address / Data Bus.** The standard PCI address and data lines. The address is driven with FRAME# assertion and data is driven or received in following cycles.
CBE[3:0]#	107, 122, 4, 15	IO	**VCC**	**Command / Byte Enable.** The command is driven with FRAME# assertion. Byte enables corresponding to supplied or requested data are driven on following clocks.
FRAME#	123	IO	**VCC**	**Frame.** Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator.
DEVSEL#	127	IO	**VCC**	**Device Select.** As an output, this signal is asserted to claim PCI transactions through positive or subtractive decoding. As an input, DEVSEL# indicates the response to a VT6306-initiated transaction and is also sampled when decoding whether to subtractively decode the cycle.
TRDY#	126	IO	**VCC**	**Target Ready.** Asserted when the target is ready for data transfer.
IRDY#	124	IO	**VCC**	**Initiator Ready.** Asserted when the initiator is ready for data transfer.
PREQ#	96	O	**VCC**	**PCI Bus Request.** Asserted by the bus master to indicate to the bus arbiter that it wants to use the bus.
PGNT#	95	I	**VCC**	**PCI Bus Grant.** Asserted to indicate that access to the bus is granted.
IDSEL	108	I	**VCC**	**Initialization Device Select.** IDSEL is used as a chip select during configuration read and write cycles.
INTA#	91	O	**VCC**	**Interrupt.** An asynchronous signal used to request an interrupt.
PCICLK	93	I	**VCC**	**PCI Clock.** Timing reference for all transactions on the PCI Bus.
PCIRST#	92	I	**VCC**	**Reset.** When detected low, an internal hardware reset is performed. PCIRST# assertion or deassertion may be asynchronous to PCLK, however, it is recommended that deassertion be synchronous to guarantee a clean and bounce free edge.
PAR	3	IO	**VCC**	**Parity.** A single parity bit is provided over AD[31:0] and C/BE[3:0]#.
PERR#	2	O	**VCC**	**Parity Error.** Parity error is asserted when a data parity error is detected.
STOP#	128	IO	**VCC**	**Stop.** Asserted by the target to request the master to stop the current transaction.

1394 PHY Interface				
Signal Name	**Pin #**	**I/O**	**Power**	**Signal Description**
PHYRST#	58	I	**VCCSUS**	**PHY Reset.** Used to reset the PHY logic. This pin can be left unconnected as there is an internal RC network that creates a 0.5 ms to 2 ms power-on reset interval. This pin can also be driven by an open-drain type driver.

Configuration Straps				
Signal Name	**Pin #**	**I/O**	**Default**	**Signal Description**
I2CEEENA	46	I	**Low**	**I2C EEPROM.** Low = Disable (4-wire EEPROM interface), High = Enable (2-wire I2C EEPROM interface using SCL / SDA)
I2CFAST	48	I	**Low**	**I2C EEPROM Fast Mode.** Low = Disable, High = Enable
CARDBUSENA	47	I	**Low**	**CardBus Mode.** Low = Disable (PCI), High = Enable
PHYPC[2:0]	53, 55, 54	I		**Power Class.** Used to set the three POWER_CLASS bits in the Self-ID packet. These bits describe the power consumption and source characteristics of the node. PC0, 1, and 2 are reflected in Self-ID packet bits 21, 22, and 23 respectively. See Table 7 “Power Class Pin Strapping” on page 39 for additional information.
PHYCMC	52	I	**High**	**Programmable Contender / Bus Manager Capable.** High specifies that the node is capable of being a bus manager.

Cable Interface and PHY Signals				
Signal Name	**Pin #**	**I/O**	**Power**	**Signal Description**
XTPA0P	73	IO	**VCCSUS**	**Port 0 Twisted Pair A Positive.**
XTPA0M	72	IO	**VCCSUS**	**Port 0 Twisted Pair A Negative.**
XTPB0P	71	IO	**VCCSUS**	**Port 0 Twisted Pair B Positive.**
XTPB0M	70	IO	**VCCSUS**	**Port 0 Twisted Pair B Negative.**
XTPA1P	80	IO	**VCCSUS**	**Port 1 Twisted Pair A Positive.**
XTPA1M	79	IO	**VCCSUS**	**Port 1 Twisted Pair A Negative.**
XTPB1P	78	IO	**VCCSUS**	**Port 1 Twisted Pair B Positive.**
XTPB1M	77	IO	**VCCSUS**	**Port 1 Twisted Pair B Negative.**
XTPA2P	87	IO	**VCCSUS**	**Port 2 Twisted Pair A Positive.**
XTPA2M	86	IO	**VCCSUS**	**Port 2 Twisted Pair A Negative.**
XTPB2P	85	IO	**VCCSUS**	**Port 2 Twisted Pair B Positive.**
XTPB2M	84	IO	**VCCSUS**	**Port 2 Twisted Pair B Negative.**
XTPBIAS0 **XTPBIAS1** **XTPBIAS2**	74 81 88	O	**VCCSUS**	**Port 2-0 Twisted Pair Bias Voltages.** Provides 1.85V (typical) nominal bias for proper operation of the twisted-pair cable drivers and receivers, and for signaling to the remote nodes that the cable connections are active. High-impedance during chip reset or power down. Can be disabled via remote packets or via software. Each of these pins must be decoupled with a 0.33-uF capacitor to ground.
XCPS	63	I	**VCCSUS**	**Cable Power Status.** This pin is normally connected to the cable power through an 11K Ohm / 1K Ohm voltage divider. An internal comparator is used to detect the presence of cable power.
XRES	66	A	**VCCSUS**	**External Resistor.** A 6.34K Ohm ±1% resistor to ground is required for internal current source operation.
XI	60	I	**VCCSUS**	**Crystal Input.** These pins must be connected to a 24.576 MHz parallel resonant fundamental mode crystal.
XO	61	O	**VCCSUS**	**Crystal Output.**

Serial Configuration Memory / I2C Interface				
Signal Name	**Pin #**	**I/O**	**Power**	**Signal Description**
EECS	29	O	**VCC**	**EEPROM Chip Select.** Chip select for external serial EEPROM when used to provide configuration data.
EEDO	30	O	**VCC**	**EEPROM Data Out.**
EEDI / SDA	31	I / IO	**VCC**	**EEPROM Data In / I2C Data.**
EECK / SCL	32	O / IO	**VCC**	**EEPROM Clock / I2C Clock.**

Miscellaneous				
Signal Name	**Pin #**	**I/O**	**Power**	**Signal Description**
PME#	37	O	**VCCSUS**	**Power Management Event.**
MODE[1-0]	42-43	I	**VCCSUS**	**Operation Select.** 00 Normal Mode (all PHY / Link signals are disabled) 01 PHY Test Mode 10 Link Test Mode 11 Watch Mode (all PHY / Link signals are outputs) Internal pull-down for default 00. These pins are normally not connected.
NC	38, 40, 44-48, 51-57, 67	-	-	**No Connect.** Reserved for future use. Some of these pins are used for power-on straps and some are used for test functions. Except for strap options, these pins should remain unconnected.

Power and Ground		
Signal Name	**Pin No.**	**Signal Description**
VCC	8, 20, 33, 35, 102, 113, 114, 125	**Power.** 3.3V ±0.3V.
GND	1, 9, 16, 26, 34, 36, 94, 103, 111, 115, 121	**Ground.**
VCCRAM	24	**Internal SRAM Power.** 3.3V ±0.3V.
GNDRAM	25	**Internal SRAM Ground.**
VCCSUS	39, 49	**Suspend Power.** 3.3V ±0.3V.
GNDSUS	41, 50	**Suspend Ground.**
VCCARX0	65	**Analog Power for 1394 Receive Channel 0.** 3.3V ±0.3V.
GNDARX0	64	**Analog Ground for 1394 Receive Channel 0.**
VCCATX0	62	**Analog Power for 1394 Transmit Channel 0.** 3.3V ±0.3V.
GNDATX0	59	**Analog Ground for 1394 Transmit Channel 0.**
VCCARX1	75	**Analog Power for 1394 Receive Channel 1.** 3.3V ±0.3V.
GNDARX1	68	**Analog Ground for 1394 Receive Channel 1.**
VCCATX1	76	**Analog Power for 1394 Transmit Channel 1.** 3.3V ±0.3V.
GNDATX1	69	**Analog Ground for 1394 Transmit Channel 1.**
VCCARX2	89	**Analog Power for 1394 Receive Channel 2.** 3.3V ±0.3V.
GNDARX2	82	**Analog Ground for 1394 Receive Channel 2.**
VCCATX2	90	**Analog Power for 1394 Transmit Channel 2.** 3.3V ±0.3V.
GNDATX2	83	**Analog Ground for 1394 Transmit Channel 2.**

Note 1: A combination of high frequency decoupling capacitors is suggested on all analog power / ground pairs.
Note 2. All grounds should be connected to the primary circuit board ground plane (i.e., to the lowest impedance point available).

REGISTERS

Register Overview

The following tables summarize the configuration and I/O registers of the VT6306. These tables also document the power-on default value ("Default") and access type ("Acc") for each register. Access type definitions used are RW (Read/Write), RO (Read/Only), "—" for reserved / used (essentially the same as RO), and RWC (or just WC) (Read / Write 1's to Clear individual bits). Registers indicated as RW may have some read/only bits that always read back a fixed value (usually 0 if unused); registers designated as RWC or WC may have some read-only or read write bits (see individual register descriptions for details).

Detailed register descriptions are provided in the following section of this document. All offset and default values are shown in hexadecimal unless otherwise indicated

Table 2. Registers

PCI Function 0 Registers – Link Controller

Configuration Space Header Registers

Offset	PCI Configuration Space Header	Default	Acc
1-0	Vendor ID	**1106**	RO
3-2	Device ID	**3044**	RO
5-4	Command	0000	**RW**
7-6	Status	**0280**	**WC**
8	Revision ID	nn	RO
9	Programming Interface	**10**	RO
A	Sub Class Code	00	RO
B	Base Class Code	**0C**	RO
C	-reserved- (cache line size)	00	—
D	Latency Timer	00	**RW**
E	Header Type	00	RO
F	-reserved- (Built In Self Test)	00	—
13-10	OHCI CSR MMIO Base Address	0000 0000	**RW**
17-14	VIO I/O Base Address	**0000 0001**	**RW**
1B-18	CIS Base Address (PCI Mode)	0000 0000	RO
	CIS Base Address (Cardbus Mode)	0000 0000	**RW**
1C-27	-reserved- (base address registers)	00	—
28-2B	CIS Pointer (PCI Mode)	0000 0000	RO
	CIS Pointer (Cardbus Mode)	**0000 0083**	RO
2F-2C	Subsystem ID Read	Nnnn nnnn	RO
30-33	-reserved- (expan. ROM base addr)	00	—
34	Capabilities Pointer	**50**	RO
35-3B	-reserved- (unassigned)	00	—
3C	Interrupt Line	00	**RW**
3D	Interrupt Pin	**01**	RO
3E	Minimum Grant	00	RO
3F	Maximum Latency	**20**	RO

Controller-Specific Configuration Registers

Offset	Configuration Registers	Default	Acc
43-40	PCI HCI Control	0000 0000	RO
44-4F	-reserved-	00	—

Power Management Registers

Offset	Power Management Register Block	Default	Acc
50	Power Management Capabilities ID	**01**	RO
51	Next Pointer	00	RO
53-52	Power Management Capabilities	**E002**	RO
55-54	Power Management CSR	0000	**WC**
56	Power Management CSR BSE	00	RO
57	Power Management Data	00	RO
58-FF	-reserved-	00	—

Memory-Space Registers – Link Controller

Offset	Heading	Default	Acc
0	Version (OHCI 1.0 Mode)	**0001 0000**	**RO**
	Version (OHCI 1.1 Mode)	**0001 0010**	**RO**
4	-reserved- (GUID ROM)	0000 0000	—
8	Asynchronous Transmit Retries	0000 0000	RW
C	CSR Data	0000 0000	RW
10	CSR Compare Data	0000 0000	RW
14	CSR Control	**8000 0000**	RW
18	Configuration ROM Header	0000 0000	RW
1C	1394 Bus ID	**3133 3934**	**RO**
20	1394 Bus Options	**F000 0002**	RW
24	Global Unique ID High	0000 0000	RW
28	Global Unique ID Low	0000 0000	RW
2C-33	-reserved-	00	—
34	Configuration ROM Map	0000 0000	RW
38	Posted Write Address Low	0000 0000	**RO**
3C	Posted Write Address High	0000 0000	**RO**
40	Vendor ID	0000 0000	**RO**
44-4F	-reserved-	00	—
50	HC Control Set	0000 0000	RW
54	HC Control Clear	0000 0000	RW
58-5F	-reserved-	00	—
60-63	-reserved-	00	—
64	Self-ID Buffer Pointer	0000 0000	RW
68	Self-ID Count	0000 0000	**RO**
6C-6F	-reserved-	00	—
70	Isoch Rcv Channel Mask High Set	0000 0000	RW
74	Isoch Rcv Channel Mask High Clr	0000 0000	RW
78	Isoch Rcv Channel Mask Low Set	0000 0000	RW
7C	Isoch Rcv Channel Mask Low Clr	0000 0000	RW
80	Interrupt Event Set	0000 0000	RW
84	Interrupt Event Clear	0000 0000	RW
88	Interrupt Mask Set	0000 0000	RW
8C	Interrupt Mask Clear	0000 0000	RW
90	Isoch Xmit Interrupt Event Set	0000 0000	RW
94	Isoch Xmit Interrupt Event Clear	0000 0000	RW
98	Isoch Xmit Interrupt Mask Set	0000 0000	RW
9C	Isoch Xmit Interrupt Mask Clear	0000 0000	RW
A0	Isoch Rcv Interrupt Event Set	0000 0000	RW
A4	Isoch Rcv Interrupt Event Clear	0000 0000	RW
A8	Isoch Rcv Interrupt Mask Set	0000 0000	RW
AC	Isoch Rcv Interrupt Mask Clear	0000 0000	RW

Offset	Heading	Default	Acc
B3-B0	Initial Bandwidth Available	**0000 1333**	RW
B7-B4	Initial Channels Available Hi	**FFFFFFFF**	RW
BB-B8	Initial Channels Available Lo	**FFFFFFFF**	RW
BC-DB	-reserved-	00	—
DC	Fairness Control	0000 0000	RW
E0	Link Control Set	0000 0000	RW
E4	Link Control Clear	0000 0000	RW
E8	Node ID	0000 0000	RW
EC	PHY Control	0000 0000	RW
F0	Isochronous Cycle Timer	0000 0000	RW
F4-FF	-reserved-	00	—
100	Async Request Filter High Set	0000 0000	RW
104	Async Request Filter High Clear	0000 0000	RW
108	Async Request Filter Low Set	0000 0000	RW
10C	Async Request Filter Low Clear	0000 0000	RW
110	Physical Request Filter High Set	0000 0000	RW
114	Physical Request Filter High Clear	0000 0000	RW
118	Physical Request Filter Low Set	0000 0000	RW
11C	Physical Request Filter Low Clear	0000 0000	RW
120-123	Physical Upper Bound	0000 0000	RW
124-17F	-reserved-	00	—
180	Async Request Xmit Context Set	0000 0000	RW
184	Async Request Xmit Context Clr	0000 0000	RW
18C	Async Request Xmit Command Ptr	0000 0000	RW
1A0	Async Response Xmit Context Set	0000 0000	RW
1A4	Async Response Xmit Context Clr	0000 0000	RW
1AC	Async Response Xmit Cmd Ptr	0000 0000	RW
1C0	Async Request Rcv Context Set	0000 0000	RW
1C4	Async Request Rcv Context Clr	0000 0000	RW
1CC	Async Request Rcv Command Ptr	0000 0000	RW
1E0	Async Response Rcv Context Set	0000 0000	RW
1E4	Async Response Rcv Context Clr	0000 0000	RW
1EC	Async Response Rcv Command Ptr	0000 0000	RW

Offset	Heading	Default	Acc
200	Isoch Xmit Context 0 Set	0000 0000	RW
204	Isoch Xmit Context 0 Clr	0000 0000	RW
20C	Isoch Xmit Context 0 Cmd Ptr	0000 0000	RW
210	Isoch Xmit Context 1 Set	0000 0000	RW
214	Isoch Xmit Context 1 Clr	0000 0000	RW
21C	Isoch Xmit Context 1 Cmd Ptr	0000 0000	RW
220	Isoch Xmit Context 2 Set	0000 0000	RW
224	Isoch Xmit Context 2 Clr	0000 0000	RW
22C	Isoch Xmit Context 2 Cmd Ptr	0000 0000	RW
230	Isoch Xmit Context 3 Set	0000 0000	RW
234	Isoch Xmit Context 3 Clr	0000 0000	RW
23C	Isoch Xmit Context 3 Cmd Ptr	0000 0000	RW
240	Isoch Xmit Context 4 Set	0000 0000	RW
244	Isoch Xmit Context 4 Clr	0000 0000	RW
24C	Isoch Xmit Context 4 Cmd Ptr	0000 0000	RW
250	Isoch Xmit Context 5 Set	0000 0000	RW
254	Isoch Xmit Context 5 Clr	0000 0000	RW
25C	Isoch Xmit Context 5 Cmd Ptr	0000 0000	RW
260	Isoch Xmit Context 6 Set	0000 0000	RW
264	Isoch Xmit Context 6 Clr	0000 0000	RW
26C	Isoch Xmit Context 6 Cmd Ptr	0000 0000	RW
270	Isoch Xmit Context 7 Set	0000 0000	RW
274	Isoch Xmit Context 7 Clr	0000 0000	RW
27C	Isoch Xmit Context 7 Cmd Ptr	0000 0000	RW
280-3FF	-reserved-	00	—

Offset	Heading	Default	Acc
400	Isoch Rcv Context 0 Set	0000 0000	RW
404	Isoch Rcv Context 0 Clr	0000 0000	RW
40C	Isoch Rcv Context 0 Command Ptr	0000 0000	RW
410	Isoch Rcv Context 0 Match	0000 0000	RW
420	Isoch Rcv Context 1 Set	0000 0000	RW
424	Isoch Rcv Context 1 Clr	0000 0000	RW
42C	Isoch Rcv Context 1 Command Ptr	0000 0000	RW
430	Isoch Rcv Context 1 Match	0000 0000	RW
440	Isoch Rcv Context 2 Set	0000 0000	RW
444	Isoch Rcv Context 2 Clr	0000 0000	RW
44C	Isoch Rcv Context 2 Command Ptr	0000 0000	RW
450	Isoch Rcv Context 2 Match	0000 0000	RW
460	Isoch Rcv Context 3 Set	0000 0000	RW
464	Isoch Rcv Context 3 Clr	0000 0000	RW
46C	Isoch Rcv Context 3 Command Ptr	0000 0000	RW
470	Isoch Rcv Context 3 Match	0000 0000	RW
480	Isoch Rcv Context 4 Set	0000 0000	RW
484	Isoch Rcv Context 4 Clr	0000 0000	RW
48C	Isoch Rcv Context 4 Command Ptr	0000 0000	RW
490	Isoch Rcv Context 4 Match	0000 0000	RW
4A0	Isoch Rcv Context 5 Set	0000 0000	RW
4A4	Isoch Rcv Context 5 Clr	0000 0000	RW
4AC	Isoch Rcv Context 5 Command Ptr	0000 0000	RW
4B0	Isoch Rcv Context 5 Match	0000 0000	RW
4C0	Isoch Rcv Context 6 Set	0000 0000	RW
4C4	Isoch Rcv Context 6 Clr	0000 0000	RW
4CC	Isoch Rcv Context 6 Command Ptr	0000 0000	RW
4D0	Isoch Rcv Context 6 Match	0000 0000	RW
4E0	Isoch Rcv Context 7 Set	0000 0000	RW
4E4	Isoch Rcv Context 7 Clr	0000 0000	RW
4EC	Isoch Rcv Context 7 Command Ptr	0000 0000	RW
4F0	Isoch Rcv Context 7 Match	0000 0000	RW
500-7FF	-reserved-	00	—

PHY Registers

Table 3. PHY Register Map

Offset	7	6	5	4	3	2	1	0
0000b	PS	R	Physical ID					
0001b	Gap Count						IBR	RHB
0010b	Total Ports				-	always 111b		
0011b	Delay				-	Max Speed		
0100b	Power Class			Jitter			Cont	LC
0101b	Multi	Accel	PE	Tout	PF	Loop	ISBR	WT
0110b	-reserved-							
0111b	Port Select				-	Page Select		
1000b	Register 0 (Page Select)							
1001b	Register 1 (Page Select)							
1010b	Register 2 (Page Select)							
1011b	Register 3 (Page Select)							
1100b	Register 4 (Page Select)							
1101b	Register 5 (Page Select)							
1110b	Register 6 (Page Select)							
1111b	Register 7 (Page Select)							

Physical ID = Address of This Node
R = Root Node
PS = Cable Power Status
RHB = Root Hold-Off
IBR = Initiate Bus Reset
Gap Count = For Gap Time Optimization
Total Ports = 3
Max Speed = Supports 98.304, 196.608, & 393.216 Mbit/s
Delay = Worst Case Repeater Delay
LC = Link Control
Cont = Contender
Jitter = Repeater Delay Variation
WT = Watchdog Timer Enable
ISBR = Initiate Short (Arbitrated) Bus Reset
Loop = Loop Detect
PF = Cable Power Fail Detect
Tout = Arbitration State Machine Timeout
PE = Port Event Detect
Accel = Arbitration Acceleration Enable
Multi = Multispeed Packet Concatenation Enable

Register Descriptions

Link Controller Configuration Registers (PCI Function 0)

The 1394 host controller interface follows the Open HCI (OHCI) interface specification. There are two sets of software accessible registers: configuration registers and memory registers. The configuration registers are located in the function 0 PCI configuration space. The memory registers are located in system memory space at offsets from the address stored in the Base Address Register.

Configuration Space Header

Offset 1-0 - Vendor ID ..... RO

0-7 Vendor ID ..... (1106h = VIA Technologies)

Offset 3-2 - Device ID ..... RO

0-7 Device ID ..... (3044h = VT6306 1394a Controller)

Offset 5-4 - Command ..... RW

15-10 Reserved ..... always reads 0
9 Fast Back-to-Back Enable ..... fixed at 0 (disabled)
8 SERR# Enable ..... fixed at 0 (disabled)
7 Wait Cycle Control ..... fixed at 0 (disabled)
6 Parity Error Response ..... fixed at 0 (disabled)
5 VGA Palette Snoop ..... fixed at 0 (disabled)
4 Postable Memory Write Enable fixed at 0 (disabled)
3 Special Cycle Enable ..... fixed at 0 (disabled)
2 Bus Master Enable
0 Disable ..... default
1 Enable
1 Memory Space Enable
0 Disable ..... default
1 Enable Access to 1394 Memory Registers
0 I/O Space Enable ..... fixed at 0 (disabled)

Offset 7-6 - Status ..... RWC

15 Detected Parity Error ..... always reads 0
14 Signaled System Error ..... always reads 0
13 Received Master Abort
0 No Master Abort Generated ..... default
1 Master Abort Generated by 1394 Controller. Set by the 1394 interface logic if it generates a master abort while acting as a master. This bit may be cleared by software by writing a one to this bit position.
12 Received Target Abort
0 No Target Abort Received ..... default
1 Target Abort Received by 1394 Controller. Set by the 1394 interface logic if it receives a target abort while acting as a master. This bit may be cleared by software by writing a one to this bit position.
11 Signaled Target Abort ..... always reads 0
10-9 DEVSEL# Timing
00 Fast
01 Medium ..... fixed
10 Slow
11 Reserved
8 Data Parity Error Detected ..... always reads 0
7 Fast Back-to-Back Capable ..... always reads 1
6 User Definable Features ..... always reads 0
5 66 MHz Capable ..... always reads 0
4-0 Reserved ..... always reads 0

Offset 8 - Revision ID (nnh) **..... RO**

7-0 Silicon Revision Code (0 indicates first silicon)

Offset 9 - Programming Interface (10h=OHCI) **..... RO**

Offset A - Sub Class Code (00h=1394 Serial Bus) **..... RO**

Offset B - Base Class Code (0Ch=Serial Bus Controller) **... RO**

Offset D - Latency Timer (00h) **..... RW**

7-4 Latency Timer Count
PCI burst cycles generated by the VT6306 can last indefinitely as long as PCI GNT# remains active. If GNT# is negated after the burst is initiated, the VT6306 limits the duration of the burst to the number of PCI Bus clocks specified in this field.
3-0 Reserved ..... always reads 0

Offset E - Header Type (00h) **..... RO**

Offset 13-10 – OHCI CSR MMIO Base (0000 0000h) ....RW

31-11	**Base Address (2048-Byte Space)**	default = 0
10-4	**Reserved**	always reads 0
3	**Prefetechable**	always reads 0
	Reads 0 to indicate that the register space is not prefetchable.	
2-1	**Type**	always reads 0
	Reads 0 to indicate that the register space may be located anywhere in the 32-bit memory address space.	
0	**Resource Type**	always reads 0
	Reads 0 to indicate a request for memory space.	

Offset 17-14 – VIO I/O Base Address (0000 0001h).....RW

31-7	**Base Address (128-Byte Space)**	default = 0
6-4	**Reserved**	always reads 0
3	**Prefetechable**	always reads 0
	Reads 0 to indicate that the register space is not prefetchable.	
2-1	**Type**	always reads 0
	Reads 0 to indicate that the register space may be located anywhere in the 16-bit I/O address space.	
0	**Resource Type**	always reads 1
	Reads 1 to indicate a request for I/O space.	

Offset 1B-18 – CIS Base (0000 0000h) ..... RO (PCI Mode)
..... RW (Cardbus Mode)

31-8	**Base Address (256-Byte Space)**	default = 0
7-4	**Reserved**	always reads 0
3	**Prefetechable**	always reads 0
	Reads 0 to indicate that the register space is not prefetchable.	
2-1	**Type**	always reads 0
	Reads 0 to indicate that the register space may be located anywhere in the 32-bit memory address space.	
0	**Resource Type**	always reads 0
	Reads 0 to indicate a request for memory space.	

Offset 2B-28 – CIS Pointer ..... RO

31-0	**CIS Pointer (PCI Mode)**	reads 0000 0000h
	CIS Pointer (Cardbus Mode)	reads 0000 0083h

Offset 34 – Capabilities Pointer (50h)..... RO

Offset 3C - Interrupt Line (00h).....**RO**

Offset 3D - Interrupt Pin (01h=Drives INTA#) .....**RO**

Offset 3E - Minimum Grant (00h) .....**RO**

Offset 3F - Maximum Latency (20h) .....**RO**

Controller-Specific Configuration Registers

Offset 43-40 –PCI HCI Control..... RO

insert bit definitions here

Power Management Registers

Offset 50 – Capabilities ID (01h)..... RO

7-0 Capabilities ID..... always reads 01h
Always reads 01h to indicate that this list item is the Power Management Register Block

Offset 51 – Next Item Pointer (00h) ..... RO

7-0 Next Item Pointer ..... always reads 0
Always reads 0 to indicate that there are no additional items in the Capabilities List.

Offset 53-52 – Power Management Capabilities (E002) . RO

15 PME# Can Be Asserted From D3cold
0 Not capable
1 Capable**..... always reads 1**

14 PME# Can Be Asserted From D3hot
0 Not capable
1 Capable**..... always reads 1**

13 PME# Can Be Asserted From D2
0 Not capable
1 Capable**..... always reads 1**

12 PME# Can Be Asserted From D1
0 Not capable ..... always reads 0
1 Capable

11 PME# Can Be Asserted From D0
0 Not capable ..... always reads 0
1 Capable

10 D2 Power Management State Supported
0 Not supported ..... always reads 0
1 Supported

9 D1 Power Management State Supported
0 Not supported ..... always reads 0
1 Supported

8-6 3.3V Auxiliary Current Required
000 None (device is self powered) .... always reads 0
001 55 mA
010 100 mA
011 160 mA
100 220 mA
101 270 mA
110 320 mA
111 375 mA

5 Device-Specific Initialization Required
0 Not required ..... always reads 0
1 Required

4 Reserved ..... always reads 0

3 PME Clock
0 No PCI clock is required ..... always reads 0
1 PCI clock is required for PME# generation

2-0 Specification Version ..... always reads 010b
Reads 010b to indicate that this function complies with Revision 1.1 of the PCI Power Management Interface Specification

Offset 55-54 – Pwr Mgmt Control / Status (PMCSR) .RWC

15 PME Status ..... RWC
This bit is set when the function would normally assert the PME# signal independent of the state of the PME_Enable bit. Writing a "1" will clear this bit and cause the function to stop asserting PME# (if enabled).

14-13 Data Scale ..... RO
Scaling factor to use when interpreting the value of the Data register ..... always reads 0

12-9 Data Select ..... RW
Used to select which data is to be reported through the Data register and Data_Scale field..... default = 0

8 PME Enable ..... RW
0 PME# assertion disabled.....default
1 PME# assertion enabled

7-2 Reserved ..... always reads 0

1-0 Power State ..... RW
These bits indicate the current power state and are used to change to a new power state. If an attempt is made to write a code corresponding to an unsupported state, the write of these bits is ignored and no state change occurs.
00 D0
01 D1
10 D2
11 D3hot

Offset 56 – Pwr Mgmt CSR Bridge Support Extensions.RO

7 Bus Power / Clock Control Enable.... always reads 0

6 B2/B3 Support for D3hot ..... always reads 0

5-0 Reserved ..... always reads 0

Offset 57 – Power Management Data.....RO

7-0 Data
Used to report state-dependent data requested by the Data Select field of the PMCSR register (scaled per the Data Scale field).

Link Controller Memory-Space Registers

These registers occupy a 2048-byte space in system memory (offsets 0-7FFh). This address space begins at the address contained in the 1394 Configuration Space "Base Address Register" (Function 0 Configuration Space Offset 10h).

All registers must be accessed as 32-bit words on 32-bit boundaries. Writes to reserved addresses have undefined results and reads from reserved addresses return indeterminate data. Unless specified otherwise, all register fields default to 0 and are unchanged after a 1394 bus reset.

Some registers are designated as Set and Clear registers. These registers are in pairs, where a read of either address will return the current contents of the register. Data written to the Set register address is assumed to be a bit mask where one bits determine which bits should be set. Data written to the Clear register address is assumed to be a bit mask where one bits determine which bits should be cleared.

Memory Offset 0 – Version..... RO

31-0 Version – OHCI 1.0 Mode.....reads 0001 0000
Version – OHCI 1.1 Mode.....reads 0001 0010

Memory Offset 8 – Asynchronous Transmit Retries.....RW

31-29 Second Limit.....RO
Count in Seconds (modulo 8). These bits and the Cycle Limit bits below define a time limit for retry attempts when the outbound dual-phase retry protocol is in use.

28-16 Cycle Limit .....RO
Count in Cycles (modulo 8000). These bits and the Second Limit bits above define a time limit for retry attempts when the outbound dual-phase retry protocol is in use.

15-12 Reserved ..... always reads 0

11-8 Max Physical Response Retries ..... default = 0
Specifies how many times to attempt to retry the transmit operation for the physical response packet when a "busy" or "ack_type_error" acknowledge is received from the target node. This value is used only for responses to physical requests.

7-4 Max AT Response Retries ..... default = 0
Specifies to the Asynchronous Transmit Response subsystem how many times to attempt to retry the transmit operation for the response packet when a "busy" or "ack_type_error" acknowledge is received from the target node. This value is used only for responses sent by software via the Asynchronous Transmit Response DMA context.

3-0 Max AT Request Retries ..... default = 0
Specifies to the Asynchronous Transmit DMA Request subsystem how many times to attempt to retry the transmit operation for a packet when a "busy" or "ack_type_error" acknowledge is received from the target node. This value is used only for responses sent by software via the Asynchronous Transmit Request DMA context.

Autonomous CSR Resources

The VT6306 implements the 1394 "Compare-and-Swap" bus management registers, the Configuration ROM Header, and the "Bus Info Block". It also allows access to the first 1K bytes of the configuration ROM.

Atomic compare-and-swap transactions, when accessed from the 1394 bus, are autonomous without software intervention. To access these bus management resource registers via the PCI bus, the software first loads the CSR Data register with a new data value to be loaded, then it loads the CSR Compare register with the expected value. Finally, it writes the CSR Control register with the selected value of the resource. This initiates a compare-and-swap operation. When complete, the CSR Control register "done" bit will be set and the CSR Data register will contain the value of the selected resource prior to the host-initiated compare-and-swap operation.

Bus Management CSR Registers

1394 requires certain 1394 bus management resource registers to be accessible only via 32-bit read and 32-bit lock (compare-and-swap) transactions. These special bus management resource registers are implemented on-chip:

CSR Address	CSR Select	Register Name	Hardware or Bus Reset
FFFF F000 021C	00	Bus Manager ID	0000 003F
FFFF F000 0220	01	Bandwidth Available	0000 1333
FFFF F000 0224	10	Channels Available Hi	FFFF FFFF
FFFF F000 0228	18	Channels Available Lo	FFFF FFFF

CSR Address FFFF F000 021C – Bus Manager ID .....RW

31-6 Reserved ..... always reads 0
5-0 Bus Manager ID ..... default = 3Fh

CSR Address FFFF F000 0220 – Bandwidth Available .RW

31-13 Reserved ..... always reads 0
12-0 Bandwidth Available ..... default = 1333h

CSR Address FFFF F000 0224 – Channels Avail Hi .....RW

7-0 Reserved ..... always reads 0

CSR Address FFFF F000 0228 – Channels Avail Lo.....RW

7-0 Reserved ..... always reads 0

Memory Offset C – CSR Data.....RW

31-0 CSR Data ..... default = undefined
Data to be stored if comparison is successful.

Memory Offset 10 – CSR Compare Data.....RW

31-0 CSR Compare Data ..... default = undefined
Data to be compared with existing value of CSR resource.

Memory Offset 14 – CSR Control .....RW

31 CSR Done ..... default = 1
Set when a compare-swap operation is completed. Reset whenever this register is written.
30-2 Reserved ..... always reads 0
1-0 CSR Resource Select..... default = undefined
00 Bus Manager ID
01 Bandwidth Available
10 Channels Available Hi
11 Channels Available Lo

Memory Offset 18 – Configuration ROM Header.....RW

31-24 Bus Info Block Length..... default = 0
Length of the Bus Information Block in doublewords
23-16 CRC Length..... default = 0
Length of the block protected by the CRC (a value of 4 indicates that the CRC only protects the configuration ROM header).
15-0 ROM CRC Value
Default value loaded from GUID ROM if present (default is undefined if GUID ROM is not present). Must be set prior to setting the "HC Control" register "Link Enable" bit.

Memory Offset 1C – 1394 Bus ID ..... RO

This register maps to the 1st 32-bit word of the bus info block.

31-0 Bus ID.....always reads 31333934h (ASCII "1394")

Memory Offset 20 – 1394 Bus Options.....RW

This register maps to the 2nd quadword of the bus info block.

31 Isochronous Resource Manager Capable
- 0 Not capable
- 1 Capable..... default

30 Cycle Master Capable
- 0 Not capable
- 1 Capable..... default

29 Isochronous Capable
- 0 Not capable
- 1 Capable..... default

28 Bus Manager Capable
- 0 Not capable
- 1 Capable..... default

27 Power Management Capable
- 0 Not capable ..... default
- 1 Capable

26-24 Reserved ..... always reads 0

23-16 Cycle Clock Acc
1394 Bus Management Field. This field must be written with valid data prior to setting the "HC Control" register "link enable" bit.

15-12 Received Block Write Request Packet Max Length
1394 Bus Management Field. This field must be written with valid data prior to setting the "HC Control" register "link enable" bit. Received block write request packets with a length greater than the value contained in this field may generate an "ack_type_error".

11-8 Reserved ..... always reads 0

7-6 Configuration ROM Changed Since Last Bus Reset
- 0 Configuration ROM not changed..... default
- 1 Configuration ROM changed

5-3 Reserved ..... always reads 0

2-0 Max Link Speed..... default = 010

Memory Offset 24 – Global Unique ID High.....RW

This register maps to the 3rd 32-bit word of the bus info block. Contents are cleared by hardware reset but are not affected by software reset. Read/Write if Rx44[0] is cleared, Read/Only if Rx44[0] is set.

31-8 Node Vendor ID ..... default = 0
1394 Bus Management Field. Must be set prior to setting the "HC Control" register "link enable" bit.

7-0 Chip ID High..... default = 0
1394 Bus Management Field. Must be set prior to setting the "HC Control" register "link enable" bit.

Memory Offset 28 – Global Unique ID Low .....RW

This register maps to the 4th 32-bit word of the bus info block. Contents are cleared by hardware reset but are not affected by software reset. Read/Write if Rx44[0] is cleared, Read/Only if Rx44[0] is set.

31-0 Chip ID Low..... default = 0
1394 Bus Management Field. Must be set prior to setting the "HC Control" register "link enable" bit.

Memory Offset 34 – Configuration ROM Map.....RW

This register contains the start address within the memory space that maps to the start address of the 1394 configuration ROM. Only 32-bit word reads to the first 1K bytes of the configuration ROM will map to memory space.(all other transactions to this space will be rejected with an "ack_type_error"). The system address of the configuration ROM must start on a 1K-byte boundary. The first five 32-bit words of the configuration ROM space are mapped to the configuration ROM header and Bus Info Block, so the first five registers addressed by this register are not used. This register must be set to a valid address prior to setting the "HC Control" register "link enable" bit.

31-10 Configuration ROM Address..... default = 0
Read requests to 1394 offsets FFFF F000 0400 through FFFF F000 03FC have the low-order 10 bits of the offset added to this register to determine the host memory address of the returned data value.

9-0 Reserved ..... always reads 0

Memory Offset 38 – Posted Write Address Low ..... RO

31-0 Offset Low ..... default = undefined
If the "Posted Write Error" bit is set in the Interrupt Events register, this and the "Posted Write Address High" register contain the 48 bits of the 1394 destination offset of the write request that resulted in the PCI error.

Memory Offset 3C – Posted Write Address High ..... RO

31-16 Source ID ..... default = undefined
The Bus Number and Node Number of the node which has issued the failed write request.

15-0 Offset High ..... default = undefined
If the "Posted Write Error" bit is set in the Interrupt Events register, this and the "Posted Write Address Low" register contain the 48 bits of the 1394 destination offset of the write request that resulted in the PCI error.

Memory Offset 40 – Vendor ID..... RO

31-0 Vendor ID ..... always reads TBD

HC Control Registers

The following two registers are a "set / clear" register pair. Writing to the "Set" register address sets selected bits in the control register where the written bit value is 1. Writing to the "Clear" register address clears selected bits in the control register where the written bit value is 1. Reading from either address returns the contents of the control register.

Memory Offset 50 (Set), 54 (Clear) – HC Control .....RW

31-20 Reserved ..... always reads 0

19 Link Power Status
- 0 Prohibit Link to PHY Communications.....def
- 1 Permit Link to PHY Communications (link can use LREQs to perform PHY reads and writes).

This bit has no effect on "Link On" status for the node (see Link Enable status below). Both software and hardware resets clear this bit.

18 Posted Write Enable ..... default = undefined
- 0 All writes return "ack_pending"
- 1 Enable 2-deep posted write queue

Software should only change this bit when "Link Enable" is 0.

17 Link Enable
- 0 Disable packets from being transmitted, received, or processed .....default
- 1 Enable packets to be transmitted, received, and processed

Both software and hardware resets clear this bit. Software should not set this bit until the Configuration ROM mapping register is valid.

16 Soft Reset
When set, all on-chip 1394 states are reset, all FIFOs are flushed, and all registers are set to their hardware reset (default) values unless otherwise specified. PCI configuration registers are not affected. Hardware clears this bit automatically when the reset is complete (it reads 1 while the reset is in progress).

15-0 Reserved ..... always reads 0

Self-ID Control Registers

Memory Offset 64 – Self ID Buffer Pointer .....RW

31-11 Self-ID Buffer Pointer..... default = undefined
Contains the base address of a 2K-byte buffer in host memory where received Self-ID packets are stored.

10-0 Reserved ..... always reads 0

Memory Offset 68 – Self ID Count ..... RO

31 Self-ID Error ..... default = undefined
0 Self-ID packet received with no errors (this bit is automatically cleared after error-free reception of a Self-ID packet)
1 Error detected during most recent Self-ID packet reception (the contents of the Self-ID Buffer are undefined in this case)

30-24 Reserved ..... always reads 0

23-16 Self-ID Generation..... default = undefined
The value in this field is incremented automatically each time the Self-ID reception process begins. The value rolls over after reaching 255.

15-13 Reserved ..... always reads 0

12-2 Self-ID Size ..... default = undefined
Contains the length in 32-bit words of Self-ID data that has been received. This field is cleared by 1394 bus reset.

1-0 Reserved ..... always reads 0

Channel Mask Registers

Offset 70 (Set), 74 (Clear) – Iso Rcv Channel Mask Hi ..RW

31-0 Iso Channel Mask N+32 ..... default = 0000
Bits 31-0 correspond to channel numbers 63-32.
Writing 1 bits to offset 70 enables corresponding channels for receiving isochronous data. Writing 1 bits to offset 74 disables corresponding channels from receiving isochronous data.

Offset 78 (Set), 7C (Clear) – Iso Rcv Channel Mask Lo .RW

31-0 Iso Channel Mask N+32 ..... default = 0000
Bits 31-0 correspond to channel numbers 31-0.
Writing 1 bits to offset 78 enables corresponding channels for receiving isochronous data. Writing 1 bits to offset 7C disables corresponding channels from receiving isochronous data.

Interrupt Registers

Memory Offset 80 (Set), 84 (Clear) – Interrupt Events ..RW

31-27 Reserved ..... always reads 0

26 PHY Register Data Received
PHY register data byte received (data byte not sent when register 0 received)

25 Cycle Too Long
More than 115 usec (but not more than 120 usec) elapsed between the start of sending a cycle start packet and the end of a subaction gap.

24 Unrecoverable Error
Error encountered that has forced the chip to stop operations of any or all subunits (e.g., when a DMA context sets its "ContextControl.Dead" bit)

23 Cycle Inconsistent
Cycle start received with a cycle count different from the value in the "Cycle Timer" register

22 Cycle Lost
Expected cycle start not received (cycle start not received immediately after the first subaction gap after the "Cycle Sync" event or arbitration reset gap detected after a "Cycle Sync" event without an intervening cycle start).

21 Cycle 64 Seconds Interrupt
Bit 7 of the "Cycle Seconds Counter" has changed.

20 Cycle Synch Interrupt
New isochronous cycle started (least significant bit of the cycle count toggled).

19 PHY Requested Interrupt
The PHY has requested an interrupt using a status transfer.

18 Reserved ..... always reads 0

17 Bus Reset Entered
The Phy has entered bus reset mode.

16 Self-ID Complete
Self-ID packet stream received.

15-10 Reserved ..... always reads 0

9 Lock Response Error
Lock response sent to a serial bus register in response to a lock request but no "ack_complete" received.

8 Posted Write Error
A host bus error occurred while the chip was trying to write a 1394 write request (which had already been given an "ack_complete") into system memory.

7 Isochronous ReceiveDMA Complete
One or more Isochronous receive contexts have generated an interrupt (one or more bits have been set in the "Isochronous Receive Interrupt Event" register masked by the "Isochronous Receive Interrupt Mask" register).

6 Isochronous Transmit DMA Complete
One or more Isochronous transmit contexts have generated an interrupt (one or more bits have been set in the "Isochronous Transmit Interrupt Event" register masked by the "Isochronous Transmit Interrupt Mask" register).

5 Response Packet Sent
A packet was sent to an asynchronous receive response context buffer.

4 Receive Packet Sent
A packet was sent to an asynchronous receive request context buffer.

3 Async Receive Response DMA Complete
Conditionally set upon completion of an ARDMA Response context command descriptor.

2 Async Receive Request DMA Complete
Conditionally set upon completion of an ARDMA Request context command descriptor.

1 Async Response Transmit DMA Complete
Conditionally set upon completion of an ATDMA Response command.

0 Async Request Transmit DMA Complete
Conditionally set upon completion of an ATDMA Request command.

Memory Offset 88 (Set), 8C (Clear) – Interrupt Mask ...RW

The bits in this register (except for the Master Interrupt Enable bit in bit-31) correspond to the bits in the Interrupt Event register above. Zeros in these bits prevent the corresponding interrupt condition from generating an interrupt. Bits are set in the mask register by writing one bits to the "Set" address and cleared by writing one bits to the "Clear" address. The current value of the mask bits may be read from either address.

31 Master Interrupt Enable
- 0 Disable All Interrupt Events.....default
- 1 Generate interrupts per mask bits 0-26

30-27 Reserved ..... always reads 0

26-0 Interrupt Mask..... default = undefined (see Interrupt Event register)

Offset 90 (Set), 94 (Clear) – Iso Xmit Interrupt Events ..RW

31-4 **Reserved** ..... always reads 0

3-0 **Isochronous Transmit Context** . default = undefined
An interrupt is generated by an isochronous transmit context if an "Output Last DMA" command completes and its "i" bits are set to "interrupt always". Software clears the bits in this register by writing one bits to the "Clear" address. Bits in this register will only get set to one if the corresponding bits in the mask register are set to one.

Offset 98 (Set), 9C (Clear) – Iso Xmit Interrupt Mask ...RW

31-4 **Reserved** ..... always reads 0

3-0 **Iso Transmit Context Mask**..... default = undefined
Setting bits in this register enables interrupts to be generated by the corresponding isochronous transmit context

Offset A0 (Set), A4 (Clear) – Iso Rcv Interrupt Events ..RW

31-4 **Reserved** ..... always reads 0

3-0 **Isochronous Receive Context** .... default = undefined
An interrupt is generated by an isochronous receive context if an "Input Last DMA" command completes and its "i" bits are set to "interrupt always". Software clears the bits in this register by writing one bits to the "Clear" address. Bits in this register will only get set to one if the corresponding bits in the mask register are set to one.

Offset A8 (Set), AC (Clear) – Iso Rcv Interrupt Mask....RW

31-4 **Reserved** ..... always reads 0

3-0 **Iso Receive Context Mask**..... default = undefined
Setting bits in this register enables interrupts to be generated by the corresponding isochronous receive context

Offset B3-B0 – Initial Bandwidth Available.....RW

31-13 **Reserved** ..... always reads 0

12-0 **Initial Bandwidth Available**..... default = 1333h

Offset B7-B4 – Initial Channels Available High .....RW

31-0 **Initial Channels Available**.....default = FFFF FFFFh

Offset BB-B8 – Initial Channels Available Low.....RW

31-0 **Initial Channels Available**.....default = FFFF FFFFh

Link Control Registers

Memory Offset DC – Fairness Control ..... RO

31-8 Reserved ..... always reads 0

7-0 Requests Per Fairness Interval ..... default = 0
The number of request packets allowed to be transmitted per fairness interval

Memory Offset E0 (Set), E4 (Clear) – Link Control .....RW

This register contains the control flags that enable and configure the link core protocol portions of the chip. It contains controls for the receiver and cycle timer.

31-22 Reserved ..... always reads 0

21 Cycle Master ..... default = undefined
- 0 Received cycle start packets will be accepted to maintain synchronization with the node that is sending them.
- 1 If the PHY has sent notification that it is root, a cycle start packet will be generated every time the cycle timer rolls over, based on the setting of the "Cycle Source" bit.

This bit is cleared automatically if the "Cycle Too Long" interrupt event occurs and cannot be set until the "Cycle Too Long" interrupt event bit is cleared.

20 Cycle Timer Enable ..... default = undefined
- 0 Cycle timer offset will not count
- 1 Cycle Timer offset will count cycles of the 24.576 MHz clock and roll over at the appropriate time based on the settings of the above bits

19-11 Reserved ..... always reads 0

10 Receive PHY Packet ..... default = 0
- 0 All PHY packets received outside of the self-ID phase are ignored
- 1 The receiver will accept incoming PHY packets into the AR request context if the AR request context is enabled. This bit does not control receipt of self-ID packets.

9 Receive Self-ID ..... default = 0
- 0 All self-ID packets are ignored
- 1 The receiver will accept incoming self-identification packets. Before setting this bit, software must ensure that the self-ID buffer pointer register contains a valid address.

8-0 Reserved ..... always reads 0

Memory Offset E8 – Node ID.....RW

This register contains the CSR address for the node on which this chip resides. The 16-bit combination of the Bus Number and Node Number fields is referred to as the "Node ID". The Node Number field is updated when register 0 is sent from the PHY. This can happen either because software requested a read from the PHY through the PHY Control register or because the PHY is sending the register (most likely due to a bus reset).

31 ID Valid
- 0 No valid node number (cleared by bus reset)
- 1 Valid node number received from PHY

30 Root
This bit is set to 0 or 1 during bus reset
- 0 Attached PHY is not root .....def
- 1 Attached PHY is root

29-28 Reserved ..... always reads 0

27 Cable Power Status
- 0 PHY reports cable power status is not OK....def
- 1 PHY reports cable power status is OK.

26-16 Reserved ..... always reads 0

15-6 Bus Number .....
Used to identify the specific 1394 bus to which this node belongs when multiple 1394-compatible buses are connected via a bridge (set to 3FFh by bus reset)

5-0 Node Number ..... default = 0
The physical node number established by the PHY during self-identification and automatically set to the value received from the PHY after the self-identification phase. If the PHY sets this field to 63 (all ones), all link-level transmits are disabled.

PHY Control Registers

Memory Offset EC – PHY Control.....RW

This register is used to read or write a PHY register. To read or write, the address of the register is written into the Register Address field. For reads the "Read Register" bit is set (when the request has been sent to the PHY, the "Read Register" bit is cleared automatically by the chip). When transmitting the request, the first clock for LREQ for the register read/write portion will be bit-11 of this register followed by bit-10, etc, finishing with bit-8 for register reads and bit-0 for register writes. When the PHY returns the register through a status transfer, the "Read Done" bit is set. The address of the register received is placed in the "Read Address" field and the contents in the "Read Data" field. The first bits of data received on the status transfer for the register are placed in bits 27 (D[0]) and 26 (D[1]) of this register. For writes, the value to write is written to the "Write Data" field and the "Write Register" bit is set. The "Write Register" bit is cleared automatically by the chip when the write request has been sent to the PHY.

31 Read Done
Indicates that a read request has been completed and valid information is contained in the Read Data and Read Address fields. Cleared when the "Read Register" bit is set. It is set by the chip when a register transfer is received from the PHY.

30-28 Reserved ..... always reads 0

27-24 Read Address
The address of the register most recently received from the PHY.

23-16 Read Data
The contents of the register most recently received from the PHY

15 Read Register
Used to initiate a read request from a PHY register (must not be set at the same time as the "Write Register" bit). Cleared by the chip when the request has been sent.

14 Write Register
Used to initiate a write request to a PHY register (must not be set at the same time as the "Read Register" bit). Cleared by the chip when the request has been sent.

13-12 Reserved ..... always reads 0

11-8 Register Address
The address of the PHY register to be read or written

7-0 Write Data
The data to be written to the PHY (ignored for reads)

Cycle Timer Registers

Memory Offset F0 – Isochronous Cycle Timer .....RW

This register shows the current cycle number and offset. When the chip is cycle master, this register is transmitted with the cycle start message. When it is not cycle master, this register is loaded with the data field in an incoming cycle start. In the event that the cycle start message is not received, the fields continue incrementing on their own (when the "Cycle Timer Enable" field is set in the "Link Control" register) to maintain a local time reference.

31-25 Cycle Seconds ..... default = 0
This field counts seconds ("Cycle Count" rollovers) modulo 128.

24-12 Cycle Count ..... default = 0
This field counts cycles ("Cycle Offset" rollovers) modulo 8000.

11-0 Cycle Offset ..... default = 0
This field counts 24.576 MHz clocks modulo 3072 (125 usec).

Filter Registers

Offset 100 (Set), 104 (Clear) – Async Req Filter High ....RW

31 **Async Request Resources All Buses**

0 Asynchronous requests received from non-local bus nodes will be accepted only if the bit which is set corresponds to the node number (see the remaining bits of this register and the "Async Request Filter Low" register). ..... default

1 All asynchronous requests received from non-local bus nodes will be accepted.

Bus reset does not affect the value of this bit.

30-0 **Async Request Resource "N"**..... default = 0

If set to one for local bus node number N+32, asynchronous requests received from that node number will be accepted. The bit number corresponds to the node number + 32. Bus reset sets all bits of this field to 0.

Offset 108 (Set), 10C (Clear) – Async Req Filter Low ....RW

31-0 **Async Request Resource "N"**..... default = 0

If set to one for local bus node number N, asynchronous requests received from that node number will be accepted. The bit number corresponds to the node number. Bus reset sets all bits of this field to 0.

Offset 110 (Set), 114 (Clear) – Physical Req Filter High RW

31 **Physical Request Resources All Buses**

0 Asynchronous physical requests received from non-local bus nodes will be accepted only if the bit which is set corresponds to the node number (see the remaining bits of this register and the "Physical Request Filter Low" register). .....default

1 All asynchronous physical requests received from non-local bus nodes will be accepted.

Bus reset does not affect the value of this bit.

30-0 **Physical Request Resource "N"**..... default = 0

If set to one for local bus node number N+32, asynchronous physical requests received from that node number will be accepted. The bit number corresponds to the node number + 32. Bus reset sets all bits of this field to 0.

Offset 118 (Set), 11C (Clear) – Physical Req Filter Low RW

31-0 **Physical Request Resource "N"**..... default = 0

If set to one for local bus node number N, asynchronous physical requests received from that node number will be accepted. The bit number corresponds to the node number. Bus reset sets all bits of this field to 0.

Offset 120 – Physical Upper Bound.....RW

31-0 **Physical Upper Bound**..... default = 0

Asynchronous Transmit & Receive Context Registers

Offset 180 (Set), 184 (Clr) – Async Req Xmit Context....RW

Offset 1A0 (Set), 1A4 (Clr) – Async Rsp Xmit Context ..RW

Offset 1C0 (Set), 1C4 (Clr) – Async Req Rcv Context ....RW

Offset 1E0 (Set), 1E4 (Clr) – Async Rsp Rcv Context.....RW

These registers are the Context Control registers for Asynchronous Transmit Requests and Responses and Asynchronous Receive Requests and Responses, respectively. They contain bits for control of options, operational state, and status for a DMA context. The bit layout for both registers is given below:

31-16 Reserved ..... always reads 0

15 Run

This bit is set and cleared by software to enable descriptor processing for a context. The chip will clear this bit automatically on a hardware or software reset. Before software sets this bit, the active bit must be clear and the Command Pointer register for the context must contain a valid descriptor block address and a Z value that is appropriate for the descriptor block address.

Software may stop the chip from further processing of a context by clearing this bit. When cleared, the chip will stop processing of the context in a manner that will not impact the operation of any other context or DMA controller. This may require a significant amount of time. If software clears a run bit for an isochronous context while the chip is processing a packet for the context, it will continue to receive or transmit the packet and update the descriptor status. It will then stop at the conclusion of that packet. If the run bit is cleared for a non-isochronous context, the chip will stop processing at a convenient point and put the descriptors in a consistent state (e.g., status updated if a packet was sent and acknowledged).

Clearing the bit may have other side effects that are DMA controller dependent. This is described in the sections that cover each of the DMA controllers.

14-13 Reserved ..... always reads 0

12 Wake ..... default = 0

When software adds to a list of descriptors for a context, the chip may have already read the descriptor that was at the end of the list before it was updated. This bit provides a semaphore to indicate that the list may have changed.

If the chip had fetched a descriptor and the indicated branch address had a Z value of zero, it will reread the pointer value when the wake bit is set. If, on the reread, the Z value is still zero, then the end of the list has been reached and the chip will clear the active bit. If, however, the Z value is now non-zero, the chip will continue processing. If the wake bit is set while the chip is active and has a Z value of non-zero, it takes no special action.

The chip will clear this bit before it reads or rereads a descriptor. The wake bit should not be set while the run bit is zero.

11 Dead ..... default = 0

This bit is set by the chip to indicate a fatal error in processing a descriptor. When set, the active bit is cleared. This bit is cleared when software clears the run bit or on a hardware or software reset.

10 Active ..... default = 0

This bit is set by the chip when software sets the run bit or sets the wake bit while the run bit is set. The chip will clear this bit:

1) when a branch is indicated by a descriptor but the Z value of the branch address is 0
2) when software clears the run bit and the chip has reached a safe stopping point
3) while the dead bit is set
4) after a hardware or software reset
5) for asynchronous transmit contexts (request and response), when a bus reset occurs

When this bit is 0 and the run bit is 0, the chip will set the Interrupt Event bit for the context.

9-8 Reserved ..... always reads 0

7-5 Speed (Async Receive Contexts Only)

This field indicates the speed at which the packet was received or transmitted:

000 100 Mbits/sec
001 200 Mbits/sec
010 400 Mbits/sec
011 -reserved-
1xx -reserved-

4-0 Ack / Err Code..... default = 0

Following an "Output Last" command, the received "Ack Code" or "Event Error Code" is indicated in this field. Possible values are: "Ack Complete", "Ack Pending", Ack Busy X", "Ack Data Error", "Ack Type Error", "Event Tcode Error", "Event Missing Ack", "Event Underrun", "Event Descriptor Read", "Event Data Read", "Event Timeout", "Event Flushed", and "Event Unknown" (see "Table 4. Packet Event Codes" on the following page for descriptions and values for these codes).

Offset 18C – Async Req Xmit Context Command Ptr....RW

Offset 1AC – Async Rsp Xmit Context Command Ptr...RW

Offset 1CC – Async Req Rcv Context Command Ptr.....RW

Offset 1EC – Async Rsp Rcv Context Command Ptr .....RW

Table 4. Packet Event Codes

Code	Name	DMA	Meaning
00/10	**Event Tcode Error**	AT, AR, IT, IR, IT	A bad Tcode is associated with this packet. The packet was flushed.
01/11	**Event Short Packet**		The received data length was less than the packet's data length (IR packet-per-buffer mode only).
02/12	**Event Long Packet**	IR	The received data length was greater than the packet's data length (IR packet-per-buffer mode only).
03/13	**Event Missing Ack**	AT	A subaction gap was detected before an ack arrived
04/14	**Event Underrun**	AT, IT	An underrun occurred on the corresponding FIFO and the packet was truncated.
05/15	**Event Overrun**	IR	A receive FIFO overflowed during the reception of an isochronous packet.
06/16	**Event Descriptor Read**	AT, AR, IT, IR	An unrecoverable error occurred while the Host Controller was reading a descriptor block.
07/17	**Event Data Read**	AT, IT	An error occurred while the Host Controller was attempting to read from host memory in the data stage of descriptor processing.
08/18	**Event Data Write**	AR, IR, IT	An error occurred while the Host Controller was attempting to write to host memory in the data stage of descriptor processing.
09/19	**Event Bus Reset**	AR	Identifies a PHY packet in the receive buffer as being the synthesized bus reset packet
0A/1A	**Event Timeout**	AT	Indicates that the asynchronous transmit response packet expired and was not transmitted
0B	**Event Tcode Error**	AT	A bad Tcode is associated with this packet. The packet was flushed.
0C-0D/1B-1D	**Reserved**		
0E/1E	**Event Unknown**	AT, AR, IT, IR	An error condition has occurred that cannot be represented by any other defined event codes
0F/1F	**Event Flushed**	AT	Sent by the link side of the output FIFO when asynchronous packets are being flushed due to a bus reset
11	**Ack Complete**	AT, AR, IT, IR	The destination node has successfully accepted the packet. If the packet was a request subaction, the destination node has successfully completed the transaction and no response subaction shall follow. The ack / err code for transmitted PHY, isochronous and broadcast packets, none of which yield an ack code, will be set by hardware to "Ack Complete" unless an "Event Underrun" or "Event Data Read" occurs.
12	**Ack Pending**	AT, AR	The destination node has successfully accepted the packet. If the packet was a request subaction, a response subaction will follow at a later time. This code is not returned for a response subaction.
13	**Reserved**		
14	**Ack Busy X**	AT	The packet could not be accepted after max "ATretries" attempts and the last Ack received was "Ack Busy X."
15	**Ack Busy A**	AT	The packet could not be accepted after max "ATretries" attempts and the last Ack received was "Ack Busy A." OHCI does not support the dual phase retry protocol for transmitted packets, so this Ack should not be received.
16	**Ack Busy B**	AT	The packet could not be accepted after max "ATretries" attempts and the last Ack received was "Ack Busy B" (see note for "Ack Busy A").
17-1C	**Reserved**		
1D	**Ack Data Error**	AT, IR	The destination node could not accept the block packet because the data field failed the CRC check or because the length of the data block payload did not match the length contained in the "Data Length" field. This code is not returned for any packet that does not have a data block payload.
1E	**Ack Type Error**	AT, AR	Returned when a received block write request or received block read request is greater than "max_rec"
1F	**Reserved**		

Isochronous Transmit Context Registers

Offset 200 (Set), 204 (Clr) – Isoch Xmit Context 0 .....RW
Offset 210 (Set), 214 (Clr) – Isoch Xmit Context 1 .....RW
Offset 220 (Set), 224 (Clr) – Isoch Xmit Context 2 .....RW
Offset 230 (Set), 234 (Clr) – Isoch Xmit Context 3 .....RW
Offset 240 (Set), 244 (Clr) – Isoch Xmit Context 4 .....RW
Offset 250 (Set), 254 (Clr) – Isoch Xmit Context 5 .....RW
Offset 260 (Set), 264 (Clr) – Isoch Xmit Context 6 .....RW
Offset 270 (Set), 274 (Clr) – Isoch Xmit Context 7 .....RW

These registers are the Context Control registers for isochronous Transmit Contexts 0-7. Each context consists of two registers: a Command Pointer and a Context Control register. The Command Pointer is used by software to tell the controller where the context program begins. The Context Control register controls the context's behavior and indicates current status. The bit layout for the Context Control registers is given below:

31-30 Reserved ..... always reads 0

29 Cycle Match Enable
In general, when set to one the context will begin running only when the 13-bit "Cycle Match" field matches the 13-bit "Cycle Count" in the Cycle Start packet. The effects of this bit however are impacted by the values of other bits in this register. Once the context becomes active, this bit is cleared automatically by the chip.

28-16 Cycle Match
Contains a 13-bit value corresponding to the 13-bit "Cycle Count" field. If the "Cycle Match Enable" bit is set, this ITDMA context will become enabled for transmits when the bus cycle time "Cycle Count" value equals the value in this field.

15 Run
This bit is set and cleared by software to enable descriptor processing for a context. The chip will clear this bit automatically on a hardware or software reset. Before software sets this bit, the active bit must be clear and the Command Pointer register for the context must contain a valid descriptor block address and a Z value that is appropriate for the descriptor block address.
Software may stop the chip from further processing of a context by clearing this bit. When cleared, the chip will stop processing of the context in a manner that will not impact the operation of any other context or DMA controller. This may require a significant amount of time. If software clears a run bit while the chip is processing a packet for the context, it will continue to receive or transmit the packet and update the descriptor status. It will then stop at the conclusion of that packet.
Clearing the bit may have other side effects that are DMA controller dependent. This is described in the sections that cover each of the DMA controllers.

14-13 Reserved ..... always reads 0

12 Wake ..... default = 0
When software adds to a list of descriptors for a context, the chip may have already read the descriptor that was at the end of the list before it was updated. This bit provides a semaphore to indicate that the list may have changed.
If the chip had fetched a descriptor and the indicated branch address had a Z value of zero, it will reread the pointer value when the wake bit is set. If, on the reread, the Z value is still zero, then the end of the list has been reached and the chip will clear the active bit. If, however, the Z value is now non-zero, the chip will continue processing. If the wake bit is set while the chip is active and has a Z value of non-zero, it takes no special action.
The chip will clear this bit before it reads or rereads a descriptor. The wake bit should not be set while the run bit is zero.

11 Dead ..... default = 0
This bit is set by the chip to indicate a fatal error in processing a descriptor. When set, the active bit is cleared. This bit is cleared when software clears the run bit or on a hardware or software reset.

10 Active ..... default = 0
This bit is set by the chip when software sets the run bit or sets the wake bit while the run bit is set. The chip will clear this bit:
1) when a branch is indicated by a descriptor but the Z value of the branch address is 0
2) when software clears the run bit and the chip has reached a safe stopping point
3) while the dead bit is set
4) after a hardware or software reset

When this bit is cleared and the run bit is clear, the chip will set the Interrupt Event bit for the context.

9-5 Reserved ..... always reads 0

4-0 Ack / Err Code..... default = 0
Following an "Output Last" command, the received "Ack Code" or "Event Error Code" is indicated in this field. Possible values are: "Ack Complete", "Ack Pending", Ack Busy X", "Ack Data Error", "Ack Type Error", "Event Tcode Error", "Event Missing Ack", "Event Underrun", "Event Descriptor Read", "Event Data Read", "Event Timeout", "Event Flushed", and "Event Unknown" (see "Table 4. Packet Event Codes" on the previous page for descriptions and values for these codes).

Offset 20C – Isoch Xmit Context 0 Command Ptr.....RW
Offset 21C – Isoch Xmit Context 1 Command Ptr.....RW
Offset 22C – Isoch Xmit Context 2 Command Ptr.....RW
Offset 23C – Isoch Xmit Context 3 Command Ptr.....RW
Offset 24C – Isoch Xmit Context 4 Command Ptr.....RW
Offset 25C – Isoch Xmit Context 5 Command Ptr.....RW
Offset 26C – Isoch Xmit Context 6 Command Ptr.....RW
Offset 27C – Isoch Xmit Context 7 Command Ptr.....RW

Isochronous Receive Context Registers

Offset 400 (Set), 404 (Clr) – Isoch Rcv Context 0 .....RW
Offset 420 (Set), 424 (Clr) – Isoch Rcv Context 1 .....RW
Offset 440 (Set), 444 (Clr) – Isoch Rcv Context 2 .....RW
Offset 460 (Set), 464 (Clr) – Isoch Rcv Context 3 .....RW
Offset 480 (Set), 484 (Clr) – Isoch Rcv Context 4 .....RW
Offset 4A0 (Set), 4A4 (Clr) – Isoch Rcv Context 5 .....RW
Offset 4C0 (Set), 4C4 (Clr) – Isoch Rcv Context 6 .....RW
Offset 4E0 (Set), 4E4 (Clr) – Isoch Rcv Context 7.....RW

These registers are the Context Control registers for isochronous Receive Contexts 0-3. Each context consists of three registers: a Command Pointer, a Context Control register, and a Context Match register. The Command Pointer is used by software to tell the controller where the context program begins. The Context Control register controls the context's behavior and indicates current status. The Context Match Register is used to start transmitting from a context program on a specified cycle number. The bit layout for the Context Control registers is given below:

31 Buffer Fill
- 0 Each received packet is placed in a single buffer
- 1 Received packets are placed back-to-back to completely fill each receive buffer

If the "Multi-Channel Mode" bit is set, this bit must also be set. This bit must not be changed while the "Active" bit is set.

30 Isoch Header
- 0 The packet header is stripped from received isochronous packets
- 1 Received packets will include the isochronous packet header (the header will be stored first in memory followed by the payload). The end of the packet will be marked with a "Transfer Status" (bits 15-0 of this register) in the first word followed by a 16-bit time stamp indicating the time of the most recently received "Cycle Start" packet.

29 Cycle Match Enable
- 0 Context will begin running immediately
- 1 Context will begin running only when the 13-bit "Cycle Match" field in the "Context Match" register matches the 13-bit "Cycle Count" in the Cycle Start packet.

The effects of this bit are impacted by the values of other bits in this register. Once the context becomes active, this bit is cleared automatically by the chip.

28 Multi-Channel Mode
- 0 The context will receive packets for a single channel.
- 1 The context will receive packets for all isochronous channels enabled in the "IR Channel Mask High" and "IR Channel Mask Low" registers (the channel number in the "Context Match" register is ignored). If more than one Context Control register has the Multi-Channel Mode bit set, unspecified behavior will result.

27-16 Reserved ..... always reads 0

15 Run

This bit is set and cleared by software to enable descriptor processing for a context. The chip will clear this bit automatically on a hardware or software reset. Before software sets this bit, the active bit must be clear and the Command Pointer register for the context must contain a valid descriptor block address and a Z value that is appropriate for the descriptor block address.

Software may stop the chip from further processing of a context by clearing this bit. When cleared, the chip will stop processing of the context in a manner that will not impact the operation of any other context or DMA controller. This may require a significant amount of time. If software clears the run bit while the chip is processing a packet for the context, it will continue to receive or transmit the packet and update descriptor status. It will then stop at the conclusion of that packet.

Clearing the bit may have other side effects that are DMA controller dependent. This is described in the sections that cover each of the DMA controllers.

14-13 Reserved ..... always reads 0

12 Wake ..... default = 0

When software adds to a list of descriptors for a context, the chip may have already read the descriptor that was at the end of the list before it was updated. This bit provides a semaphore to indicate that the list may have changed.

If the chip had fetched a descriptor and the indicated branch address had a Z value of zero, it will reread the pointer value when the wake bit is set. If, on the reread, the Z value is still zero, then the end of the list has been reached and the chip will clear the active bit. If, however, the Z value is now non-zero, the chip will continue processing. If the wake bit is set while the chip is active and has a Z value of non-zero, it takes no special action.

The chip will clear this bit before it reads or rereads a descriptor. The wake bit should not be set while the run bit is zero.

11 Dead ..... default = 0

This bit is set by the chip to indicate a fatal error in processing a descriptor. When set, the active bit is cleared. This bit is cleared when software clears the run bit or on a hardware or software reset.

10 Active ..... default = 0

This bit is set by the chip when software sets the run bit or sets the wake bit while the run bit is set. The chip will clear this bit:

1) when a branch is indicated by a descriptor but the Z value of the branch address is 0

2) when software clears the run bit and the chip has reached a safe stopping point
3) while the dead bit is set
4) after a hardware or software reset

When this bit is cleared and the run bit is clear, the chip will set the Interrupt Event bit for the context.

9-7 Reserved ..... always reads 0

6-5 Speed

This field indicates the speed at which the packet was received or transmitted:

00 100 Mbits/sec
01 200 Mbits/sec
10 400 Mbits/sec
11 -reserved-

4-0 Ack / Err Code..... default = 0

Following an "Input" command, this field contains the error code.

For "Buffer Fill" mode, possible values are: "Ack Complete", "Ack Data Error", "Event Overrun", "Event Descriptor Read", "Event Data Write", and "Event Unknown" (see "Table 4. Packet Event Codes" for descriptions and values for these codes).

For "Packet-Per-Buffer" mode, possible values are: "Ack Complete", "Ack Data Error", "Event Short Packet", "Event Long Packet", "Event Overrun", "Event Descriptor Read", "Event Data Write", and "Event Unknown" (see "Table 4. Packet Event Codes" for descriptions and values for these codes).

Offset 40C – Isoch Receive Context 0 Command Ptr.....RW
Offset 42C – Isoch Receive Context 1 Command Ptr.....RW
Offset 44C – Isoch Receive Context 2 Command Ptr.....RW
Offset 46C – Isoch Receive Context 3 Command Ptr.....RW
Offset 48C – Isoch Receive Context 4 Command Ptr.....RW
Offset 4AC – Isoch Receive Context 5 Command Ptr.....RW
Offset 4CC – Isoch Receive Context 6 Command Ptr.....RW
Offset 4EC – Isoch Receive Context 7 Command Ptr.....RW

Offset 410 – Isoch Receive Context 0 Match .....RW
Offset 430 – Isoch Receive Context 1 Match .....RW
Offset 450 – Isoch Receive Context 2 Match .....RW
Offset 470 – Isoch Receive Context 3 Match .....RW
Offset 490 – Isoch Receive Context 4 Match .....RW
Offset 4B0 – Isoch Receive Context 5 Match .....RW
Offset 4D0 – Isoch Receive Context 6 Match .....RW
Offset 4F0 – Isoch Receive Context 7 Match.....RW

PHY Registers

The PHY registers are accessed through the PHY Control register at Memory Offset 0ECh.

PHY Register Overview

Offset	7	6	5	4	3	2	1	0
0000b	PS	R	Physical ID					
0001b	Gap Count						IBR	RHB
0010b	Total Ports				-	Extended		
0011b	Delay				-	Max Speed		
0100b	Power Class			Jitter			Cont	LC
0101b	Multi	Accel	PE	Tout	PF	Loop	ISBR	WT
0110b	-reserved-							
0111b	Port Select				-	Page Select		
1000b	Register 0 (Page Select)							
1001b	Register 1 (Page Select)							
1010b	Register 2 (Page Select)							
1011b	Register 3 (Page Select)							
1100b	Register 4 (Page Select)							
1101b	Register 5 (Page Select)							
1110b	Register 6 (Page Select)							
1111b	Register 7 (Page Select)							

PHY Register Bit Field Descriptions

Field	Bits	Type	Def	Description
Physical_ID	6	R	-	The address of this node determined during self-identification. A value of 63 indicates a malconfigured bus where the link must not transmit any packets.
R	1	R	-	A setting of one indicates that this node is the root.
PS	1	R	-	Cable Power status.
RHB	1	RW	0	Root hold-off bit. A setting of one instructs the chip to attempt to become the root during the next tree identification process.
IBR	1	RW	0	Initiate bus reset. A setting of one instructs the chip to initiate a bus reset immediately (without arbitration). This causes assertion of the reset state for 166 us and is self-clearing.
Gap Count	6	RW	3Fh	Used to configure the arbitration timer setting in order to optimize gap times according to the topology of the bus.
Extended	3	R	111	Constant value of seven
Total Ports	5	R	011	Three ports
Max Speed	3	R	010	Supports 98.304, 196.608, and 393.216 Mbit/s
Delay	4	R	0	Worse case repeater delay = 144 ns
Link Control	1	RW	1	Link Control. Cleared or set by software to control the value of the L bit transmitted in the node's Self-ID packet 0.

PHY Register Bit Field Descriptions (continued)

Contender	1	RW	Pin CMC	Contender. Cleared or set by software to control the value of the C bit transmitted in the first self-ID packet.
Power Class	3	RW	Pins PC [0:2]	Power class. This information will be copied to bits 21-23 of the first self-ID packet.
Jitter	3	R	0	Repeater delay; 20ns variation max
WT	1	RW	0	Watchdog enable. Controls whether loop, power fail, and timeout interrupts are indicated to the link when the link is in sleep. Also determines whether interrupts are indicated to the internal link when resume operations start from any port.
ISBR	1	RW	0	Initiate short (arbitrated) bus reset. A write of one to this bit instructs the chip to arbitrate and issue a short bus reset. This bit is self-clearing.
Loop	1	RW	0	Loop detect. A write of one to this bit clears it to zero.
Power Fail	1	RW	1	Cable power failure detect. Set to one when the PS bit changes from one to zero. A write of one to this bit clears it to zero.
Timeout	1	RW	0	Arbitration state machine timeout. A write of one to this bit clears it to zero.
Port Event	1	RW	0	Port event detect. The chip sets this bit to one if any of connected, Bias, Disabled or Fault change for a port whose Int_enable bit is one. The chip also sets this bit to one if resume operations commence for any port and Resume_int is one. A write of one to this bit clears it to zero.
Enable Acceleration	1	RW	0	Enable arbitration acceleration. When set to one, the chip must use the enhancements specification in IEEE P1394a 4.0.
Enable Multi	1	RW	0	Enable multi-speed packet concatenation.
Page Select	3	RW	000	Selects which of eight possible PHY register pages are accessible through the window at PHY register address 1000b through 1111b, inclusive.
Port Select	4	RW	0000	If the page selected by Page_select presents per port information, this field selects which port's registers are accessible through the window at PHY register addresses 1000b through 1111b, inclusive.

PHY Register Page 0 - Port Status

The Port Status page is used to access configuration and status information for each of the PHY's port. The port is selected by writing zero to Page_select and the desired port number to Port_select in the PHY register at address 0111.

Offset	7	6	5	4	3	2	1	0
1000b	Disa	Bias	Conn	Child	Bstat		Astat	
1001b	-reserved-			Fault	IntEn	Negotiated Speed		
1010b	-reserved-							
1011b	-reserved-							
1100b	-reserved-							
1101b	-reserved-							
1110b	-reserved-							
1111b	-reserved-							

Table 5. PHY Register Page 0 Bit Field Descriptions

Field	Bits	Type	Def	Description
Astat	2	R	-	TPA line state for the port 00 = invalid 01 =1 10 =0 11 =z
Bstat	2	R	-	Same encoding as Astat
Child	1	R	-	1 indicates the port is a child, 0 a parent. The meaning of this bit is undefined from the time a bus reset is detected until the chip transitions to state T1:Child Handshake during the tree identify process (see 4.4.2.2 in IEEE 1394-1995)
Conncted	1	R	0	One indicates the port is connected, zero indicates it is disconnected. The value reported by this bit is filtered by hysteresis logic to reduce multiple status changes caused by contact scrape when a connector is inserted or removed.
Bias	1	R	-	One indicates that bias voltage is detected (possible connection). The value reported by this bit is filtered by hysteresis logic to reduce multiple status changes caused by contact scrape when a connector is inserted or removed.
Disabled	1	RW	0	When set to one, the port is disabled. The value of this bit subsequent to a power reset is implementation-dependent, but should be a strappable option.
Negotiated Speed	3	R	-	Indicates the maximum speed negotiated between this port and its immediately connected port. 000 – 98.304 Mbit/s 001 - and 196.608 Mbit/s 010 - and 393.216 Mbit/s
Interrupt Enable	1	RW	0	Enable port event interrupts. When set to one, the chip sets Port_event to one if any of Connected, Bias, Disabled or Fault (for this port) change state.
Fault	1	rw	0	Set to one if an error is detected during a suspend or resume operation. A write of one to this bit clears it to zero.

PHY Register Page 1 - Vendor Identification

The Vendor Identification page is used to identify the VT6306's vendor and compliance level. The page is selected by writing one to Page_select in the PHY register at address 0111.

Offset	7	6	5	4	3	2	1	0
1000b	Compliance Level							
1001b	-reserved-							
1010b	Vendor ID							
1011b								
1100b								
1101b	Product ID							
1110b								
1111b								

Table 6. PHY Register Page 1 Bit Field Descriptions

Field	Bits	Type	Default	Description
Compliance Level	8	R	1	"1" indicates IEEE P1394a
Vendor ID	24	R	00 40 63	The company ID or Organizationally Unique Identifier (OUI) of the manufacturer of the PHY. The most significant byte of Vendor_ID appears at PHY register location 1010 and the least significant at 1100.
Product ID	24	R	30 60 00	The meaning of this number is determined by the company or organization that has been granted Vendor_ID. The most significant byte of Product_ID appears at PHY register location 1101 and the least significant at 1111.

PHY Register Page 7 - Vendor-Dependent

The vendor-dependent page provides registers set aside for use by the PHY's vendor. The page is selected by writing seven to Page_select in the PHY register at address 0111.

Offset	7	6	5	4	3	2	1	0
1000b	Reserved for Test (Do Not Access)							
1001b	Reserved for Test (Do Not Access)							
1010b	Reserved for Test (Do Not Access)							
1011b	Reserved for Test (Do Not Access)							
1100b	Reserved for Test (Do Not Access)							
1101b	Reserved for Test (Do Not Access)							
1110b	Reserved for Test (Do Not Access)							
1111b	Reserved for Test (Do Not Access)							

FUNCTIONAL DESCRIPTIONS

PHY General Description

Cable Interface

The VT6306 provides three-port physical layer function in a cable IEEE 1394-1995 network. Each cable port incorporates two differential line transceivers. The transceivers include circuitry to monitor the line conditions as needed for determining connection status, for initialization and arbitration, and for half duplex packet reception and transmission.

Data bits to be transmitted through the cable ports are latched internally in the VT6306 in synchronization with the 49.152-MHz system clock. During transmission the encoded data is transmitted differentially on the TPB cable pair(s) and the encoded strobe information is transmitted differentially on the TPA cable pair(s).

During packet reception, the TPA and TPB transmitters of the receiving cable port are disabled, and the receivers for that port are enabled. The encoded data information is received on the TPA cable pair, and the encoded Strobe information is received on the TPB cable pair. The received data-strobe information is resynchronized to local PLL clocks and the retiming buffer can tolerate clock variation up to +/-100ppm with 4K bytes at 393.216 Mbps, 2K bytes at 196.608 Mbps, and 1K bytes at 98.304 Mbps.

Both the TPA and TPB cable interfaces (see figure below) incorporate differential comparators to monitor the line states during initialization and arbitration. The outputs of these comparators are used by internal logic to determine the arbitration status. The TPA channel generates the cable common-mode voltage. The value of this common mode voltage is used during arbitration to detect the speed of the next packet transmission by the peer PHY. In addition, VT6306 adds a current source and a connection detect circuit at TPA channel. When TPBIAS is driven low, the connection detect circuit is used to detect the presence or absence of a peer PHY at the other end of a cable connection. The TPB channel monitors the incoming cable common-mode voltage for the presence of the remotely supplied twisted-pair bias voltage. The presence or absence of this common-mode voltage is used as an indication of cable suspend, resume and active status.

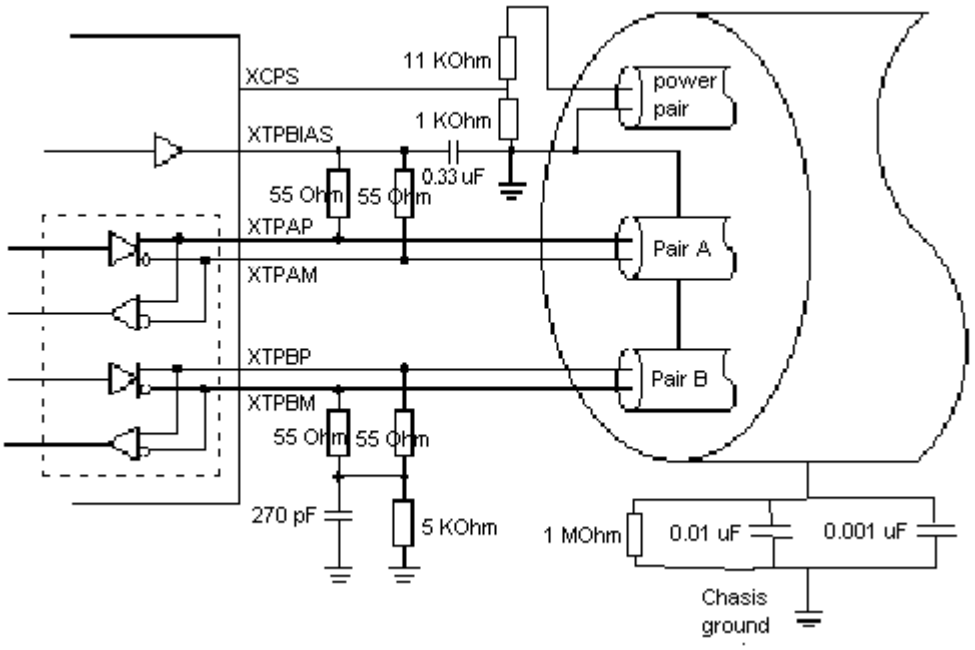


Figure 5. Cable Interface

PHY Circuit Description

Pinless PLL and Clock Generation

The VT6306 PHY requires an external 24.576 MHz crystal as a reference. An external clock can also be provided instead of a crystal. An internal oscillator drives an internal phase-locked loop (PLL), which generates the required 393.216 MHz reference clock. This reference signal is internally divided to provide the clock signals used to control transmission of the outbound encoded Strobe and Data information. A 49.152 MHz clock signal is used for resynchronization of the received data. The PLL requires no external filter components, referred to as "pinless PLL", saving board implementation cost.

Power Down and Auto Power Save

The power down function stops operation of the PLL and disables all circuits except the connection detection circuits and bias detection circuits at the XTPBIAS pins. Port transmitter and receiver circuitry are also disabled automatically when the port is disabled, suspended, or disconnected.

Pinless PHY RESET

The RESET# can be left unconnected for saving board implementation cost. The internal power good circuit generates the required PHY reset if the RESET# pin is unconnected. The required reset time is at least 0.5 ms. The reset time can be extended if an external RC network is implemented. The port transmitter and receiver circuitry is disabled during power down, during reset (when the RESET# input pin is asserted low), when no active cable is connected to the port, or when controlled by the internal arbitration logic.

Data Transmission

Data bits to be transmitted through the cable ports are latched internally in synchronization with the 49.152 MHz system clock.

These bits are combined serially, encoded, and transmitted at 98.304/196.608/392.216 Mbps (referred to as S100, S200, and

S400 speed, respectively) as the outbound data-strobe information stream. During transmission, the encoded data information is transmitted differentially on the TPB cable pair(s), and the encoded strobe information is transmitted differentially on the TPA cable pair(s).

Data Reception

During packet reception the TPA and TPB transmitters of the receiving cable port are disabled, and the receivers for that port are enabled. The encoded data information is received on the TPA cable pair, and the encoded strobe information is received on the TPB cable pair. The received data-strobe information is decoded to recover the receive clock signal and the serial data bits. The serial data bits are collected into two-bit, four-bit or eight-bit parallel streams (depending upon the indicated receive speed), resynchronized to the local 49.152 MHz system clock and sent to the LLC. The retiming buffer can tolerate clock variation up to +/- 100 ppm (compared to peer PHY) with 4K bytes at 393.216 Mbps, 2K bytes at 196.608 Mbps, and 1K bets at 98.304 Mbps. The received data is also transmitted (repeated) to the other active (connected) cable ports.

TPBIAS

Both the TPA and TPB cable interfaces incorporate differential comparators to monitor the line states during initialization and arbitration. The outputs of these comparators are used by the internal logic to determine the arbitration status. The TPA channel monitors the incoming cable common-mode voltage to determine the speed of the next packet transmission (speed signaling) during arbitration. In addition, the TPB channel monitors the incoming cable common-mode voltage on the TPB pair for the presence of the peer PHY bias voltage. The VT6306 provides three independent 1.84V nominal bias voltages at the XTPBIAS pins. The bias voltage, when seen through a cable by a remote receiver, indicates the presence of an active connection. The bias voltage source must be stabilized by an external filter capacitor of 0.33 µF.

Bias-Detector / Connect-Detector / Bias-Discharger

The VT6306 supports suspend / resume / disable functions as defined in the IEEE P1394a V4.0 specification. The suspend mechanism allows pairs of directly connected ports to be placed into a low power state while maintaining a port-to-port connection between 1394 bus segments. While in a low power state, a port is unable to transmit or receive data transaction packets. However, a port in a low power state is capable of detecting connection status changes and detecting incoming TPBIAS. When all three ports

are suspended, all circuits except the connect-detect circuits and bias-detect circuits are powered down, resulting in significant power savings. The connect-detect circuit monitors the value of incoming TPA pair common-mode voltage when local TPBIAS is inactive. A very small current source charges the XTPBIAS pin to almost VCC when the cable is not connected. Before the connect-detect circuit is enabled, the VT6306 enables a bias-discharger to improve the later-on connect-detect quality. Both the cable bias-detect monitor and connect-detect monitor are used in connect / suspend / resume / disable signaling. For additional details of suspend / resume / disable operation, refer to the IEEE P1394a V4.0 specification.

Twisted-Pair TPA and TPB

The line drivers operate in a high-impedance current mode, and are designed to work with external 110 Ohm line-termination resistor networks in order to match the 110 Ohm cable impedance. One network is provided at each end of all twisted-pair cable. Each network is composed of a pair of series-connected 55 Ohm resistors. The midpoint of the pair of resistors that is directly connected to the twisted-pair TPA pins is connected to its corresponding XTPBIAS pin. The midpoint of the pair of resistors that is directly connected to the twisted-pair B pins is coupled to ground through a parallel RC network with recommended values of 5K Ohm and 270 pF. The values of the external line termination resistors are designed to meet the standard specifications when connected in parallel with the internal receiver circuits.

Bandgap Current Generation

An external resistor connected between the XRES pin and ground sets the driver output current, as well as internal operating currents. This current setting resistor has a value of 6.34K Ohm +/- 1%.

Power Off

When the power supply of the VT6306 is removed while the twisted-pair cables are connected, the VT6306 transmitter / receiver circuitry and the XTPBIAS pin presents a high impedance state. As the consequence, peer PHYs see the VT6306 as unconnected.

Unimplemented Ports

When the VT6306 is used with one or more of the ports not brought out to a connector, some of the twisted-pair pins of the unused ports can be left unconnected to reduce implementation cost. For each unused port, the XTPBIAS pins can be tied to analog power (VCCA) for more reliable operation. The XTPAP, XTPAM, XTPBP and XTPBM pins of an unused port can be left unconnected.

CMC, PC0, PC1, PC2 Strapping

CMC and PC[0:2] are used as strapping pins to set the default value for four configuration status bits in the self-ID packet and should be hard-wired high or low as a function of the equipment design. The PC0, PC1, and PC2 pins are used to indicate the default power-class status for the node (the need for power from the cable or the ability to supply power to the cable). See Table 7 below for power class encoding. The CMC pin is used as an input to indicate that the node is a contender for bus manager.

Table 7. Power Class Pin Strapping

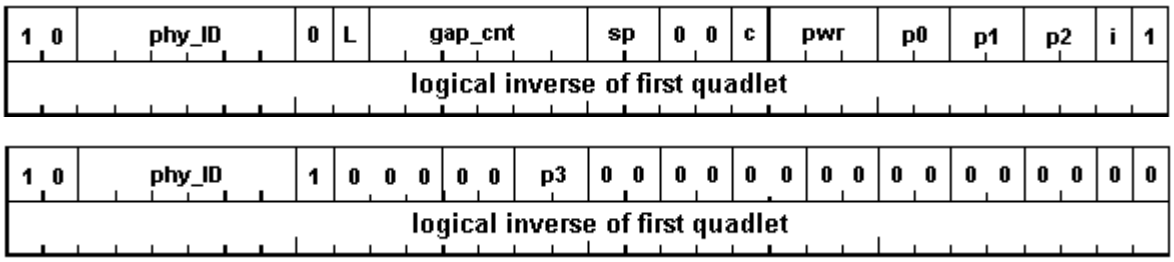
PC[0:2]	Power Consumption and Source Characteristics
000b	Node does not need power and does not repeat power
001b	Node is self-powered and provides a minimum of 15W to the bus
010b	Node is self-powered and provides a minimum of 30W to the bus
011b	Node is self-powered and provides a minimum of 45W to the bus
100b	Node may be powered from the bus and is using up to 1W
101b	Node is powered from the bus and is using up to 1W. An additional 2W is needed to enable the link and higher layers.
110b	Node is powered from the bus and is using up to 1W. An additional 5W is needed to enable the link and higher layers.
111b	Node is powered from the bus and is using up to 1W. An additional 9W is needed to enable the link and higher layers.

Support to PHY Packet

The VT6306 PHY will forward to the link (if the internal link layer is active) every PHY packet received on the bus. It will interpret every PHY packet which it receives from the local link device for transmission on the bus (in addition to responding to every PHY packet received from the bus). The VT6306 PHY will act on it in exactly the same way as if the packet was received from the bus.

Self-ID Packet

The Self-ID packet has the format shown in Figure 6 and the fields in the Self-ID packet are derived as shown in Table 8.



Note: Bit 0 (the lsb) is on the left in the above diagram

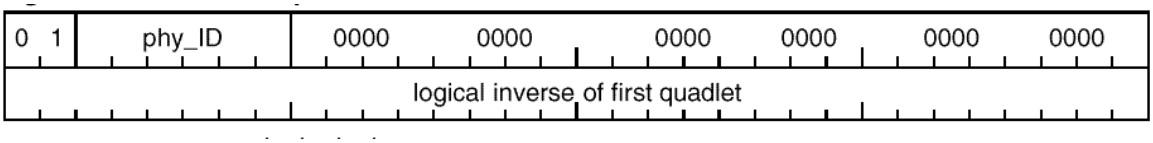
Figure 6. Self-ID Packet Format

Table 8. Self ID Packet Fields

Field Definition	Meaning
phy_ID	Physical node identifier
L	Link enabled register Logical AND of PHYLPS signal and the Link_active register
gap_cnt	Gap_Count register current value of Gap Count register
Sp	Max_Phy_Speed is 10b (S100, S200 and S400 capable)
C	Contender register current value of C register
Pwr	Power class register current value of Power class register
p0, p1, p2	p0, p1, p2 port status for port 0, 1, and 2 respectively. 01 - not active (disabled, disconnected or suspended) 10 – active and connected to parent node 11 – active and connected to child node
I	Initiated reset set whenever the node initiated the current bus reset

Link-On Packet

The VT6306 PHY will respond to a Link_on packet addressed to it received on the bus. The packet has the format shown below in Figure 7 If the logical AND of the PHYLPS pin and the Link_active bit is zero, then the PHY will generate a 6.144 MHz signal on the PHYLON pin, until this logical value becomes 1. Otherwise the packet is forwarded to the local link. Note that all Link_on packets received on the bus are forwarded to the local link if it is active, whether or not the packets are addressed to the local node.

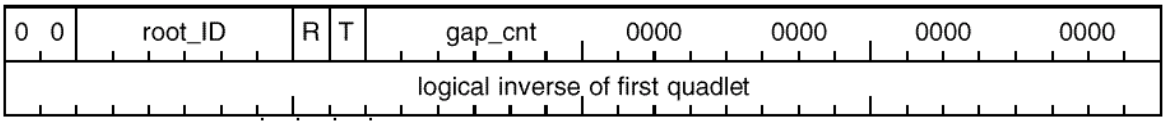


Note: Bit 0 (the lsb) is on the left in the above diagram

Figure 7. Link_on Packet Format

PHY-Configuration Packet

The VT6306 PHY will respond to every PHY configuration packet which it receives on the bus, or from the host for transmission on the bus. The packet has the format shown in the figure below. The fields in the PHY configuration packet are interpreted as shown in the table below. Note that either or both of R and T must be set to 1.



Note: Bit 0 (the lsb) is on the left in the above diagram

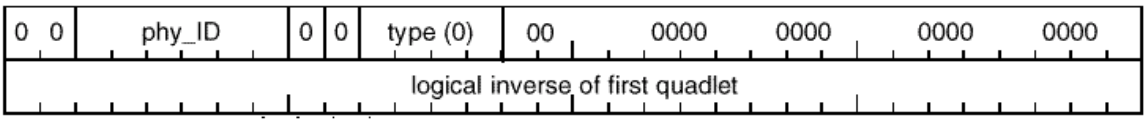
Figure 8. Configuration Packet Format

Table 9. PHY Configuration Packet Fields

Field Name	Meaning
Root_ID	Physical ID. The physical node identifier of the node to become root on next reset
R	Set root. The Force_Root bit in the VT6306 PHY is set if R=1 and Root_ID = the Node_ID of this node
T	Set gap count. If T=1, then the value of the gap count register in the VT6306 is set to gap_cnt.
Gap_cnt	Gap_Count value. New value of Gap Count register

Ping Packet

The VT6306 supports the use of ping for bus round trip calculation. The ping packet has the format shown in the figure below. When the VT6306 receives a ping packet from the bus or from the local link addressed to the node, it responds immediately (without arbitration) with a Self_ID packet to both the bus and the local link.

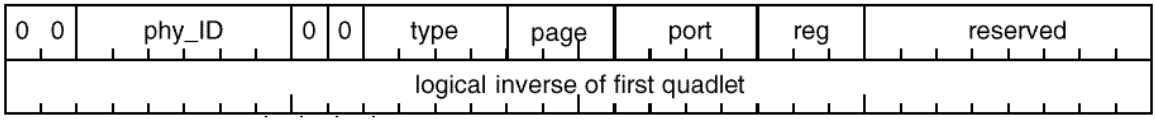


Note: Bit 0 (the lsb) is on the left in the above diagram

Figure 9. Ping Packet Format

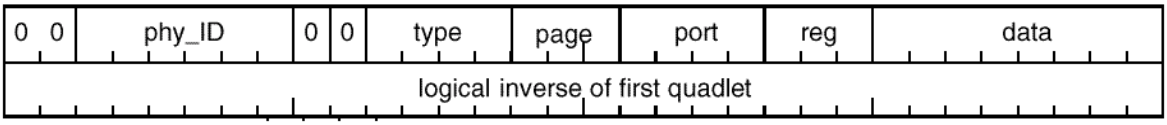
Remote Access and Reply Packets

The VT6306 PHY supports remote access (see Figure 10) to its internal registers. On receipt of a remote access packet addressed to the node (either from the bus or from the host), the VT6306 PHY will immediately respond with the appropriate remote reply packet (seeFigure 11). The remote access packet and the reply packet are also forwarded to the local link. The fields in the remote access and remote reply packets are interpreted as shown in the table below.



Note: Bit 0 (the lsb) is on the left in the above diagram

Figure 10. Remote Access Packet Format



Note: Bit 0 (the lsb) is on the left in the above diagram

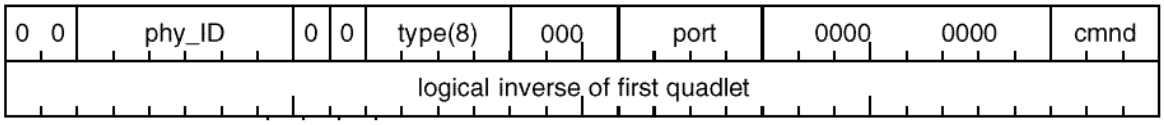
Figure 11. Remote Reply Packet Format

Table 10. Remote Access and Remote Reply Packet Fields

Field Name	Meaning
Phy_ID	Physical node identifier of the destination of the packet (type = 1 or 5) Physical node identifier of the source of the packet (type = 3 or 7)
Type	Type 1 - register read of the base registers Type 3 - register contents (base registers) Type 5 - register read of the paged registers Type 7 - register contents (paged registers)
Page	Page 0 - Port Status Page Page 1 - Product Identification Page Page 2 - 6 - these pages are not implemented, the chip always responds with zero Page 7 contents is reserved for testing
Port	Port. Identify the port for the selected register page. For values 0, 1, 2 and 3, the page is as defined in Table 5 (PHY Register Page 0 Bit Field Descriptions). For all other values the VT6306 always responds with zero.
Reg	If type = 1, then reg directly addresses one of the base registers. If type = 5, then reg addresses 1000b +reg in the selected page and port.
Data	Current value of the VT6306 register addressed by the immediately preceding Remote Access packet (reserved and unimplemented fields and registers are returned as zero).

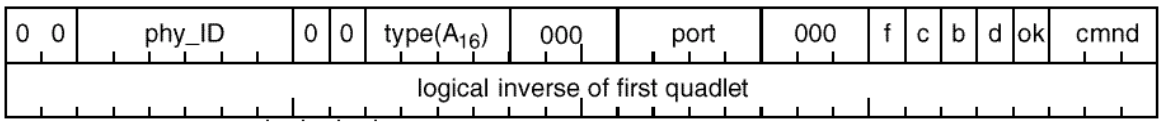
Remote Command and Confirmation Packet

The reception of the resume packet shown in Figure 12 causes the VT6306 to reply with the corresponding remote confirmation packet shown in Figure 13 for all ports that are active. After sending the confirmation packets, the VT6306 will start the requested operation if the OK bit was set. The fields in the remote command and remote confirmation packets are interpreted as shown in the table below



Note: Bit 0 (the lsb) is on the left in the above diagram

Figure 12. Remote Command Packets Format



Note: Bit 0 (the lsb) is on the left in the above diagram

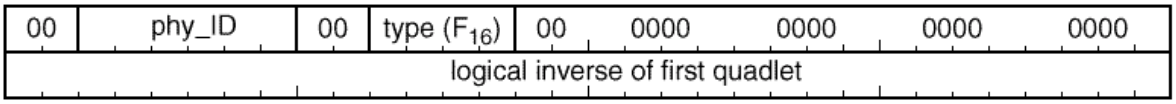
Figure 13. Remote Confirmation Packets Format

Table 11. Remote Command and Confirmation Packet Fields

Field Name	Meaning
phy_ID	Physical node identifier of the destination of the packet (type = 8) Physical node identifier of the source of the packet (type = A 16)
type	hex 8 - remote command packet hex A - remote confirmation packet, the cmd value is from the immediately preceding remote command packet
port	Identify the port for the command or confirmation. For values other than 0, 1, 2 and 3, the VT6306 always responds with the OK bit set to zero in the confirmation packet (means failure).
f	current value of the Fault bit from register 1001b for the addressed port
c	current value of the Connect bit from register 1000b for the addressed port
b	current value of the Bias bit from register 1000b for the addressed port
d	current value of the Disabled bit from register 1000b for the addressed port
ok	1 if the immediately preceding remote command was accepted by the VT6306, 0 otherwise
cmnd	0,3,7- NOP 1 - Transmit TX_DISABLE_NOTIFY then disable the port 2 - Initiate suspend 4 - Clear the port Fault bit 5 - Enable port 6– Resume port

Resume Packet

The reception of the resume packet shown in the figure below causes the VT6306 to commence resume operations for all ports that are both connected and suspended. This is equivalent to setting the resume variable TRUE for each of these ports. The resume packet is broadcast; there is no reply. The fields in the resume packets are interpreted as shown in the table below.



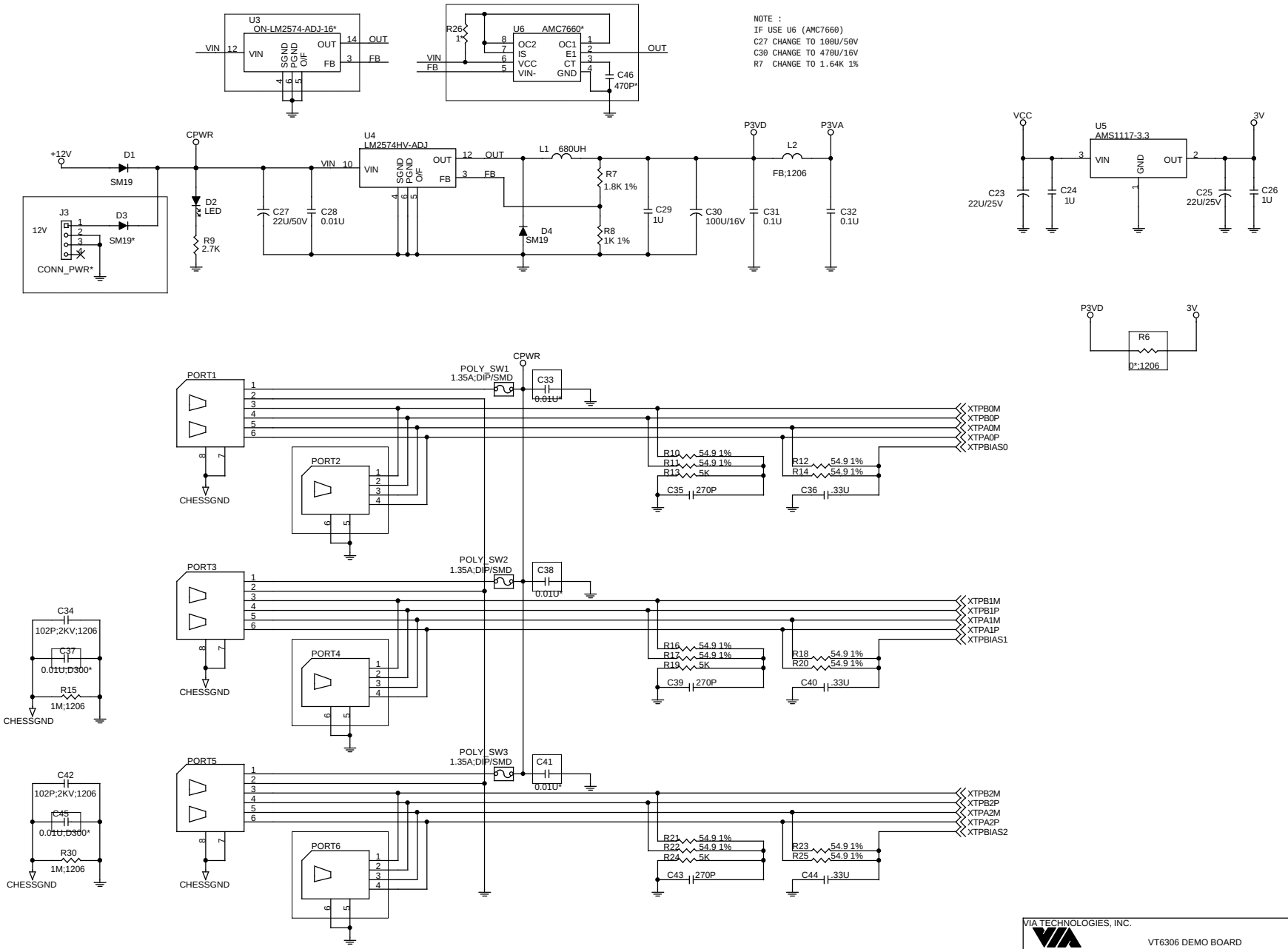
Note: Bit 0 (the lsb) is on the left in the above diagram

Figure 14. Resume Packet Format

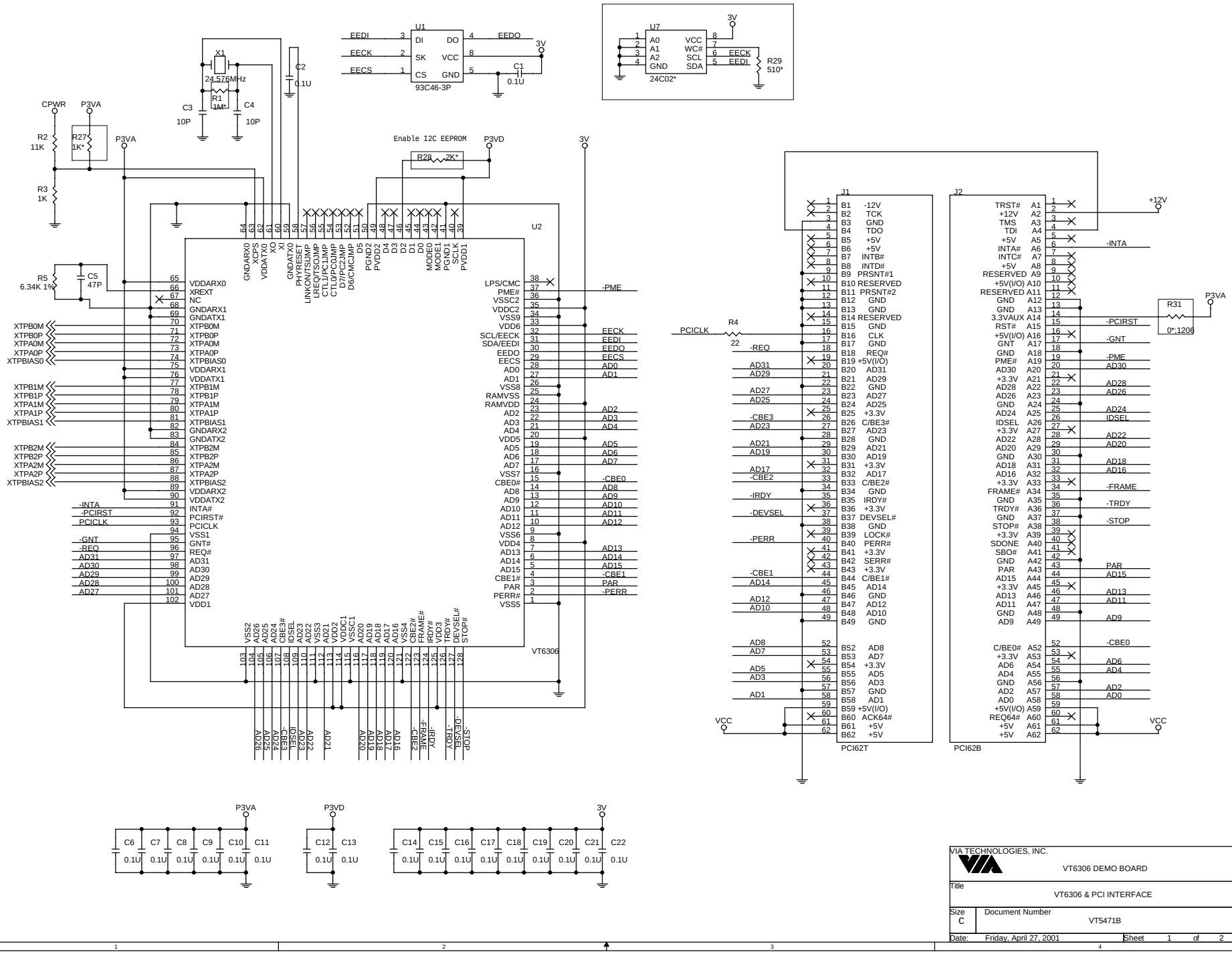
Table 12. Resume Packet Fields

Field Name	Description
Phy_ID	Physical node identifier of the source of this packet
Type	Hex F. Indicates resume packets

APPLICATION SCHEMATICS



VIA TECHNOLOGIES, INC.	VT6306 DEMO BOARD	
Title	1394 CONNECTOR AND POWER CIRCUIT	
Size: C	Document Number: VT5471B	Rev: 0.1
Date: Friday, April 27, 2001	Sheet 2 of 2	



VIA TECHNOLOGIES, INC.			
	VT6306 DEMO BOARD		
Title	VT6306 & PCI INTERFACE		
Size: C	Document Number: VT5471B		Rev: 0.1
Date: Friday, April 27, 2001	Sheet 1 of 2		

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Comment
T_{STG}	Storage temperature	-55	125	^oC	
T_C	Case operating temperature	0	55	^oC	
V_{CC}	Power supply voltage	-0.5	4.0	Volts	
V_I	Input voltage	-0.5	5.5	Volts	
V_O	Output voltage at any output	-0.5	V_{CC} + 0.5	Volts	V_{CC} = 3.1 – 3.6V
V_{ESD}	Electrostatic discharge		2	kV	Human Body Model

Note: Stress above the conditions listed may cause permanent damage to the device. Functional operation of this device should be restricted to the conditions described under operating conditions.

DC Characteristics

T_C = 0-55^{o}C, V_{CC} = 3.3V+/-5%, GND = 0V

Symbol	Parameter	Min	Max	Unit	Condition
V_{IL}	Input Low Voltage	-0.50	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5	V	
V_{OL}	Output Low Voltage	-	0.45	V	I_{OL}=4.0mA
V_{OH}	Output High Voltage	2.4	-	V	I_{OH}=-1.0mA
I_{IL}	Input Leakage Current	-	+/-10	uA	$0<V_{IN}<V_{CC}$
I_{OZ}	Tristate Leakage Current	-	+/-20	uA	$0.45<V_{OUT}<V_{CC}$

Power Characteristics

T_C = 0-55^{o}C, V_{CC} = 3.3V+/-5%, GND = 0V

Symbol	Parameter	Typ	Max	Unit	Condition
I_{CC-PD}	Power Supply Current – VCC			mA	Power Down or Suspend
$I_{CCRAM-PD}$	Power Supply Current – VCCRAM			mA	Power Down or Suspend
$I_{CCSUS-PD}$	Power Supply Current – VCCSUS			mA	Power Down or Suspend
I_{CC}	Power Supply Current – VCC			mA	S400, three ports transmitting
I_{CCRAM}	Power Supply Current – VCCRAM			mA	S400, three ports transmitting
I_{CCSUS}	Power Supply Current – VCCSUS			mA	S400, three ports transmitting
I_{CCARX}	Power Supply Current – VCCARXn			mA	S400, three ports transmitting
I_{CCATX}	Power Supply Current – VCCATXn			mA	S400, three ports transmitting
P_D	Power Dissipation			W	S400, three ports transmitting

Recommended Operating Conditions - PHY

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{CC}	Supply voltage		3	3.3	3.6	V
V_{IL1}	Input Low Voltage	PHYCMC, PHYPC[0:2]	-0.5		1.1	V
V_{IH1}	Input High Voltage	PHYCMC, PHYPC[0:2]	2.2		V_{CC} +0.5	V
V_{IL2}	Input Low Voltage	PHYRST#	-0.5		0.9	V
V_{IH2}	Input High Voltage	PHYRST#	2.1		V_{CC} +0.5	V
I_O	TPBIAS output current		-1.2		1.2	mA
I_{OL} , I_{OH}	Output High/Low current		-16		16	mA
T_{PU}	Power-up reset time	PHYRST# input	0.5			ms
V_{ID}	Differential input voltage	TPA/TPB cable input during data reception	118		260	mV
V_{IDA}	Differential input voltage	TPA/TPB cable input during arbitration	168		265	mV
V_{IC}	Common mode input voltage		1.165		2.515	V
	Receive input jitter	S400			+/-0.5	ns
	Receive input skew	S400			+/-0.5	ns
f_{XSTAL}	Crystal or external clock frequency	XI	24.5735	24.576	24.5785	MHz

Analog Signal Characteristics

Unless otherwise noted, all test conditions are as follows:
T_C = 0 to +55^{0}C
V_{CC} = 3.3V +/- 10%
24.576 MHz +/- 0.01%
XRES = 6.34 K +/- 1%, no load

TPA/TPB Driver Characteristics

Symbol	Parameter	Condition	Min	Max	Unit
V_{OD}	Output signal amplitude	Differential, 54.9 Ohm	172	265	mV
	Transmitter skew	S400		0.1	ns
	Transmitter jitter	S400		0.15	ns
	Data output rise/fall time	S100(10%-90%)	0.5	3.2	ns
		S200(10%-90%)	0.5	2.2	ns
		S400(10%-90%)	0.5	1.2	ns
V_{OFF}	OFF state differential voltage	Peak-to-peak, differential, 54.9 Ohm		20	mV
I_{OD}	Driver difference current	Speed signaling OFF, XTPAP, XTPAM, XTPBP, XTPBM	-1.05	1.05	mA
	Common mode speed signaling current	S100, XTPBP, XTPBM	-0.81	-0.44	mA
		S200, XTPBP, XTPBM	-4.84	-2.53	mA
		S400, XTPBP, XTPBM	-12.4	-8.10	mA

TPA/TPB Receiver Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Z_{ID}	Differential input impedance	Driver disabled			4	pF
				14		Kohm
Z_{IC}	Common mode impedance	Driver disabled			24	pF
			20			Kohm
V_{TH-R}	Receiver input threshold voltage	Driver disabled	-30		30	mV
V_{TH-CB}	Cable bias detect threshold, XTPBx cable inputs	Driver disabled	0.6		1.0	V
V_{TH+}	Positive arbitration comparator threshold voltage	Driver disabled	89		168	mV
V_{TH-}	Negative arbitration comparator threshold voltage	Driver disabled	-168		-89	mV
$V_{TH-S200}$	S200 speed signal threshold	Driver disabled	49		131	mV
$V_{TH-S400}$	S400 speed signal threshold	Driver disabled	314		396	mV
I_{CD}	Connect Detect output at TPBIAS pins				76	uA

PHY Characteristics

Symbol	Parameter	Condition	Min	Max	Unit
	Power status threshold	CPS input with 1K/11K voltage divider	7.8	40	V
	TPBIAS output voltage	At I_O current	1.665	2.015	V

PACKAGE MECHANICAL SPECIFICATIONS

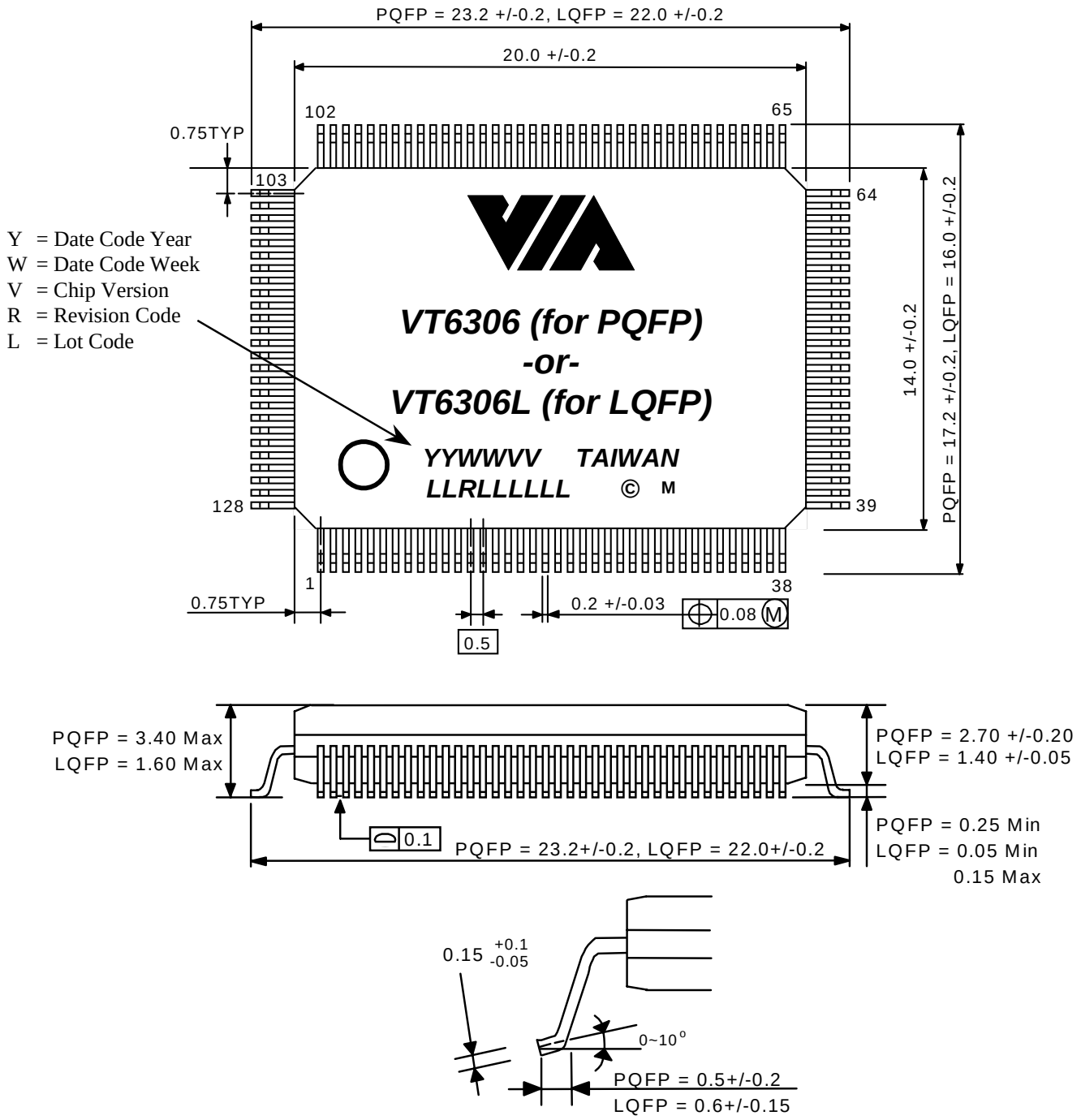


Figure 15. Mechanical Specifications – 128 Pin PQFP / LQFP Package