VL82C205A

PAGE-MODE/INTERLEAVE CONTROLLER

FEATURES

- Supports 16 MHz 80286 operation with 100 ns DRAMs, 20 MHz with 80 ns DRAMs
- Supports two bank interleaved page-mode DRAM accesses for PC/AT-compatible systems
- Speed upgrades to 20 MHz
- Companion to VL82CPCAT-16 and VL82CPCAT-20, 16/20 MHz PC/AT-compatible chip sets
- 13 chip PC/AT implementation (non-memory chips)
- Less than 0.6 wait state average DRAM performance
- Low power CMOS technology
- 68-pin PLCC package
- Backward compatible with VL82C205

DESCRIPTION

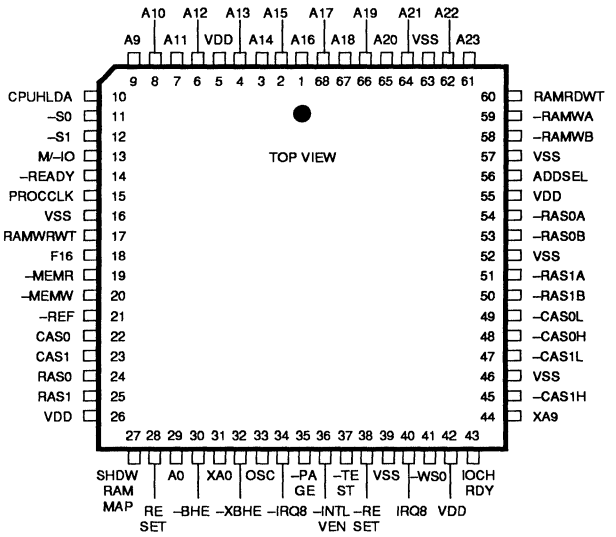
The VL82C205A is a page-mode memory controller for the VLSI VL82CPCAT-16 and VL82CPCAT-20, 16/20 MHz PC/AT-compatible chip sets.

This chip, in addition to the other five chips from the VLSI chip sets, allows two bank interleaved page-mode memory cycles to be run. This allows a 16 MHz processor to use page-mode 100 ns DRAMs and still have less than 0.6 wait states performance.

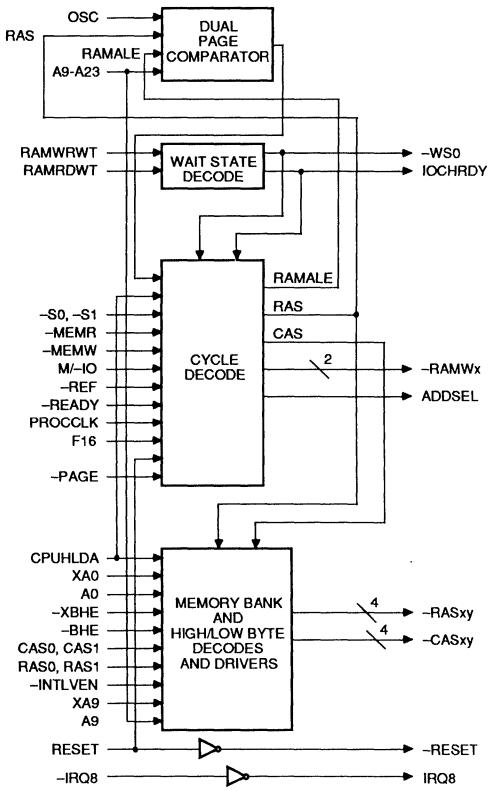
When using page-mode, accesses to each bank that are within 512 bytes of the last access are performed with zero wait states. Accesses that are outside that range are performed in two wait states.

PIN DIAGRAM

VL82C205A



BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Clock Freq.	Package
VL82C205A-16QC	16 MHz	Plastic Leaded Chip Carrier (PLCC)
VL82C205A-20QC	20 MHz	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature is 0°C to +70°C.

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Type	Signal Description
A9-A23	9-6, 4-1, 68-64, 62, 61	I	Upper Address Bits from the CPU - These inputs are latched any time the –RASxy signals go active. On any following memory reads, the address bits are compared to the latched value to determine if a page hit has occurred.
CPUHLDA	10	I	CPU Hold Acknowledge - This input is used to determine which signals are used to initiate and terminate memory cycles. When CPUHLDA is low, the status signals –S0, –S1 and M/–IO along with –READY are used to control memory cycles. When CPUHLDA is high, the inputs –MEMR and –MEMW are used to generate the DRAM control signals.
–S0	11	I	Status 0 - This input is used along with –S1 and M/–IO to determine which type of bus cycle is being requested by the CPU.
–S1	12	I	Status 1 - This input is used along with –S0 and M/–IO to determine which type of bus cycle is being requested by the CPU.
M/–IO	13	I	Memory or I/O select - This input is used along with –S0 and –S1 to determine which type of bus cycle is being requested by the CPU.
–READY	14	I	An input used to determine when to terminate the current memory access to the DRAMs.
PROCCLK	15	I	This is the main clock input to the VL82C205A and should be connected to the same signal that drives the 80286 CLK pin.
RAMWRWT RAMRDWT	17 60	I I	The wait select inputs control the number of wait states to be used for memory accesses when the –PAGE input is high. If RAMRDWT is low, zero wait state read cycles are generated. If RAMWRWT is low, zero wait state write cycles are generated. If either signal is high, one wait state memory cycles are generated for the read or write. These are normally jumpers and are common to the VL82C201 pins. They should be held high in page-mode operation (–PAGE=low).
F16	18	I	The F16 input comes from the memory controller chip and is used to indicate that the current address is in the on-board memory address space.
–MEMR	19	I	Memory Read - An input which is used to determine when memory read accesses to the DRAMs should occur if CPUHLDA is high.
–MEMW	20	I	Memory Write - An input which is used to determine when memory write accesses to the DRAMs should occur if CPUHLDA is high.
–REF	21	I	Refresh - The –REF input is used by the VL82C205A to force the ADDSEL output low.
CAS0	22	I	CAS Enable Input for Bank 0 - This input is used along with CAS1, RAS0, and RAS1 to determine which bank of DRAM should be accessed.
CAS1	23	I	CAS Enable Input for Bank 1 - This input is used along with CAS0, RAS0, and RAS1 to determine which bank of DRAM should be accessed.
RAS0	24	I	RAS Enable Input for Bank 0 - This input is used along with RAS1, CAS0, and CAS1 to determine which bank of DRAM should be accessed.
RAS1	25	I	RAS Enable Input for Bank 1 - This input is used along with RAS0, CAS0, and CAS1 to determine which bank of DRAM should be accessed.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
SHDWRAMMAP	27	I	Shadow RAM Map - An active high input that indicates the system is using the shadow mode (see the VL82C202 description for complete discussion of shadow mode). This signal is used to generate RAS and CAS outputs while doing memory writes during the copying of ROM into shadow RAM. This is needed because the F16 signal is inhibited during the writes.
RESET	28	I	This input is the main reset signal for the page-mode controller chip.
–RESET	38	O	This output is the logical inversion of the RESET input.
A0	29	I	A0 is an input signal from the CPU. It is used when CPUHLDA is low to enable the appropriate low byte –CAS output during a memory cycle.
–BHE	30	I	Byte High Enable - An input signal from the CPU. It is used when CPUHLDA is low to enable the appropriate high byte –CAS output during a memory cycle.
XA0	31	I	XA0 is sampled when CPUHLDA is high to enable the appropriate low byte –CAS output during a memory cycle.
–XBHE	32	I	–XBHE is sampled when CPUHLDA is high to enable the appropriate high byte –CAS output during a memory cycle.
OSC	33	I	The OSC clock input is used as a fixed frequency to determine when a RAS precharge is required.
–IRQ8	34	I	This input is the active low interrupt request from the real-time clock. It is inverted and sent out as IRQ8.
IRQ8	40	O	This output is the logical inversion of the –IRQ8 input.
–PAGE	35	I	The –PAGE input controls the type of memory accesses to be performed for CPU requests. When –PAGE is low, the VL82C205A will generate zero wait state page-mode accesses on page hits. When –PAGE is high, the VL82C205A will sample RAMWRWT or RAMRDWT to generate normal zero or one wait state memory accesses.
–INTLVEN	36	I	Interleaving - –INTLVEN is used to enable two bank interleaving when page-mode is active.
–TEST	37	I	An active low input which should be pulled high through an external pull-up resistor. When pulled low, it will force the page-mode controller to put all output pins into a high impedance state to isolate it from other parts in the system.
–WS0	41	O	Wait State 0 - An active low output which is pulled low any time the page-mode controller wants the current bus cycle to be a zero wait state cycle. It requires an external 300 ohm pull-up resistor.
IOCHRDY	43	O	I/O Channel Ready - An output which is pulled low when the controller wants to entend the memory cycle. It requires an external 300 ohm pull-up resistor.
XA9	44	I	XA9 is sampled when two bank interleave is active and CPUHLDA is high to enable the appropriate –RASxy output.
–CAS1H	45	O	Column Address Strobe 1 High - This active low column address strobe should be connected directly to the DRAMs for the high byte of the upper bank. It is enabled for memory accesses to bank 1 when –BHE is low in CPU mode or when –XBHE is low in non-CPU mode.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
–CAS1L	47	O	Column Address Strobe 1 Low - This active low column address strobe should be connected directly to the DRAMs for the low byte of the upper bank. It is enabled for memory accesses to bank 1 when A0 is low in CPU mode or when XA0 is low in non-CPU mode.
–CAS0H	48	O	Column Address Strobe 0 High - This active low column address strobe should be connected directly to the DRAMs for the high byte of the lower bank. It is enabled for memory accesses to bank 0 when –BHE is low in CPU mode or when –XBHE is low in non-CPU mode.
–CAS0L	49	O	Column Address Strobe 0 Low - This active low column address strobe should be connected directly to the DRAMs for the low byte of the lower bank. It is enabled for memory accesses to bank 0 when A0 is low in CPU mode or when XA0 is low in non-CPU mode.
–RAS0A –RAS0B	54, 53,	O	Row Address Strobes for Bank 0 - These are the active low row address strobes to be connected directly to the DRAMs in the lower bank. RAS timing will vary depending on the operating mode. Refer to the functional description and AC timing diagrams for timing.
–RAS1A –RAS1B	51, 50	O	Row Address Strobes for Bank 1 - These are the active low row address strobes to be connected directly to the DRAMs in the upper bank. RAS timing will vary depending on the operating mode. Refer to the functional description and AC timing diagrams for timing.
ADDSEL	56	O	Address Select - An output used to switch from row to column addresses. It will always follow the –RASxy outputs by half a PROCCLK cycle if in page-mode. In non page-mode, (–PAGE = 1, or CPUHLDA = 1) it follows the –RASxy outputs by half a PROCCLK cycle unless zero wait state is selected. During zero wait state cycles ADDSEL follows –RASxy on the same PROCCLK edge but is delayed. ADDSEL is forced low during refresh cycles. In zero wait state applications, additional external delay may be required to insure proper address hold time depending on the DRAM specifications.
–RAMWB	58	O	RAM Write B - Used to get an early write enable signal to the DRAMs to support page-mode timing and zero wait state write cycles. It will go low during the second phase of any memory write cycle. –RAMWB will return high at the end of the bus cycle when –READY is sampled low. –RAMWB is functionally identical to –RAMWA. Each output provides sufficient drive for a single 18-bit bank.
–RAMWA	59	O	RAM Write A - Used to get an early write enable signal to the DRAMs to support page-mode timing and zero wait state write cycles. It will go low during the second phase of any memory write cycle. –RAMWA will return high at the end of the bus cycle when –READY is sampled low. –RAMWA is functionally identical to –RAMWB. Each output provides sufficient drive for a single 18-bit bank.
VSS	16, 39, 46, 52, 57, 63		System Ground
VDD	5, 26, 42, 55		System Power: 5 V

FUNCTIONAL DESCRIPTION

The VL82C205A consists of several major blocks, including the page hit detection logic, bank select logic, RAS and CAS generation, RAS time-out detection, non-page-mode timing support, time base generation and glue-collection. For a more detailed understanding of the VL82C205A, refer to the block diagram.

PAGE-MODE CONTROLLER

In this discussion, the following terms are used:

- Page refers to a block of 512 bytes, for which only the lower nine address bits change.
- Bank refers to 18 bits of DRAM (16-bit word plus two parity bits).
- High/Low Byte refers to the upper or lower 8 bits of a 16-bit word.

The VL82C205A controller may be used in either page-mode or non page-mode, as chosen by input –PAGE. In page-mode, any read access within the same page of the previous memory access is performed with zero wait states. Internal latches track the successive address references permitting the shorter cycles to be used automatically.

For references on page, the DRAM row addresses do not change. Therefore, the RAS lines remain asserted continuously between DRAM cycles. (The DRAM column lines are effectively mapped to the lower nine bits of the address space.)

An access outside of the 512-byte page or a write operation forces two wait states. Under that condition, the RAS lines are de-asserted for the required precharge time.

With the controller's page-mode operation enabled, an average of 0.6 wait states is used.

PAGE-MODE OPERATION WITH TWO BANK INTERLEAVE

When page-mode operation is selected and two 18-bit banks of DRAM are installed, it is possible to utilize the two bank interleave capability of the VL82C205A. This feature allows page-mode accesses to two disjointed pages, one in each DRAM bank. Interleaving is accomplished using the A9, XA9, CAS0 and CAS1 input signals.

RAS/CAS GENERATION

Four RAS and CAS signals are brought to supply sufficient drive for nine bits of DRAM without the need for off-chip buffering and allows for equal loading.

The controller attempts to generate RAS at the earliest time possible. A number of conditions are monitored by the chip, which could preclude early RAS. The RAS precharge timing logic then generates RAS and CAS based on them.

When page-mode and two bank interleave are active, the CAS0x, RAS0x, and CAS1x, RAS1x outputs are used to select the appropriate DRAM bank. At all other times, the four RAS outputs are identical. The CASxH and CASxL outputs are used to select the appropriate high or low byte within a bank.

RAS-ACTIVE TIMEOUT WARNING

An internal counter monitors RAS to detect maximum RAS active time. After approximately 10 µs, a RAS precharge is performed.

Input OSC is used to monitor RAS. A maximum of 72 consecutive read operations at 16 MHz to the same page can take place before a false page miss is inserted to do the RAS precharge.

WAIT STATE GENERATION

IOCHRDY and –WS0 are the outputs that indicate how many wait states are in the current cycle. –WS0 is pulled low for all page hits. Other zero wait state cycles are handled by the VL82C201. This is an open-drain output and a 300 ohm pull-up resistor is required.

IOCHRDY is pulled low for all two wait state cycles. This is a three-state output. When IOCHRDY goes high (inactive), the VL82C205A drives the signal for half a PROCCLK cycle (15 ns), then goes into three-state (see the logic below). A 300 ohm pull-up resistor is required to hold the signal high and to pull-up the other system open-drain outputs connected to IOCHRDY.

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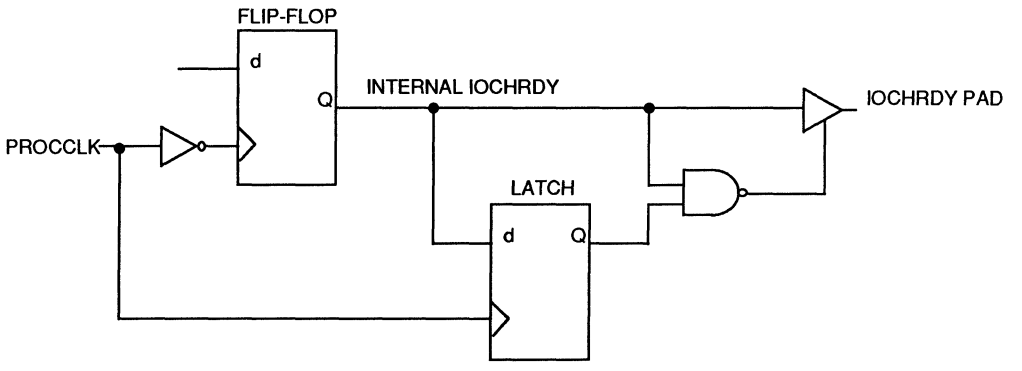
FIGURE 1. IOCHRDY GENERATION



TWO BANK INTERLEAVE DECODING
When page-mode and two bank interleave are active, the DRAM banks are decoded as follows:

Bank 1 = (CAS1•/A9) + (CAS0•A9)
Bank 0 = (CAS1•A9) + (CAS0•/A9)

Note: XA9 is used instead of A9 when CPUHLDA = 1

CASxH and CASxL are decoded within a bank as follows:

CASxH = (/CPUHLDA•/–BHE) + (CPUHLDA•/–XBHE)
CASxL = (/CPUHLDA•/A0) + (CPUHLDA•/XA0)

NON-CPU MODE
When CPUHLDA = 1, the processor surrenders the bus for Master, DMA, or Refresh modes. In these three modes the –MEMW and –MEMR inputs signify whether memory reads or writes occur. Also, inputs XA0 and –XBHE replace A0 and –BHE in the decoding of the four –CASxy outputs. XA9 replaces A9 in the decoding of memory accesses to Bank 0, or Bank 1 when two bank interleave is active.

–MEMW and –MEMR can be asynchronous to PROCCLK. They are sampled by the falling edge of PROCCLK to synchronize them with the internal state machine.

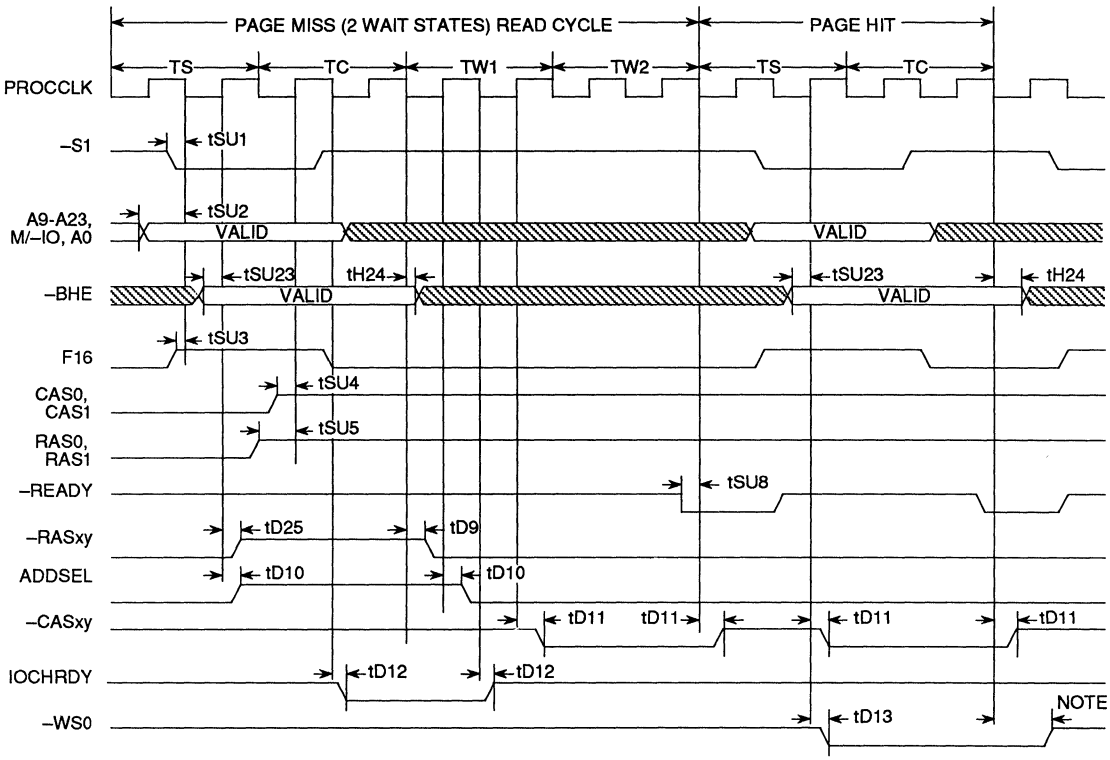
IOCHRDY is never driven active (low) in this mode since the read or write cycles can be extended by keeping –MEMR or –MEMW low (see the waveforms for non-CPU mode timing). Note that if inputs RAMRDWT or RAMWRWT are low, then ADDSEL and the –CASxy outputs go active off the falling edge of PROCCLK.

BACKWARDS COMPATIBILITY WITH THE VL82C205A AND VL82C205
The VL82C205A may be used to directly replace the VL82C205 and will operate in page-mode, non-interleaved operation as if a VL82C205 was used. If Pin 36 is tied high, XA9 (Pin 44) is not used and may be a "No Connect". To utilize the two bank interleave function of the VL82C205A, Pin 44 has to be connected to XA9, and Pin 36 should be tied low.

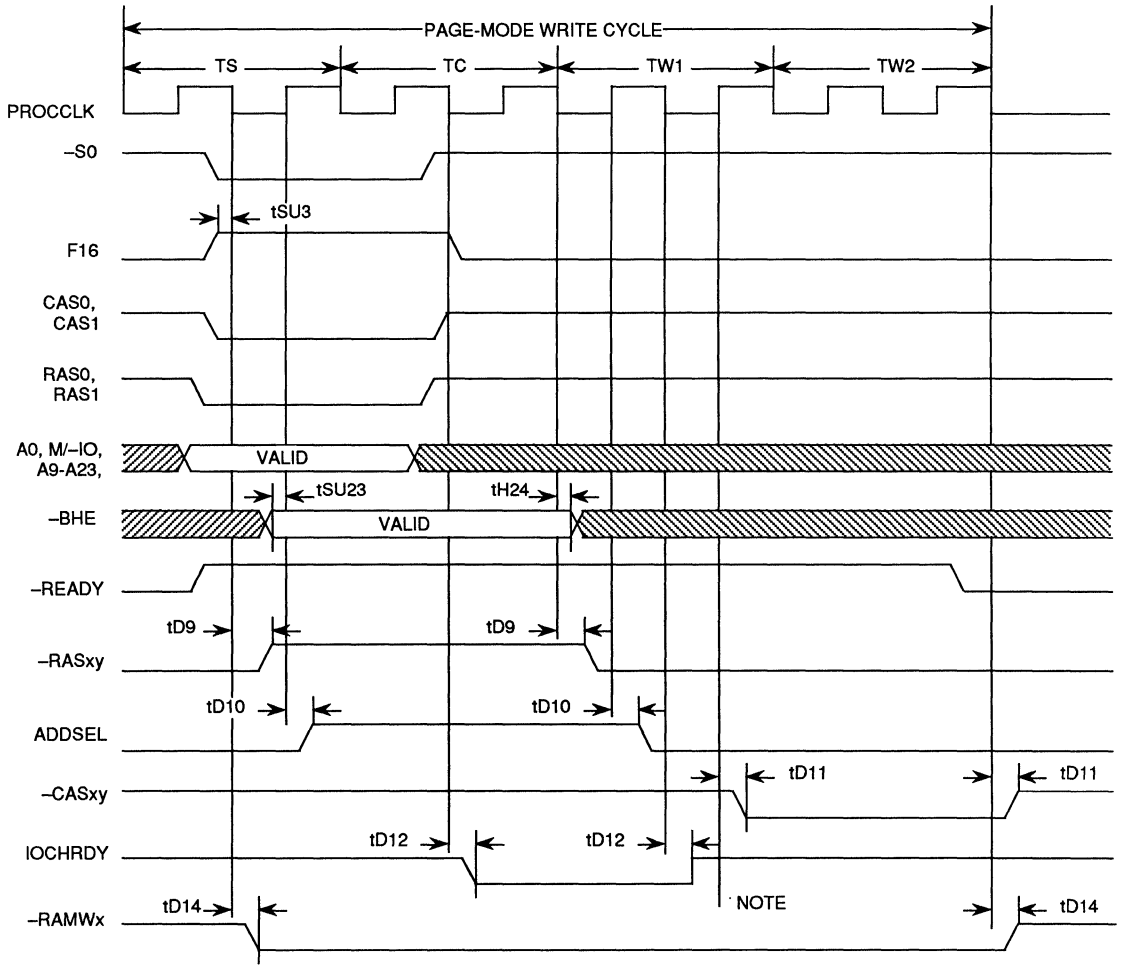
AC CHARACTERISTICS: TA = 0°C to +70°C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	16 MHz		20 MHz		Unit	Condition
		Min	Max	Min	Max		
tSU1	–S0, –S1 to PROCCLK Setup Time	13		9		ns	
tSU2	M/–IO, A9-A23, A0 to PROCCLK Setup Time	33		24		ns	
tSU3	F16 to PROCCLK Setup Time	8		6		ns	
tSU4	CAS0, CAS1 to PROCCLK Setup Time	14		10		ns	
tSU5	RAS0, RAS1 to PROCCLK Setup Time	26		20		ns	
tSU6	–MEMW to PROCCLK Setup Time	10		10		ns	Note 1
tSU7	–MEMR to PROCCLK Setup Time	10		10		ns	Note 1
tSU8	–READY to PROCCLK Setup Time	15		10		ns	
tD9	–RASxy Delay from PROCCLK Falling Edge		19		17	ns	
tD25	–RASxy Delay from PROCCLK Leading Edge		17		15	ns	
tD10	ADDSEL Delay from PROCCLK Leading Edge		20		20	ns	Note 2
tD11	–CASxy Delay from PROCCLK		22		19	ns	Note 3
tD12	IOCHRDY Delay from PROCCLK		20		20	ns	
tD13	–WS0 Active Delay from PROCCLK		20		20	ns	
tD14	–RAMWx Delay from PROCCLK		20		20	ns	
tD15	ADDSEL Delay from –RASxy	2	12	2	12	ns	0 WS Non Page-mode
tD16	–RESET, –IRQ Delay from RESET, IRQ		20		18	ns	
tD17	ADDSEL Delay from –REF		25		25	ns	
t18	PROCCLK Period	31		25		ns	
t19	PROCCLK High Pulse Width	11		9		ns	Measured at 3.6 V
t20	PROCCLK Low Pulse Width	7		6		ns	
t21	PROCCLK Fall Time		4		4	ns	3.6 V to 1.0 V
t22	PROCCLK Rise Time		5		4	ns	3.6 V to 1.0 V
tSU23	–BHE to PROCCLK Setup Time	12		10		ns	
tH24	–BHE Hold Time from PROCCLK	0		0		ns	

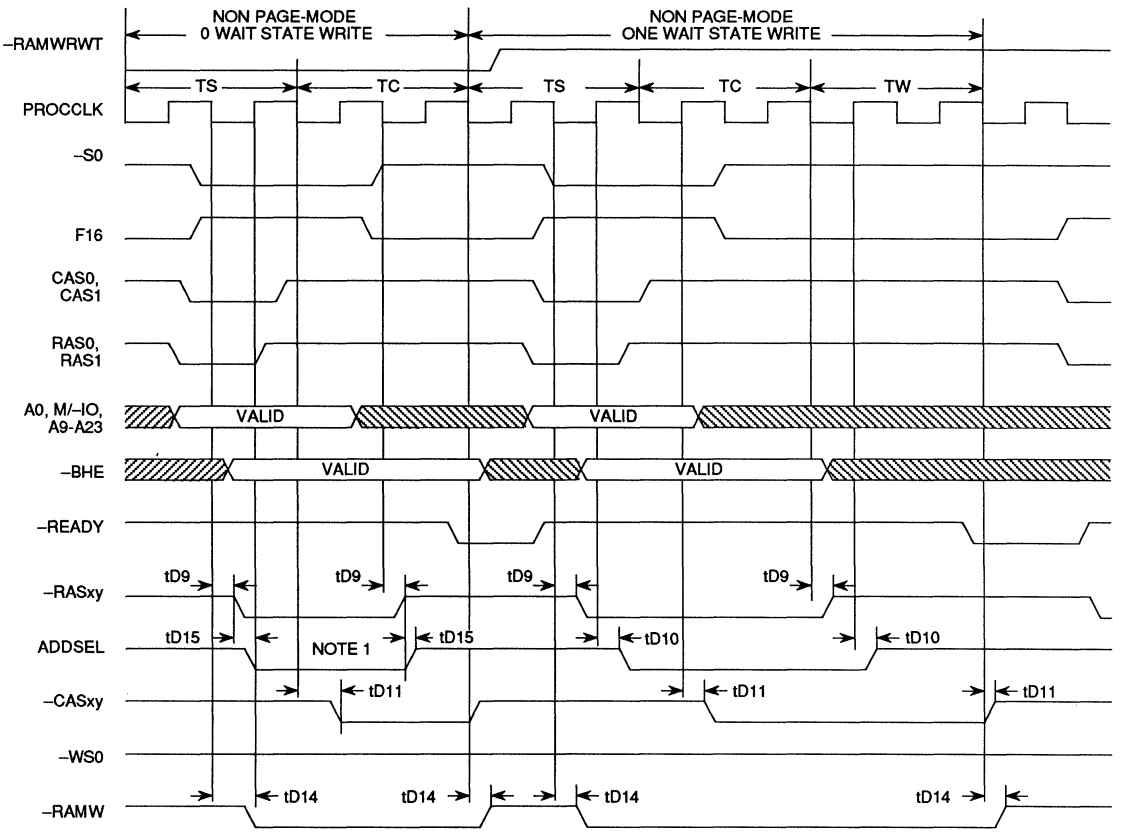
Notes:
1. –MEMR and –MEMW can be asynchronous to PROCCLK. They must meet the setup time to start the appropriate read or write cycle on the falling edge of PROCCLK. This spec is used in testing the parts.
2. ADDSEL is clocked off the rising edge of PROCCLK during all page-mode cycles and during one wait state normal cycles. During zero wait state normal cycles ADDSEL is clocked off the trailing edge of PROCCLK (see spec tD15).
3. –CASxy signals are clocked off different edges of PROCCLK. All transitions from active to inactive (0-1) are clocked off the falling edge of PROCCLK. During all page-mode cycles and all normal mode one wait state cycles, the inactive to active transition is clocked off the rising edge of PROCCLK. During zero wait state normal mode cycles, the inactive to active transition is clocked off the falling edge of PROCCLK.
4. Inputs –PAGE, RAMWRWT and RAMRDWT should be strapped to VDD or VSS to define the proper mode for a specific design.



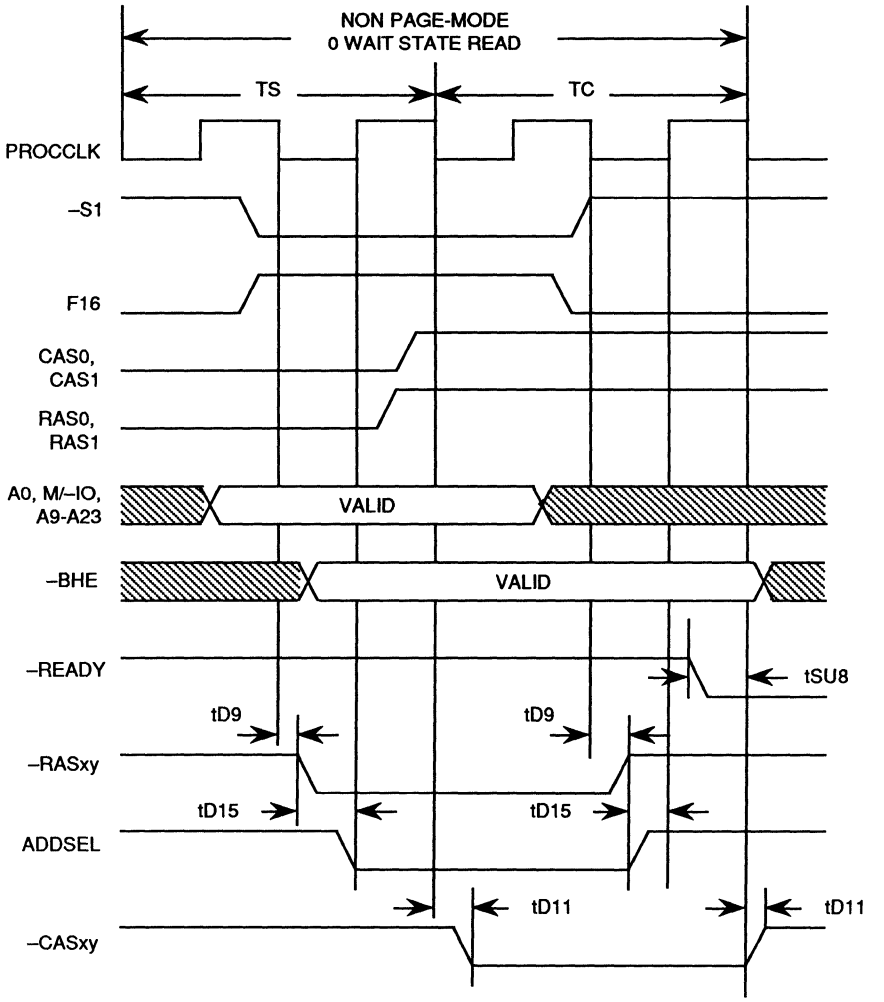
Note: -WS0 is an open drain output. The rise time depends on the size of the pull-up resistor used externally. -WS0 is released by the VL82C205A on the indicated rising edge of PROCCLK.



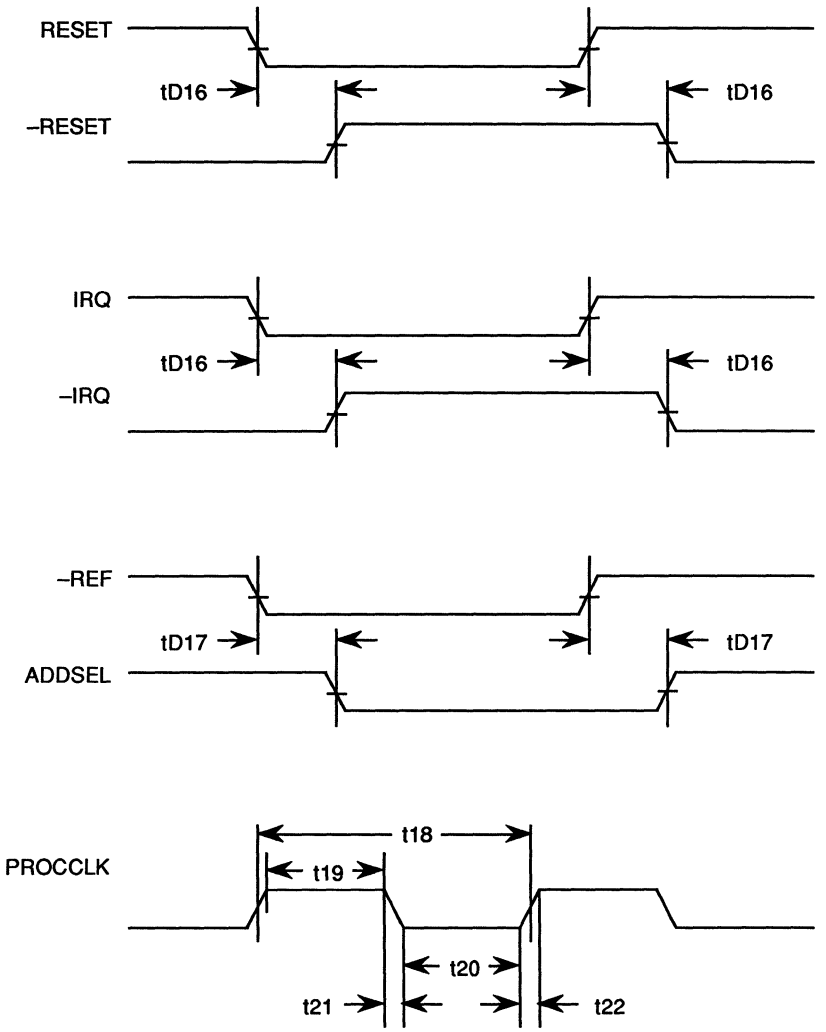
Note: IOCHRDY is three-stated after this PROCCLK rising edge.

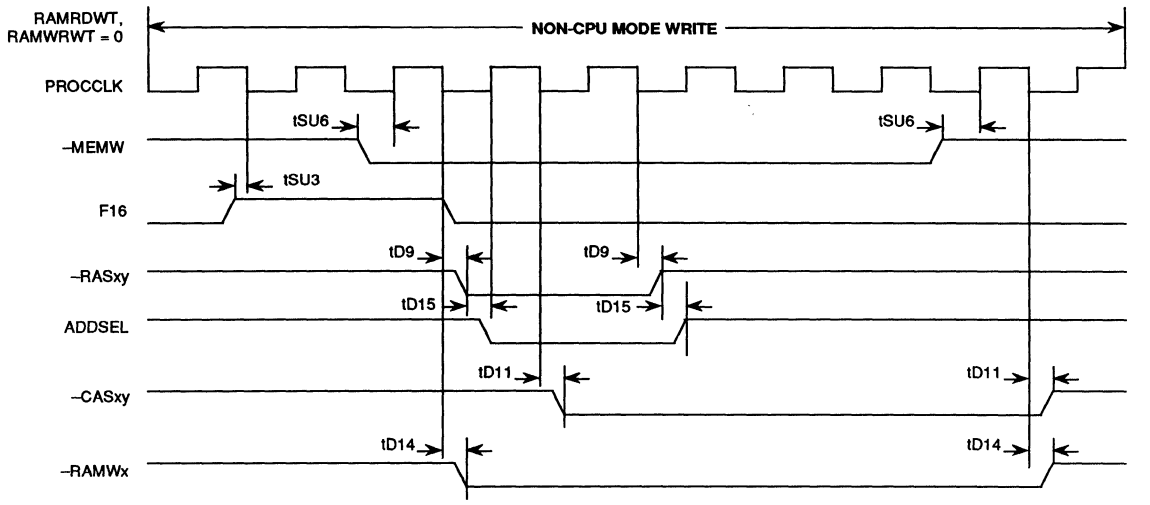


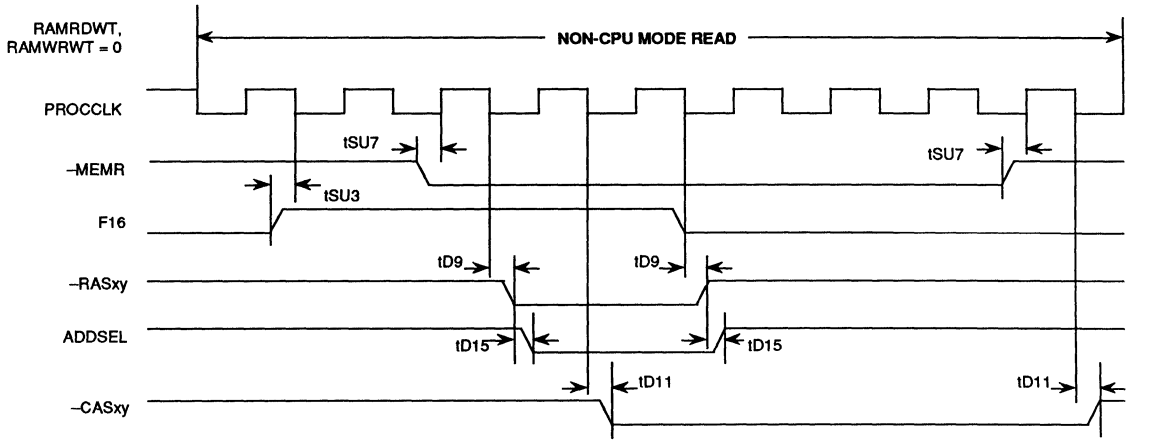
Note: In this mode ADDSEL follows -RASxy off the trailing edge of PROCCLK. The delay between -RASxy and ADDSEL is a minimum of 2 ns and a maximum of 12 ns.

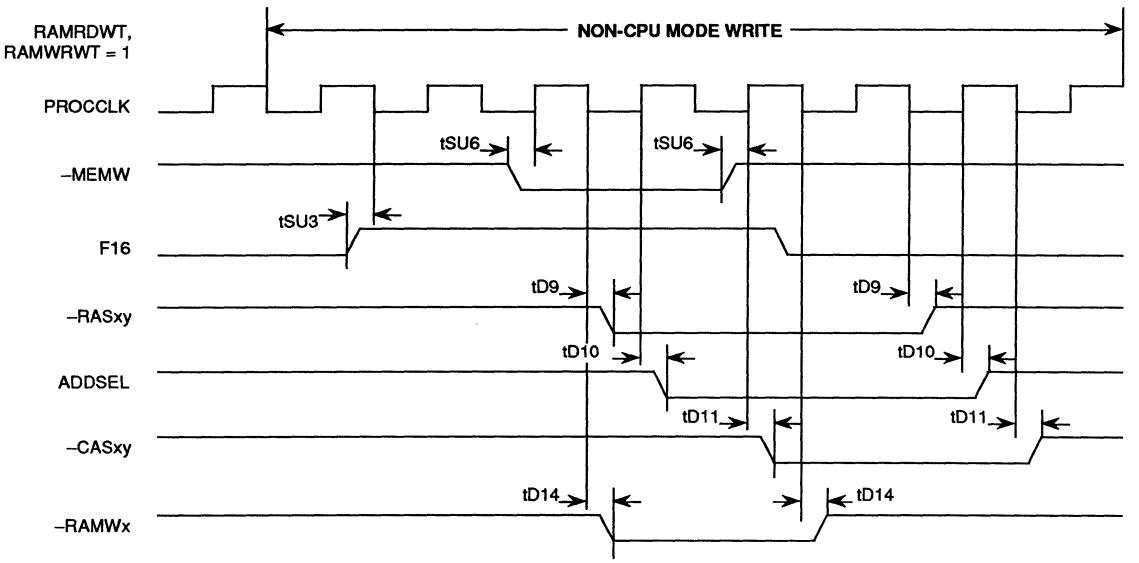

NON PAGE-MODE
0 WAIT STATE READ
TS
TC
PROCCLK
–S1
F16
CAS0,
CAS1
RAS0,
RAS1
A0, M/–IO,
A9-A23
VALID
–BHE
VALID
–READY
tSU8
tD9
tD9
–RASxy
tD15
tD15
ADDSEL
tD11
tD11
–CASxy

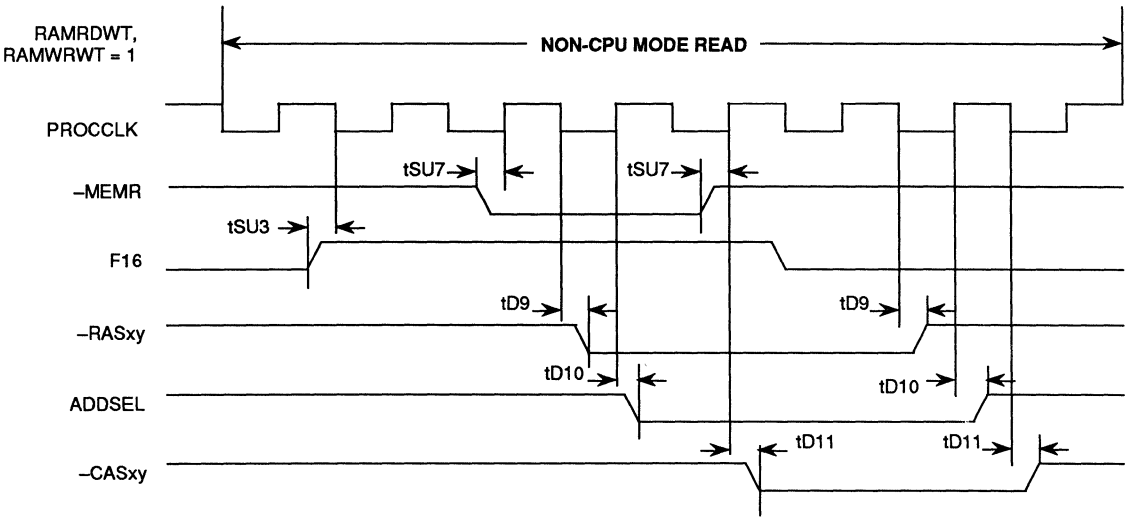
MISCELLANEOUS TIMINGS



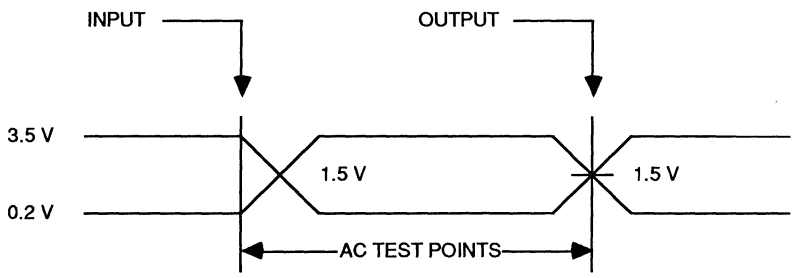

RAMRDWT,
RAMWRWT = 0
NON-CPU MODE WRITE
PROCCLK
tSU6
tSU6
–MEMW
tSU3
F16
tD9
tD9
–RASxy
tD15
tD15
ADDSEL
tD11
tD11
–CASxy
tD14
tD14
–RAMWx


RAMRDWT,
RAMWRWT = 0
NON-CPU MODE READ
PROCCLK
tSU7
tSU7
–MEMR
tSU3
F16
tD9
tD9
–RASxy
ADDSEL
tD15
tD15
tD11
tD11
–CASxy

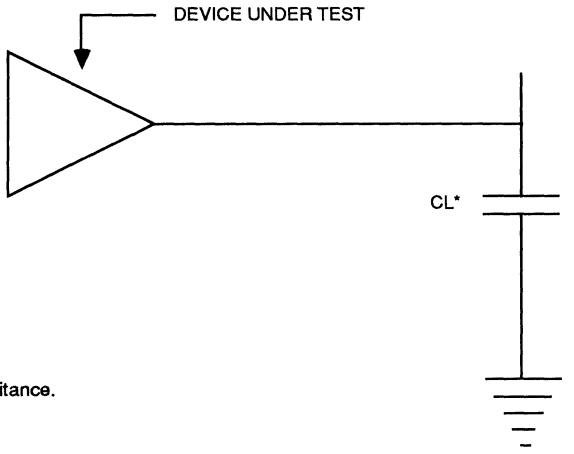

RAMRDWT,
RAMWRWT = 1
NON-CPU MODE WRITE
PROCCLK
tSU6
tSU6
-MEMW
tSU3
F16
tD9
tD9
-RASxy
tD10
tD10
ADDSEL
tD11
tD11
-CASxy
tD14
tD14
-RAMWx


RAMRDWT,
RAMWRWT = 1
NON-CPU MODE READ
PROCCLK
tSU7
tSU7
-MEMR
tSU3
F16
tD9
tD9
-RASxy
tD10
tD10
ADDSEL
tD11
tD11
-CASxy

AC TESTING - INPUT, OUTPUT WAVEFORM



AC TESTING - LOAD CIRCUIT



*Includes scope and jig capacitance.

AC TESTING - LOAD VALUES

Test Pin	CL (pF)
41, 43, 58, 59	200
45, 47-51, 53, 54	100
All Others	50

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	–10°C to +70°C
Storage Temperature	–65°C to +150°C
Supply Voltage to Ground Potential	–0.5 V to +0.3 V
Applied Output Voltage	–0.5 V to +0.3 V
Applied Input Voltage	–0.5 V to +7.0 V
Power Dissipation	500 mW

Stresses above those listed may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: TA = 0°C to +70°C, VDD = 5 V ± 5%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Condition
VOH	Output High Voltage	2.4		V	IOH = –3.3 mA
VOL1	Output Low Voltage		0.45	V	–WS0, IOCHRDY, CL = 200 pF, IOL = 24 mA
VOL2	Output Low Voltage		0.45	V	–RAMWA, –RAMWB, CL = 200 pF, IOL = 8 mA
VOL3	Output Low Voltage		0.45	V	–RASxy, –CASxy, CL = 100 pF, IOL = 8 mA
VOL4	Output Low Voltage		0.45	V	All Other Pins, CL = 50 pF, IOL = 8 mA
VIH	Input High Voltage	2.0	VDD + 0.5	V	
VIL	Input Low Voltage	–0.5	0.8	V	
VIHC	Input High Voltage	3.6	VDD + 0.5	V	PROCCLK
CO	Output Capacitance		16	pF	
CI	Input Capacitance		8	pF	
CIN	Input Pin Capacitance		10	pF	
ILI	Input Leakage Current	–10	10	µA	
IIL	Input Low Current		100	µA	XA9
ISB	Standby Supply Current		100	µA	XA9 Input High
ICC	Operating Supply Current		2	mA	Per MHz Operating Frequency

Note: Inputs = VSS or VDD, outputs are not loaded.