PC/AT-COMPATIBLE MEMORY CONTROLLER

FEATURES

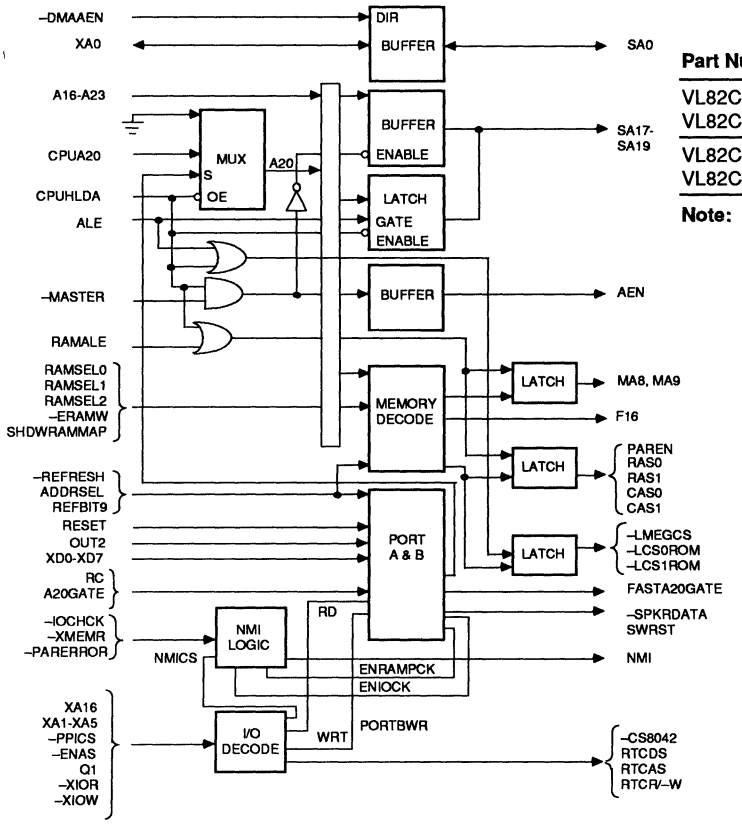
- Fully compatible with IBM PC/AT-type designs
- Completely performs memory control function in IBM PC/AT-compatible systems
- Replaces 20 integrated circuits on PC/AT-type motherboard
- Supports up to 20 MHz system clock
- Device is available as "cores" for user-specific designs
- Designed in CMOS for low power consumption

DESCRIPTION

The VL82C202 PC/AT-Compatible Memory Controller generates the row and column decodes necessary to support the dynamic RAMs used in PC/AT-type systems. In addition, the device allows six motherboard memory options for the user, from 512K-bytes up to a full 8M-byte system. In addition, the VL82C202 provides the chip select for the ROM and RAM memory, and drives the system's speaker. The optional Shadow RAM feature allows up to 384K-bytes of memory space to be copied to and executed out of high speed DRAM instead of slower EPROM.

The device is manufactured with VLSI's advanced high-performance CMOS process and is available in a JEDEC-standard 84-pin plastic leaded chip carrier (PLCC) package. The VL82C202 is part of the PC/AT-compatible chip sets available from VLSI. Please refer to the Selector Guide in the front of this manual.

BLOCK DIAGRAM



ORDER INFORMATION

Part Number	System Clock Freq.	Package
VL82C202-16QC VL82C202-16QI	16 MHz	Plastic Leaded Chip Carrier (PLCC)
VL82C202-20QC VL82C202-20QI	20 MHz	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range:
QC = 0°C to +70°C
QI = –40°C to +85°C.

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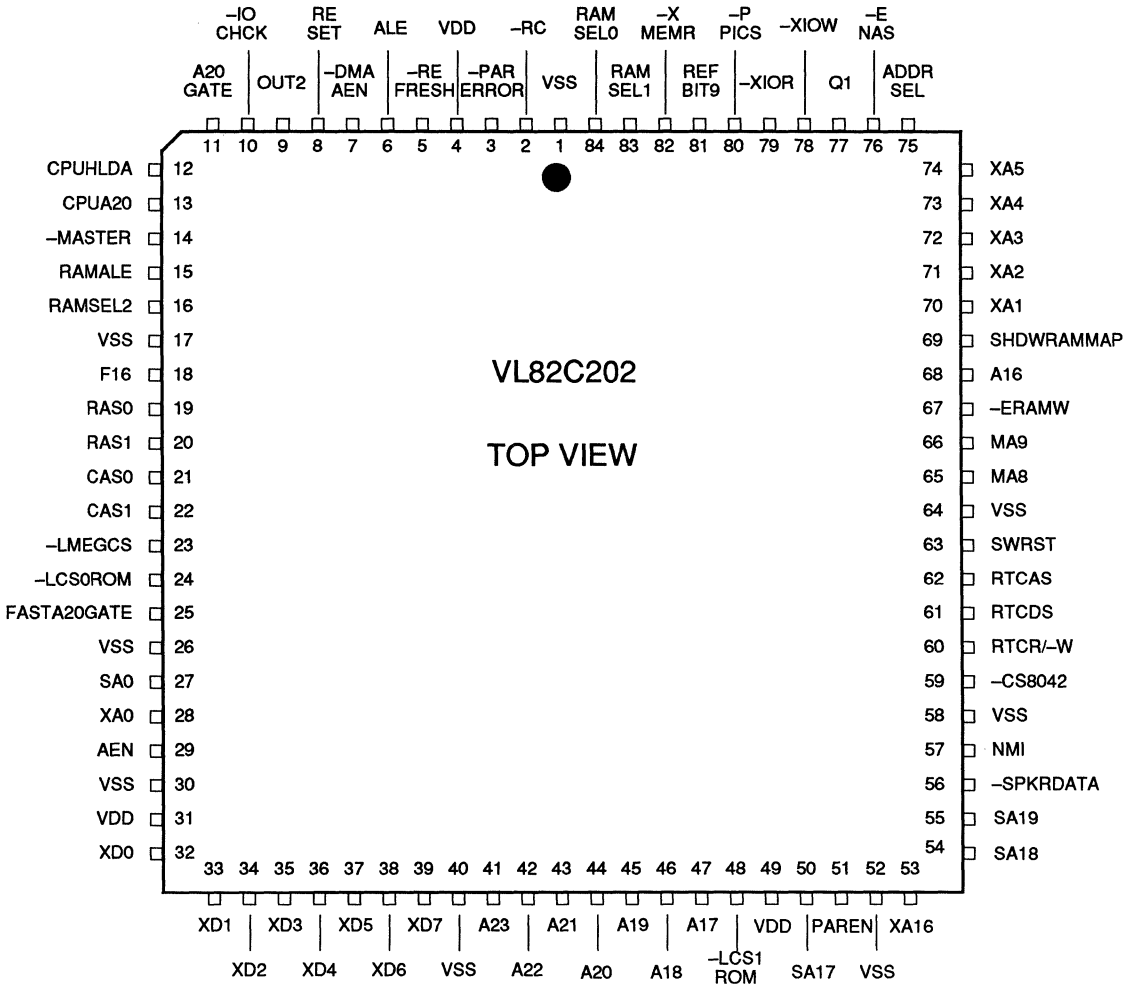
PIN DIAGRAM


VL82C202
TOP VIEW
1 A20 GATE
2 OUT2
3 –DMA AEN
4 –RE FRESH
5 –PAR ERROR
6 VSS
7 RAM SEL1
8 REF BIT9
9 –XIOR
10 Q1
11 ADDR SEL
12 –IO CHCK
13 RE SET
14 ALE
15 VDD
16 –RC
17 RAM SEL0
18 –X MEMR
19 –P PICS
20 –XIOW
21 –E NAS
22 XA5
23 XA4
24 XA3
25 XA2
26 XA1
27 SHDWRAMMAP
28 A16
29 –ERAMW
30 MA9
31 MA8
32 VSS
33 SWRST
34 RTCAS
35 RTCDS
36 RTCR/–W
37 –CS8042
38 VSS
39 NMI
40 –SPKRDATA
41 SA19
42 SA18
43 XA16
44 PAREN
45 VDD
46 A17
47 A19
48 A21
49 A23
50 VSS
51 SA17
52 –LCS1 ROM
53 A18
54 A20
55 A22
56 VSS
57 XD7
58 XD6
59 XD5
60 XD4
61 XD3
62 XD2
63 XD1
64 XD0
65 VDD
66 SA0
67 XA0
68 AEN
69 VSS
70 F16
71 RAS0
72 RAS1
73 CAS0
74 CAS1
75 –LMEGCS
76 –LCS0ROM
77 FASTA20GATE
78 VSS
79 RAMALE
80 RAMSEL2
81 –MASTER
82 CPUA20
83 CPUHLDA

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Type	Signal Description
–RC	2	I	This active low input signal will force a CPU reset when active. It is generated by the keyboard controller and its inverse is OR'ed with Port A bit 0 to form output signal SWRST (pin 63).
–PARERROR	3	I	Parity Error - A low true input used to indicate that a memory parity error has occurred.
–REFRESH	5	I	Refresh - An active low input used to initiate a refresh cycle for the dynamic RAMs.
ALE	6	I	Address Latch Enable - This is a positive edge input that controls the address latches which hold the address during a bus cycle. ALE is not issued for a halt bus cycle.
–DMAAEN	7	I	DMA Address Enable - This is an active low input. It is active whenever DMA is making an access to the system memory.
RESET	8	I	Reset - This active high input signal is the system reset generated from a POWERGOOD. It is synchronized to PROCCLK.
OUT2	9	I	Out 2 - The output of the timer controller. It can be read by the CPU on Port B.
–IOCHCK	10	I	I/O Channel Check - This active low input is asserted by devices on the expansion bus. It will generate a non-maskable interrupt if NMI is enabled. –IOCHCK can be read by the CPU on Port B.
A20GATE	11	I	A20 Gate - Used to select the proper value for address bit 20. CPUA20 is transmitted as A20 if A20GATE is high or Port A bit 1 is high, otherwise A20 is forced low.
CPUHLDA	12	I	CPU Bus Hold Acknowledge - This input indicates ownership of the local CPU bus. When high, this signal indicates that the CPU has three-stated its bus drivers in response to a hold request. When low, it indicates that the CPU bus drivers are active.
CPUA20	13	I	CPU Address Bus Bit 20 - It is transmitted out as A20 if A20GATE is high or if Port A, bit 1 is high.
–MASTER	14	I	Master - An active low input. It is asserted low by devices on the expansion bus. A low indicates that another device is active.
RAMALE	15	I	RAMALE is used to latch RAM address buffers. It is forced high at the end of any bus cycle and will go back low at the end of the status cycle.
RAMSEL2	16	I	RAM Select 2 - Used with RAMSEL0 and RAMSEL1 to select the system RAM configuration.
F16	18	O	An output that indicates an access to on-board memory.
RAS0	19	O	An active high output used to enable the Row Address Strobe to DRAM banks 0 and 3.
RAS1	20	O	An active high output used to enable the Row Address Strobe to DRAM banks 1 and 2.
CAS0	21	O	An active high output used to enable the Column Address Strobe to DRAM banks 0 and 2.
CAS1	22	O	An active high output used to enable the Column Address Strobe to DRAM banks 1 and 3.
–LMEGCS	23	O	Lower Megabyte Chip Select - An active low output that indicates that the lower memory address space (0-1 megabyte) is selected.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
–LCS0ROM	24	O	Latched Chip Select 0 for ROM - An active low output that is the latched chip select for the low 64K-bytes of ROM address space.
FASTA20GATE	25	O	This active high output is the OR of Port A bit 1 and input pin A20GATE.
SA0	27	I/O	System Address Bus Bit 0 - This signal will be an output with the value of XA0 when –DMAAEN is low. It will be an input and drive XA0 when –DMAAEN = 1.
XA0	28	I/O	Peripheral Address Bus Bit 0 - This signal is an output driven by SA0 when –DMAAEN = 1, and an input driving SA0 when –DMAAEN = 0.
AEN	29	O	Address Enable - This is an output signal for the expansion bus. It will go low when –MASTER is active or CPUHLDA is inactive.
XD0-XD7	32-39	I/O	Peripheral Data Bus Bits 0-7 - These are data bits for the peripheral bus. They are outputs when Port A or Port B is being read; otherwise they are inputs.
A16-A19, A21-A23	68, 47-45, 43-41	I	CPU Bus Bits 16-19 and 21-23 - These are the upper bits of the CPU address bus.
A20	44	I/O	Address Bus Bit 20 - Normally an output driven by CPUA20 (see above), but is an input when CPUHLDA = 1 and –MASTER = 1.
–LCS1ROM	48	O	Latched Chip Select 1 for ROM - The active low latched chip select output for the high 64K-bytes of ROM address space.
PAREN	51	O	Parity Check Enabled - Logical OR of CAS0 and CAS1, indicates a RAM memory access so parity check is enabled.
SA17-SA19	50, 54, 55	TSO	System Address Bus Bits 17-19 - A17-A19 are latched by ALE and transmitted out on these outputs when CPUHLDA is inactive. They are driven directly by A17-A19 when CPUHLDA is active and –MASTER is inactive. They are three-stated when –MASTER is active.
XA16	53	I	Peripheral Address Bus Bit 16 - This selects between 64K blocks of memory when CPUHLDA is high.
–SPKRDATA	56	O	Speaker Data - Output to be buffered and sent to the speaker.
NMI	57	O	Non-Maskable Interrupt - This output is the non-maskable interrupt signal for the CPU.
–CS8042	59	O	Chip Select Signal for the Keyboard Controller - This active low output is the chip select signal for the keyboard controller programmable interface device.
RTCR/–W	60	O	Real Time Clock Signal for Read/Write - This is the read/write select output signal for the real time clock. A high indicates a read operation and a low, a write operation.
RTCDS	61	O	Real Time Clock Data Strobe - This is the data strobe for the real time clock.
RTCAS	62	O	Real Time Clock Address Strobe - This is the address strobe for the real time clock.
SWRST	63	O	Software Reset - An active high output that goes to the System Controller chip, where it generates a reset pulse. SWRST is the logical OR of Port A bit 0 and the inverse of input –RC.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
MA8, MA9	65, 66	O	DRAM Memory Address Bus Bits 8-9 - These outputs are the 8th and 9th bits of the DRAM memory address. They are located on the VL82C202 to allow system address mapping. REFBIT9 is multiplexed into MA8 during a refresh cycle.
–ERAMW	67	I	Early RAM Write - This active low input indicates a memory write command. It is used primarily during the mapping of the ROM into the Shadow RAM.
A16	68	I	CPU Address Bus Bit 16 - Used to select between 64K blocks when CPUHLDA is low.
SHDWRAMMAP	69	I	Shadow RAM Map - An active high input that selects the Shadow RAM Map option. Normally tied to VSS or VDD.
XA1-XA5	70-74	I	Peripheral Address Bus Bits 1-5 - Inputs used to decode addresses for Port A and Port B, peripheral control signals for the keyboard controller and the real time clock.
ADDRSEL	75	I	Address Select - This input is a multiplex row/column select for the Memory Address Bus drivers.
–ENAS	76	I	Enable Address Strobe - This active low input is used to enable the address strobe on the real time clock. It will go low the first time –S0 is asserted after a system reset.
Q1	77	I	Goes active during the second phase of a CPU bus cycle following the TS state. It is used by the VL82C202 chip to generate the address strobe for the real time clock.
–XIOW	78	I	Input/Output Write - The active low input indicates an I/O write command. Used to generate selects for the keyboard controller, real time clock, Port A and Port B.
–XIOR	79	I	Input/Output Read - The active low input indicates an I/O read command. Used to generate selects for the 8042, 146818, Port A and Port B.
–PPICS	80	I	Programmable Peripheral Interface Chip Select - An active low input used to generate the chip select for the keyboard coontroller.
REFBIT9	81	I	Refresh Bit 9 - The carry out of the refresh counter. It is used with the Address Buffer to generate a refresh for 1M DRAMs. It is multiplexed out as MA8 when –REFRESH is active.
–XMEMR	82	I	Memory Read - An active low input indicates a memory read command. This pin is used to determine the direction of data on the memory data bus and to clock in parity check results.
RAMSEL1	83	I	RAM Select 1 - This input is used with RAMSEL0 and RAMSEL 2 to designate the system RAM configuration.
RAMSEL0	84	I	RAM Select 0 - This input is used with RAMSEL1 and RAMSEL 2 to designate the system RAM configuration.
VDD	4, 31, 49		System Power: 5 V
VSS	1, 17, 26, 30 40, 52, 58, 64		System Ground

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FUNCTIONAL DESCRIPTION

The VL82C202 Memory Controller provides address buffering for the upper address bits on the system and CPU address buses. It generates chip selects for the four possible RAM banks and the two possible ROM banks. The VL82C202 also contains Port A register bits 0 and 1 and the Port B register. It also generates chip select decodes for the keyboard controller and real time clock.

MEMORY DECODES

The upper address bits A16-A23 and XA16 are used to decode chip selects for all on-board memory. The three wire option inputs RAMSEL2, RAMSEL1, and RAMSEL0 are used to select one of six possible memory configurations. Refer to Figure 1.

RAM SELECTS

The memory mapping options shown in Figure 1 are used to generate the enable signals for the RAS and CAS pulses to the DRAMs. These signals will be active anytime the decode on address bits A16-A23 fall in the ranges shown in the memory maps. The signals are latched by the input signal RAMALE. The latches will be transparent while RAMALE is high and hold the value in the latch while RAMALE is low. The latch clocks will also be forced high when CPUHLDA is active making the latches transparent during all hold acknowledge operations.

When –REFRESH is active address bits A16-A23 are ignored and both RAS0 and RAS1 are forced active (high) while CAS0 and CAS1 are forced inactive (low).

MA8 AND MA9

A16-A23 are also used to generate the four address bits of the DRAM. These address bits are also latched by the combination of RAMALE and CPUHLDA as described for the RAM selects. The four latched address bits are then multiplexed out on MA8 and MA9. MA9 is needed only if a memory mapping option using 1M-bit DRAMs is selected. REFBIT9 is multiplexed out onto MA8 during refresh cycles.

ROM SELECTS

The ROM address space is decoded from A16-A23 and latched by ALE. These latches are also forced transparent when CPUHLDA is active in the same manner as the latches for the RAM chip selects. This latched value is then split into the two signals –LCS0ROM and –LCS1ROM using the A16 or XA16 inputs. If XA16 or A16 is low, –LCS0ROM will go active any time the ROM address space is decoded. If XA16 or A16 is high, –LCS1ROM is decoded. In this configuration –LCS0ROM selects the address space from 0E 0000 to 0E FFFF while –LCS1ROM selects the address space 0F 0000 to 0F FFFF.

The ROM address space is duplicated at FE 0000 to FF FFFF and the chip selects will go active in the same manner as described above in this address space.

UPPER ADDRESS BUFFERS

The VL82C202 provides buffer drive capability to drive the card slots on the signals SA17-SA19.

A17-A19 are latched by ALE and driven onto the SA17-SA19 bus whenever CPUHLDA is low. When CPUHLDA is high and –MASTER is high, the latch is bypassed and A17-A19 is driven directly to SA17-SA19. SA17-SA19 will be left floating when CPUHLDA is high and –MASTER is low.

ADDRESS BIT 20

Address bit 20 is handled differently than the other address bits. The A20 signal will be generated directly from CPUA20 (which should be connected to A20 on the 80286 CPU) if the input A20GATE is high or if Port A, bit 1 is set high. If A20GATE is low and Port A, bit 1 is low, the A20 signal is forced low.

ADDRESS BIT 0

A buffer transceiver between XA0 and SA0 is also provided on the VL82C202. If the input –DMAAEN is high, signal flow is from SA0 to XA0. If –DMAAEN is low, signal flow is from XA0 to SA0.

PORT A

The Port A register at address 92 hex contains two bits, b0 and b1. Bit 0, when set high, causes output SWRST to go high. Bit 1 provides the alternate A20 function and when set high, input CPUA20 is transmitted out as A20. If bit 1 and input A20GATE are both low, then output A20 is forced low.

Both bits are cleared on reset. When this register is read bits 2-7 are always forced low.

PORT B

The Port B register in an AT-compatible design is located on the VL82C202. It can be read or written to with an I/O command to address 61 hex. Port B is used to control the speaker and mask out NMI sources. It can be read to find status of –REFRESH, speaker data, and possible sources of NMI.

I/O DECODES

The VL82C202 provides the chip select signals for the on-board I/O peripherals (keyboard controller and real time clock).

NMI LOGIC

The logic necessary to control the Non-Maskable Interrupt (NMI) signal to the processor is contained in the VL82C202. An NMI can be caused by a parity error from the system board DRAM or if an I/O adapter pulls the input –IOCHCK low. These two possible sources can be individually enabled to cause an NMI by setting the appropriate bits in the Port B register. At power-up time, the NMI signal is masked off. NMI can be masked on by writing to I/O address 070 hex with bit 7 low, or masked off by writing to I/O address 070 hex with bit 7 high.

SHADOW RAM

In PC/AT-type memory systems, the memory space between 0A 0000h and 0F FFFFh is reserved for the graphics display buffer, the I/O adapter ROM and the system board ROM. VLSI's Shadow RAM option allows the system designer to copy these blocks into fast RAM memory for higher performance. The 384K-bytes are partitioned into six 64K blocks for maximum flexibility. When the memory is configured with Shadow RAM the selected blocks of 64K-bytes of RAM co-reside over the 64K-bytes of ROM or graphics buffer.

The Shadow RAM option is controlled by two 6-bit configuration registers and is selected by input pin 69, SHDWRAM-MAP tied high.

The two configuration registers, the Read Enable Register (RER) and the Write Protect Register (WPR), define whether an access to a block is to be treated normally (–LCSROMx and –LMEGCS are generated) or directed to Shadow RAM (F16 and CASx are generated), and if the block is writeable.

The two configuration registers are located at I/O address 09Fh. To prevent spurious access, eight consecutive writes to this address are required to "unlock" the registers. The ninth write places the configuration data in the RER and the tenth places data in the WPR. Both registers are cleared by RESET. A read of this address will access first the RER, then the WPR. See the text below for a complete description of these registers.

As an example of how to implement this feature, assume we want to map the BIOS at 0E 0000h to 0F FFFFh into Shadow Ram, define the blocks from 0A 0000h to 0B FFFFh as on-board RAM and leave blocks 0C xxxxh and 0D xxxxh as they are. First, read and write the entire address space between 0E 0000h and 0F FFFFh. Since the configuration registers are cleared by RESET, all reads are from ROM and all writes go to RAM (refer to Table 1). After the copying is complete with interrupts disabled, write eight times to 09Fh to unlock the configuration registers, then write data 33h (RER) and write again data 30H (WPR) to enable the blocks correctly. Now reads to blocks 0A xxxxh, 0B xxxxh, 0E xxxxh, and 0F xxxxh are from the RAM while accesses to blocks 0C xxxxh and 0D xxxxh are directed to the I/O channel. Writes to blocks 0A xxxxh and 0B xxxxh are allowed and writes to blocks 0E xxxxh and 0F xxxxh do not access the Shadow RAM since the Write Protect bits for these blocks have been set.

ACCESSING THE CONFIGURATION REGISTERS

The Read Enable Register (RER) and Write Protect Register (WPR) are located at I/O address 09Fh. The first –IOR to 09Fh accesses the RER and the next –IOR to the same address accesses the WPR. Additional reads follow this RER then WPR sequence. The bit that selects the next accessed register is cleared by Reset or by any –IOW.

Eight consecutive I/O writes to 09Fh are required to unlock the configuration registers. The ninth I/O write to 09Fh accesses the RER and the tenth the WPR. An internal counter keeps track of the number of I/O writes to address 09Fh. This counter is cleared by an –IOW to any address except 09Fh, by any –IOR or by RESET. It also clears on the tenth consecutive I/O write to this address (i.e., after both registers have been written). These registers are cleared on RESET (except for bits 6 and 7, which are unused and always read out high).

SYSTEM TESTING

The VL82C202 offers a test mode that allows the system designer to three-state all output and I/O pins. Unused memory select options 000 or 100 force this mode.

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TABLE 1. SHADOW RAM

SHDW RAMMAP	–ERAM W	Read Enable Register Bit	Write Protect Register Bit	Address = 0A 0000 - 0F FFFF Address = FE 0000 - FF FFFF F16 (Note 1)	RAS x	CAS x	–LCS ROM X (Note 2)	–LMEG CS	Comments
0	X	X	X	0	0	0	0	0	Shadow Mode Not Selected, Normal Access
1	0	0	0	0	1	1	1	0	Slow Shadow RAM Write
1	0	0	1	0	1	0	1	0	Slow Shadow RAM Write (Protected)
1	0	1	0	1	1	1	1	1	Fast Shadow RAM Write
1	0	1	1	1	1	0	1	1	Fast Shadow RAM Write (Protected)
1	1	0	0	0	1	0	0	0	Normal Read
1	1	0	1	0	1	0	0	0	Normal Read
1	1	1	0	1	1	1	1	1	Fast Shadow RAM Read
1	1	1	1	1	1	1	1	1	Fast Shadow RAM Read

Notes: 1. F16 is always generated by blocks 0E 0000 - 0F FFFF and FE 0000 - FF FFFF.
2. –LCSROMx is active only for blocks 0E 0000 - 0F FFFF and FE 0000 - FE FFFF.

TABLE 2. SHADOW RAM CONFIGURATION REGISTERS

	b7	b6	b5	b4	b3	b2	b1	b0
Read Enable Register	1	1	F	E	D	C	B	A
Write Protect Register	1	1	F	E	D	C	B	A

Selects Block 0A xxxx
Selects Block 0B xxxx
Selects Block 0C xxxx
Selects Block 0D xxxx
Selects Block 0E xxxx, FE xxxx
Selects Block 0F xxxx, FF xxxx

FIGURE 1. SUPPORTED DRAM CONFIGURATIONS AND RAS/CAS GENERATION

MEMORY ADDRESS (64K BLOCKS)

TOTAL DRAM		512K BYTES		1M BYTES		2M BYTES			2M BYTES		4K BYTES		8M BYTES	
DRAM TYPE		256K		256K		256K			1M		1M		1M	
NO. OF DRAMS		18		36		72			18		36		72	
RAMSEL (2, 1, 0)	000	001		010 (1)		011		100	101		110		111	
SHDW RAM MAP	X	0	1	0	1	0	1	X	0	1	0	1	0	1
00-07	TEST MODE	RAS0 CAS0	N/U	RAS0 CAS0	RAS0 CAS0	RAS0 CAS0	RAS0 CAS0	TEST MODE	RAS0 CAS0	RAS0 CAS0	RAS0 CAS0	RAS0 CAS0	RAS0 CAS0	RAS0 CAS0
08-09				RAS1 CAS1	RAS1 CAS1	RAS1 CAS0	RAS1 CAS0							
0A-0D					RAS1* CAS1		RAS1* CAS1			RAS0* CAS0		RAS1* CAS1		RAS1* CAS1
0E-0F				ROM		ROM			ROM		ROM		ROM	
10-13				RAS1 CAS1		RAS1 CAS0	RAS1 CAS0							
14-15														
16-1D						RAS0 CAS1	RAS0 CAS1		RAS0 CAS0		RAS0 CAS0	RAS0 CAS0	RAS0 CAS0	RAS0 CAS0
1E-1F							RAS1 CAS1							
20-23						RAS1 CAS1								
24-25														
26-3F											RAS1 CAS1	RAS1 CAS1	RAS1 CAS0	RAS1 CAS0
40-45														
46-65													RAS0 CAS1	RAS0 CAS1
66-7F														RAS1 CAS1
80-85													RAS1 CAS1	

*See Shadow RAM description.

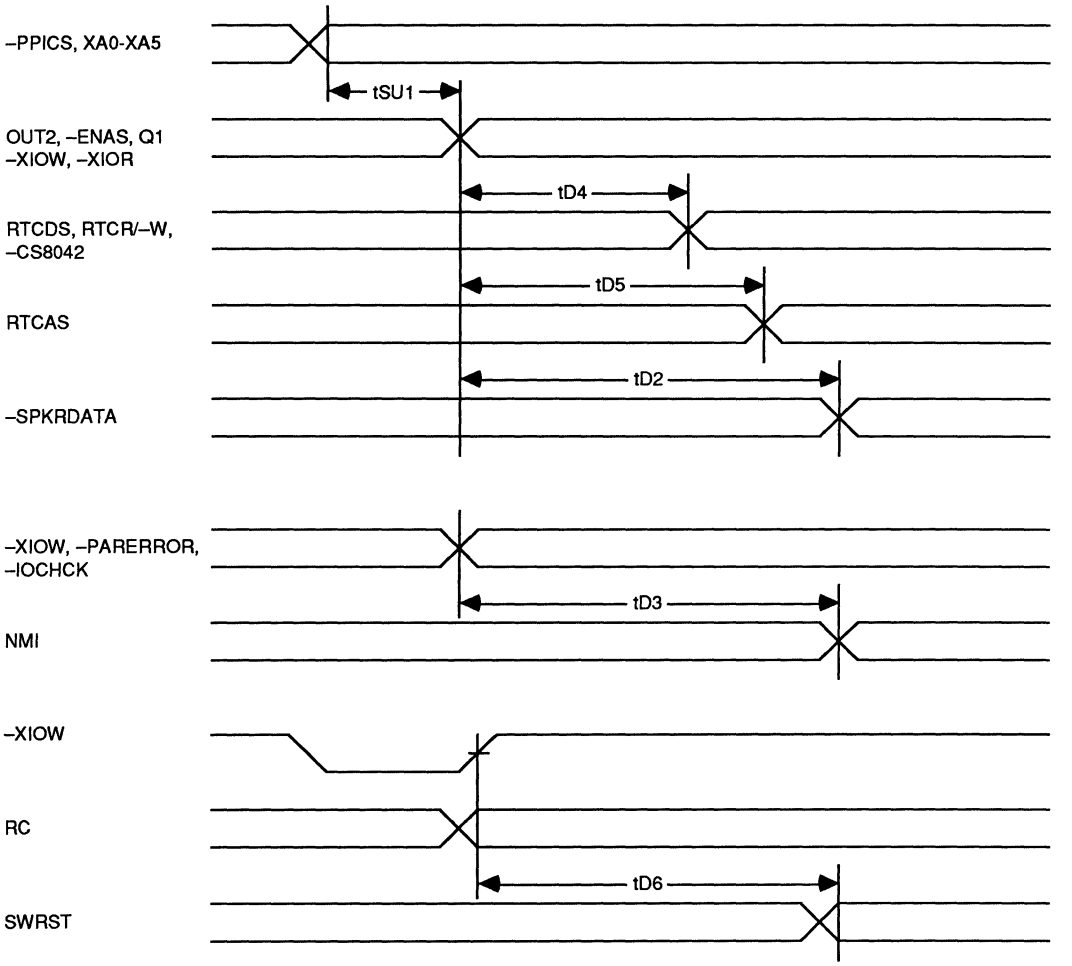
(1) This map is also useable for a 64K-byte map using a combination of 256K and 64K DRAMs.

AC CHARACTERISTICS: TA = QC: 0°C to +70°C, QI: –40°C to +85°C, VDD = 5 V ± 5%, VSS = 0 V

PERIPHERAL CONTROL TIMING

Symbol	Parameter	16 MHz Min	16 MHz Max	20 MHz Min	20 MHz Max	Unit	Condition
tSU1	–PPICS, XA Setup to –XIOW	8		8		ns	
tD2	SPKRDATA Output Delay		40		40	ns	CL = 50 pF
tD3	NMI Output Delay		40		40	ns	CL = 100 pF
tD4	RTCDS, RTCR/–W, –CS8042 Output Delay		30		30	ns	CL = 50 pF
tD5	RTCAS Output Delay		35		35	ns	CL = 50 pF
tD6	SWRST Delay		40		40	ns	CL = 50 pF

PERIPHERAL CONTROL TIMING WAVEFORMS



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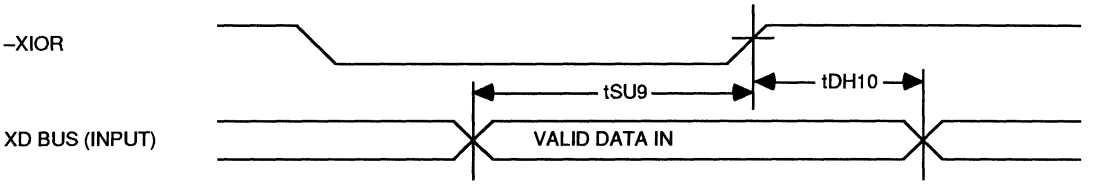
XD BUS TIMING

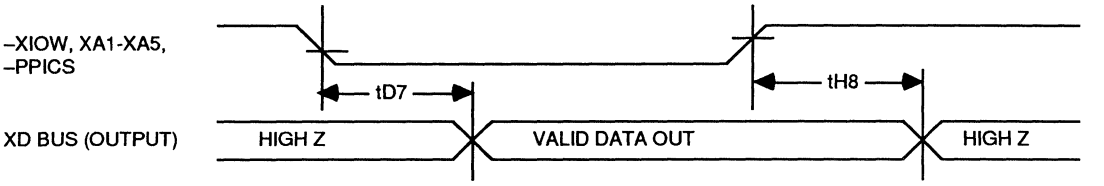
Symbol	Parameter	16 MHz		20 MHz		Unit	Condition
		Min	Max	Min	Max		
tD7	XD Bus Delay		40		40	ns	XD = Output
tH8	XD Bus Hold Time	6		6		ns	XD = Output
tSU9	XD Bus Setup Time	20		20		ns	XD = Input
tH10	XD Bus Hold Time	12		12		ns	XD = Input

XD BUS TIMING WAVEFORMS

Input



Output



ADDRESS CONTROL TIMING

Symbol	Parameter	16 MHz		20 MHz		Unit	Condition
		Min	Max	Min	Max		
tD11	F16 Output Delay		25		21	ns	CL = 50 pF
tD12	CAS0, CAS1 Delay from RAMALE		30		20	ns	CL = 50 pF
tD13	RAS0, RAS1 Delay from RAMALE		18		18	ns	CL = 50 pF
tD14	–LMEGCS Delay from ALE		25		22	ns	CL = 50 pF
tD15	–LCS1ROM, –LCS0ROM Delay from ALE		25		25	ns	CL = 50 pF
tD16	AEN Output Delay		30		30	ns	CL = 150 pF
tD17	CAS Delay from –ERAMW in Shadow Mode		17		13	ns	
tD18	–LCSxROM Delay from –ERAMW		28		28	ns	

Note: RAMSEL0, RAMSEL1, and RAMSEL2 are assumed setup one processor clock before the user generates any memory control signals. If the test mode is not used, these pins are usually strapped to VDD or VSS.

Input SHDWRAMMAP should be tied to VDD or VSS.

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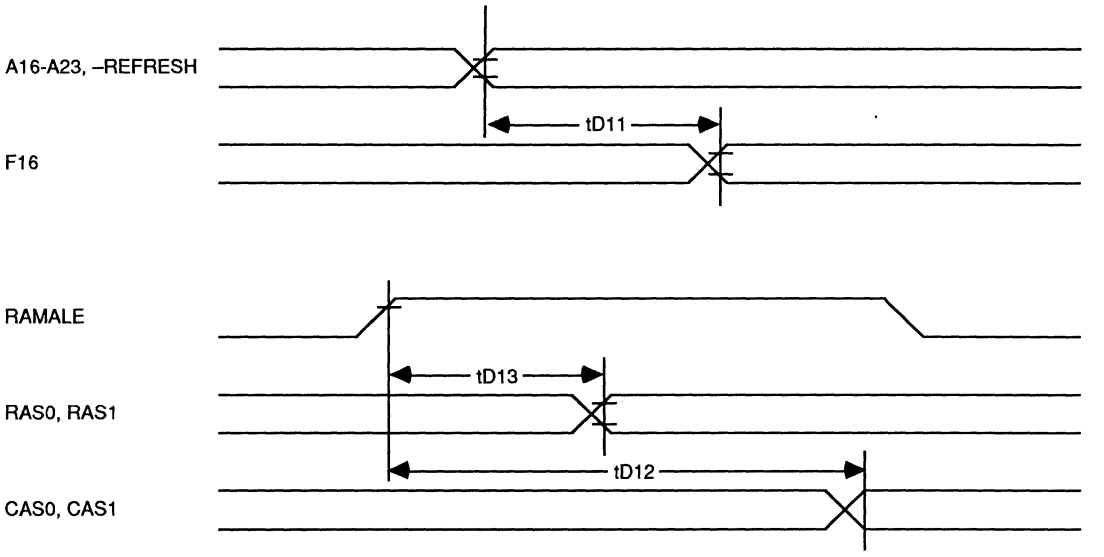
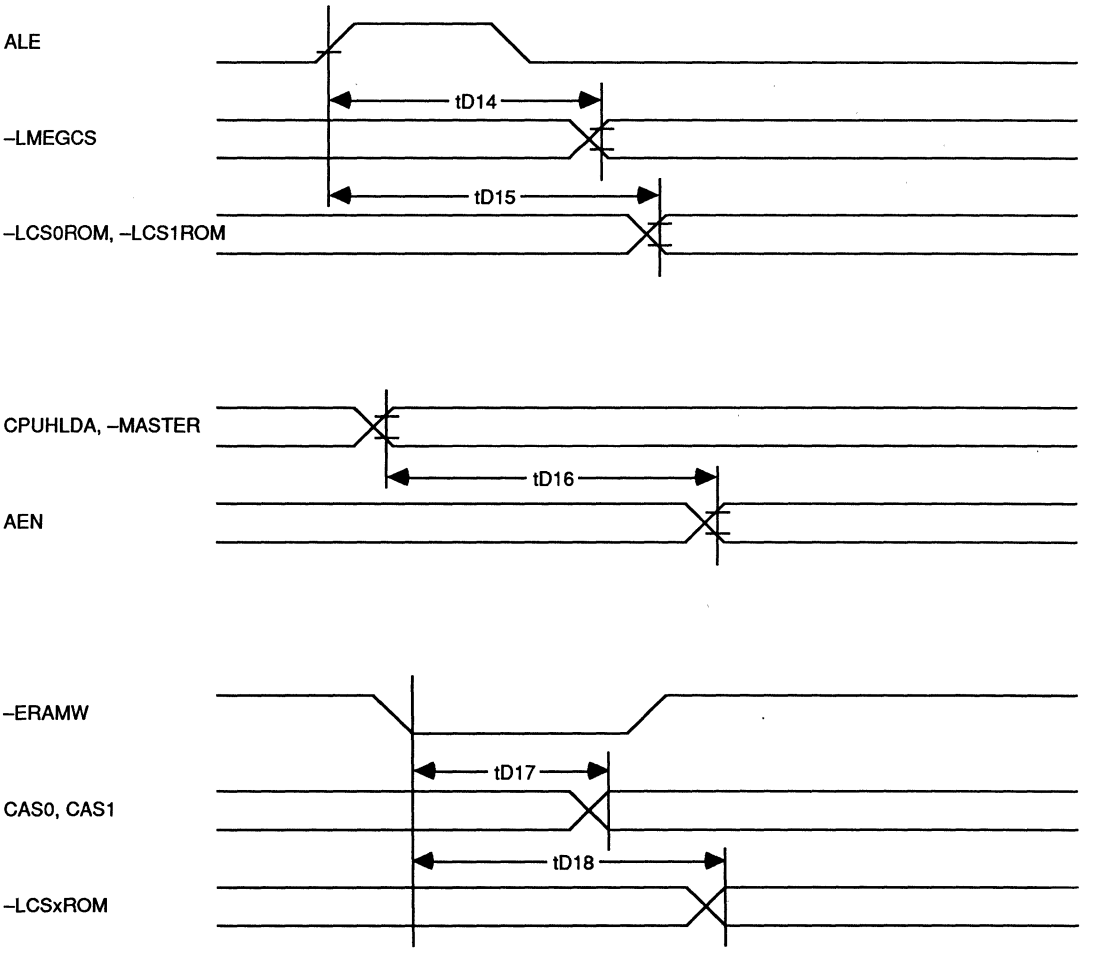
ADDRESS CONTROL TIMING WAVEFORMS



ADDRESS CONTROL TIMING WAVEFORMS (Cont.)

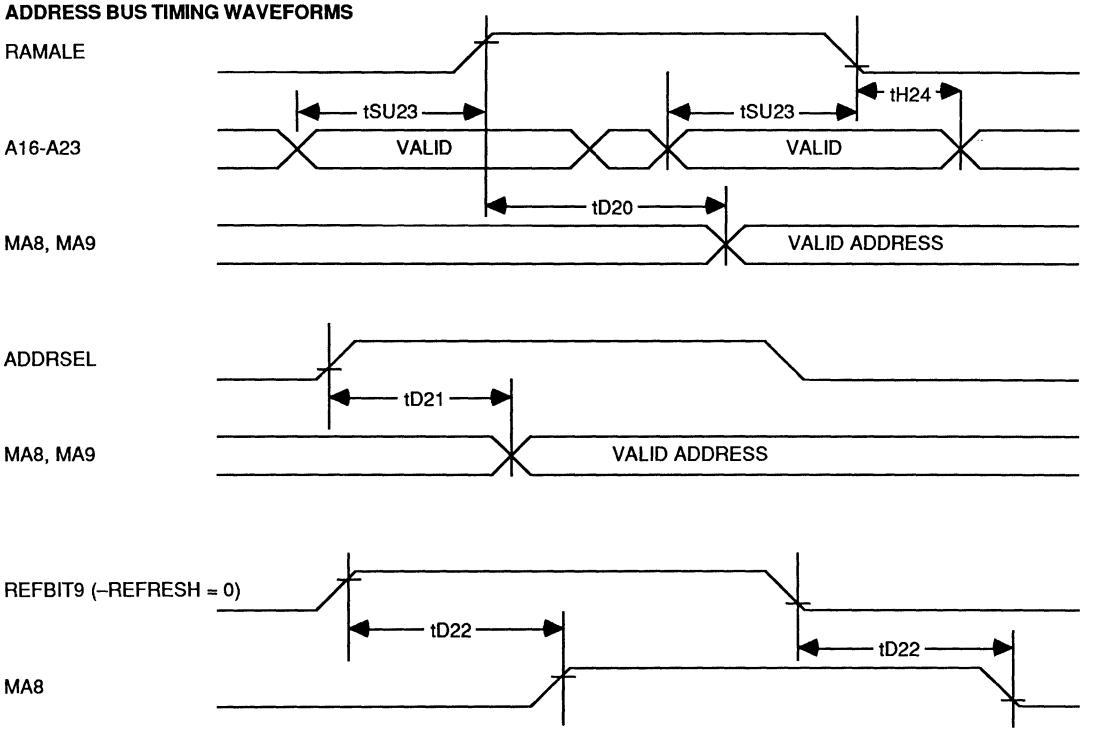


ADDRESS BUS TIMING

Symbol	Parameter	16 MHz Min	16 MHz Max	20 MHz Min	20 MHz Max	Unit	Condition
tD20	MA8, MA9 Delay from RAMALE		22		18	ns	
tD21	MA8, MA9 Delay from ADDRSEL		17		17	ns	Note
tD22	MA8 Delay from REFBIT9		25		25	ns	–REFRESH = 0
tSU23	A16-A23 Setup to ALE, RAMALE	25		25		ns	
tH24	A16-A23 Hold	10		10		ns	
tD25	XA0/SA0 Delay		35		35	ns	CL = 200 pF SA0, CL = 100 pF XA0
tD26	SA17-SA19		40		35	ns	CL = 200 pF SA0, CPUHLDA = 1, –MASTER = 1
tD27	SA17-SA19 Delay from ALE		35		30	ns	CPUHLDA = 0
tD28	A20 Delay		35		30	ns	CL = 50 pF

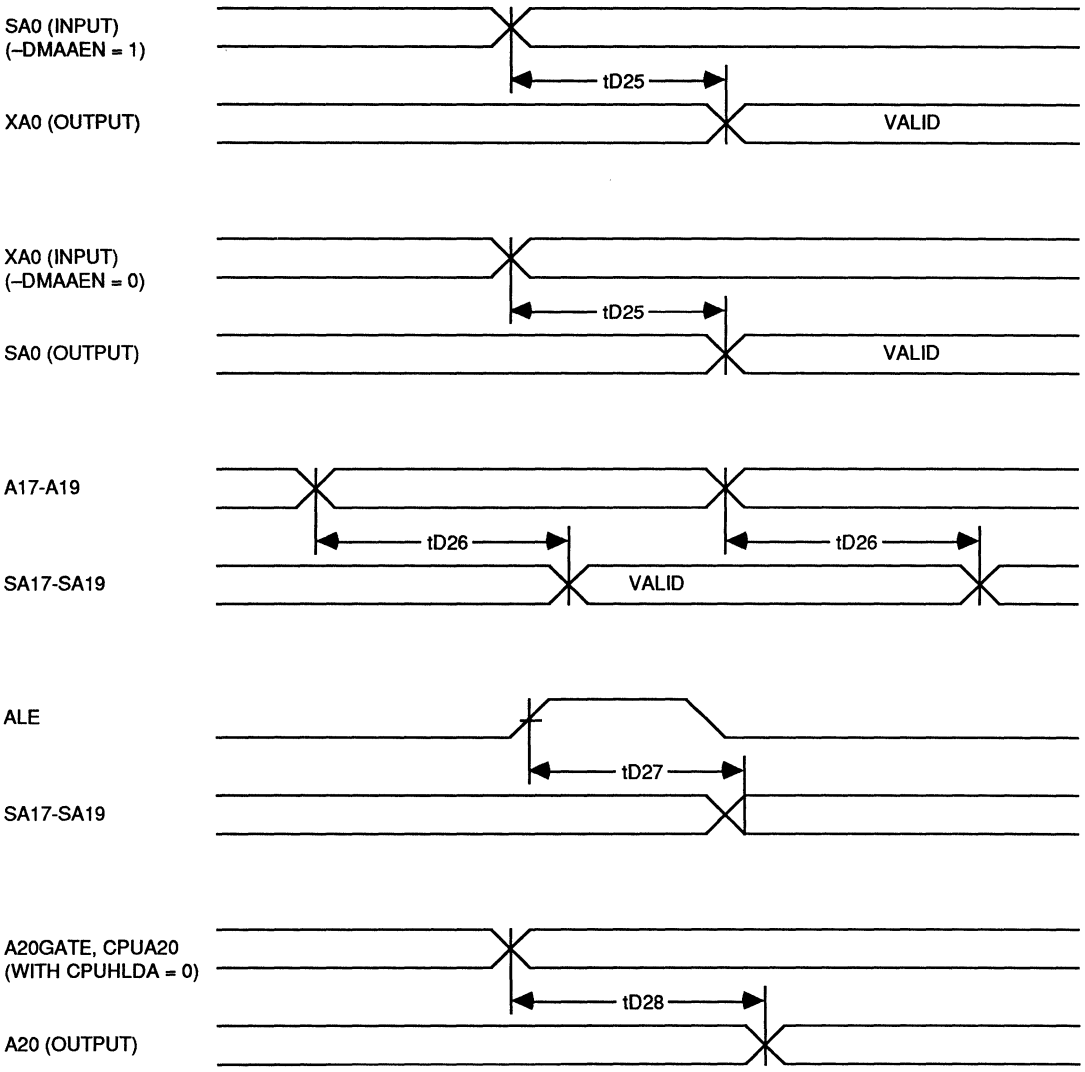
Note: tD21 delay may be derated by a factor of .04 ns/pF for heavier loads.

ADDRESS BUS TIMING WAVEFORMS



Note: tSU23 is specified with respect to the falling edge of RAMALE to guarantee the correct address decodes will be latched in. tSU23 is shown with respect to the rising edge of RAMALE to show time required for address decodes such that propagation delays tD20 and tD13 will be valid. The time does not have to be met with respect to the rising edge for correct functionality.

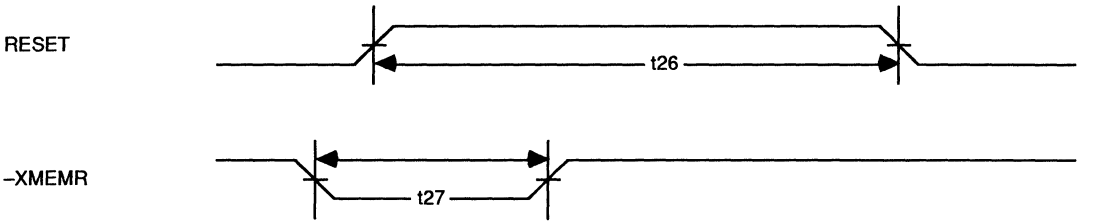
ADDRESS BUS TIMING WAVEFORMS (Cont.)



MISCELLANEOUS INPUT TIMING

Symbol	Parameter	16 MHz		20 MHz		Unit	Condition
		Min	Max	Min	Max		
t26	Min High (Active) Time on RESET	100		100		ns	
t27	Min Low Time for –XMEMR	40		40		ns	

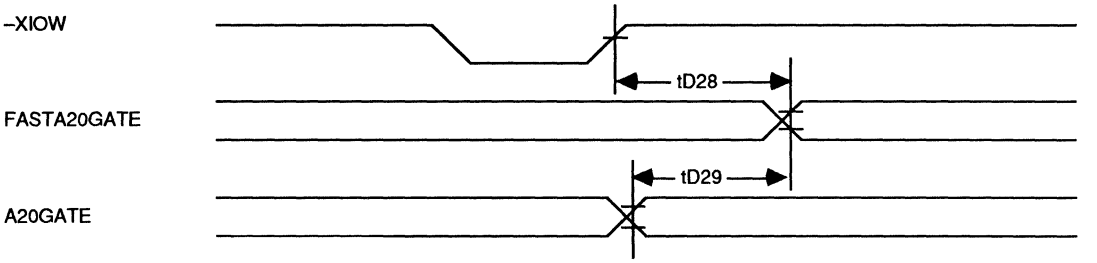
MISCELLANEOUS INPUT TIMING WAVEFORMS



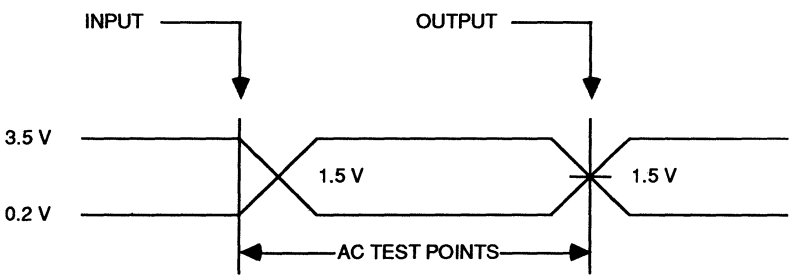
FASTA20GATE TIMING

Symbol	Parameter	16 MHz		20 MHz		Unit	Condition
		Min	Max	Min	Max		
tD28	FASTA20GATE Delay from –XIOW		40		40	ns	I/O Write to Port A, CL = 50 pF
tD29	FASTA20GATE Delay from A20GATE		35		35	ns	CL = 50 pF

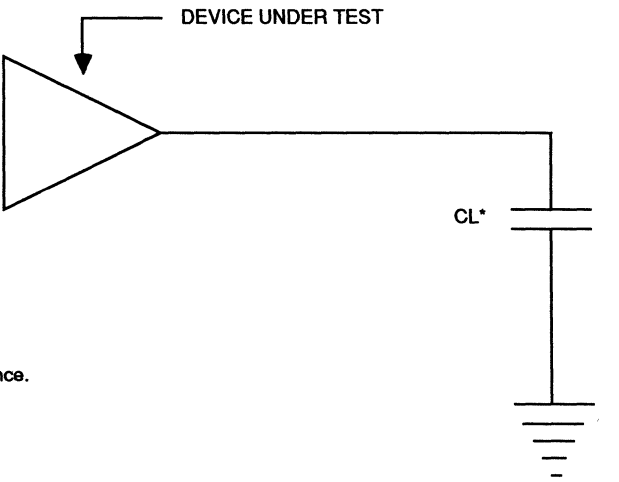
FASTA20GATE TIMING WAVEFORMS



AC TESTING - INPUT, OUTPUT WAVEFORM



AC TESTING - LOAD CIRCUIT



*Includes scope and jig capacitance.

AC TESTING - LOAD VALUES

Test Pin	CL (pF)
27, 29, 50, 54, 55	200
65, 66	150
28, 32-39	100
All Others	50

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	QC = 0°C to +70°C QI = –40°C to +85°C
Storage Temperature	–65°C to +150°C
Supply Voltage to Ground Potential	–0.5 V to +7.0 V
Applied Input Voltage	–0.5 V to +7.0 V
Power Dissipation	500 mW

Stresses above those listed may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: TA = QC: 0°C to +70°C, QI: –40°C, to +85°C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Condition
VOH	Output High Voltage	2.4		V	IOH = –3.3 mA
VOL1	Output Low Voltage		0.45	V	SA0, SA17-SA19, AEN, CL = 200 pF, IOL = 20 mA
VOL2	Output Low Voltage		0.45	V	MA8, MA9, CL = 150 pF, IOL = 8 mA
VOL3	Output Low Voltage		0.45	V	F16, XA0, XD0-XD7, CL = 100 pF, IOL = 8 mA
VOL4	Output Low Voltage		0.45	V	All Other Pins, CL = 50 pF, IOL = 2 mA
VIH	Input High Voltage	3.8	VDD + 0.5	V	ALE, RAMALE
VIL	Input Low Voltage	–0.5	0.6	V	ALE, RAMALE
VIHC	Input High Voltage	2.0	VDD + 0.5	V	All Other Pins
VILC	Input Low Voltage	–0.5	0.8	V	All Other Pins
CO	Output Capacitance		16	pF	
CI	Input Capacitance		8	pF	
CIO	Input/Output Capacitance		16	pF	
ILOL	Three-state Leakage Current	–100	100	µA	
ILI	Input Leakage Current	–10	10	µA	
ICC	Power Supply Current		25	mA	Note

Note: Inputs = VSS or VDD, outputs are not loaded.

NOTES: