# PC/AT-COMPATIBLE SYSTEM CONTROLLER

## FEATURES

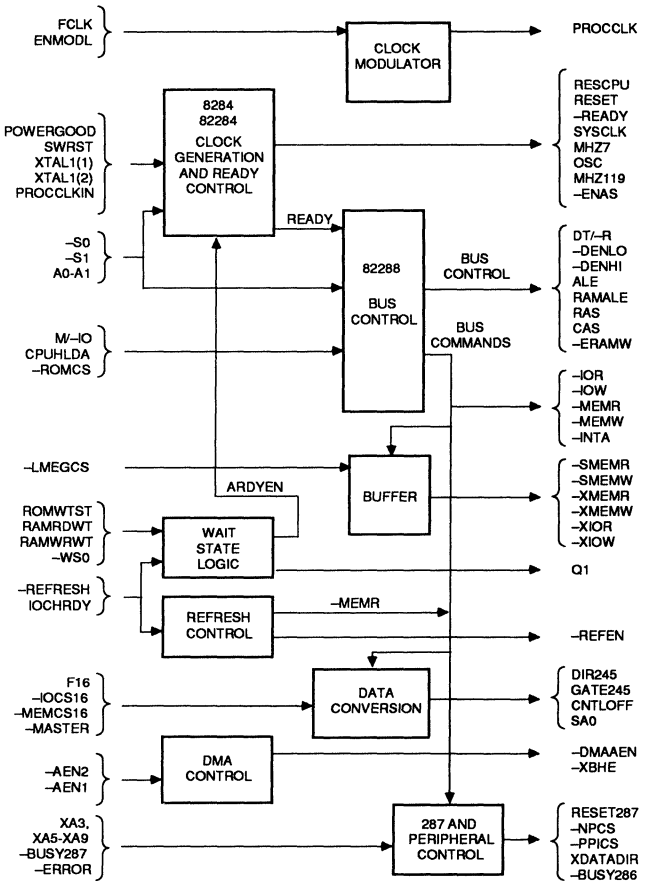
- Fully compatible with IBM PC/AT-type designs
- Replaces 36 integrated circuits on the PC/AT-type board
- Supports 20 MHz system clock
- Device is available as "cores" for user-specific designs
- Sink 24 mA on slot driver outputs
- Designed in CMOS for low power consumption

## DESCRIPTION

The VL82C201 PC/AT-Compatible System Controller replaces an 82C284 Clock Controller and an 82C288 Bus Controller (both are used in '286-based systems), an 82C84A Clock Generator and Driver, two PAL16L8 devices (used for memory decode), and approximately 30 other less complex integrated circuits used as wait state logic. The device accepts a user supplied PROCCLK or generates its own using an internal clock modulation circuit. It also accepts a 14.318 MHz crystal to control the video clock and supplies reset and clock signals to the I/O slots.

The device is manufactured with VLSI's advanced high-performance CMOS process and is available in a JEDEC-standard 84-pin plastic leaded chip carrier (PLCC) package. The VL82C201 is part of the PC/AT-compatible chip sets available from VLSI. Please refer to the Selector Guide in the front of this manual.

## BLOCK DIAGRAM




## ORDER INFORMATION

| Part Number | System Clock Freq. | Package |
|---|---|---|
| VL82C201-16QC<br>VL82C201-16QI | 16 MHz | Plastic Leaded Chip Carrier (PLCC) |
| VL82C201-20QC<br>VL82C201-20QI | 20 MHz | Plastic Leaded Chip Carrier (PLCC) |

**Note:** Operating temperature:
QC = 0°C to +70°C
QI = –40°C to +85°C.

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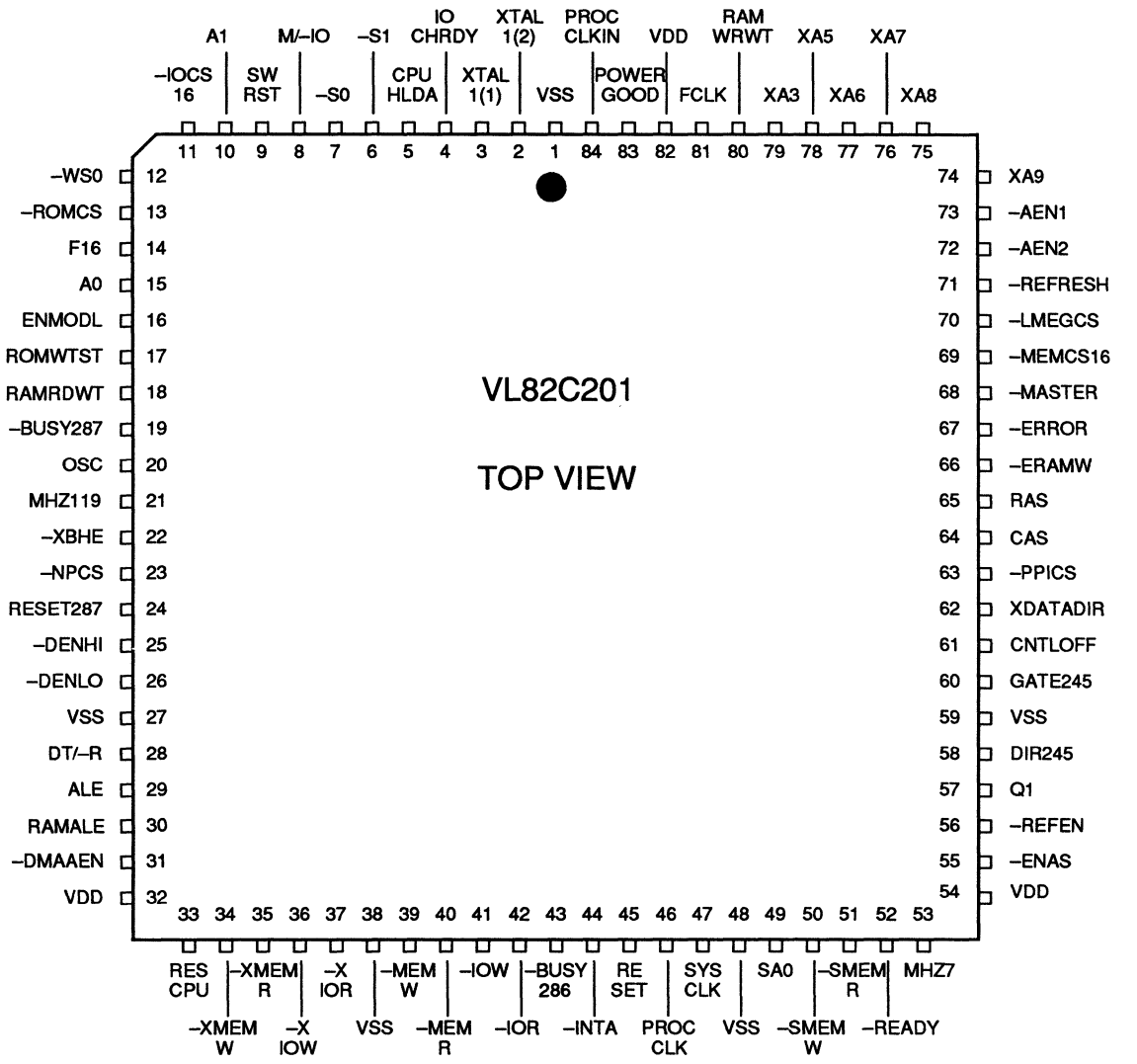
## PIN DIAGRAM


VL82C201
TOP VIEW
11 A1
10 –IOCS 16
9 SW RST
8 M/–IO
7 –S0
6 –S1
5 CPU HLDA
4 IO CHRDY
3 XTAL 1(1)
2 XTAL 1(2)
1 VSS
84 PROC CLKIN
83 POWER GOOD
82 VDD
81 FCLK
80 RAM WRWT
79 XA3
78 XA5
77 XA6
76 XA7
75 XA8
12 –WS0
13 –ROMCS
14 F16
15 A0
16 ENMODL
17 ROMWTST
18 RAMRDWT
19 –BUSY287
20 OSC
21 MHZ119
22 –XBHE
23 –NPCS
24 RESET287
25 –DENHI
26 –DENLO
27 VSS
28 DT/–R
29 ALE
30 RAMALE
31 –DMAAEN
32 VDD
74 XA9
73 –AEN1
72 –AEN2
71 –REFRESH
70 –LMEGCS
69 –MEMCS16
68 –MASTER
67 –ERROR
66 –ERAMW
65 RAS
64 CAS
63 –PPICS
62 XDATADIR
61 CNTLOFF
60 GATE245
59 VSS
58 DIR245
57 Q1
56 –REFEN
55 –ENAS
54 VDD
33 RES CPU
34 –XMEM W
35 –XMEM R
36 –X IOW
37 –X IOR
38 VSS
39 –MEM W
40 –MEM R
41 –IOW
42 –IOR
43 –BUSY 286
44 –INTA
45 RE SET
46 PROC CLK
47 SYS CLK
48 VSS
49 SA0
50 –SMEM W
51 –SMEM R
52 –READY
53 MHZ7

## SIGNAL DESCRIPTIONS

| Signal Name | Pin Number | Signal Type | Signal Description |
|---|---|---|---|
| XTAL1(2) | 2 | O | Crystal 1 Output 2 - A parallel resonant fundamental mode crystal should be attached across XTAL1(1) and XTAL1(2). This is the crystal output. Typical load = 33 pF. |
| XTAL1(1) | 3 | I | Crystal 1 Input 1 - A parallel resonant fundamental mode crystal should be attached across XTAL1(1) and XTAL1(2). This input drives the internal oscillator and determines the frequency of OSC. Typical load = 33 pF. |
| IOCHRDY | 4 | I | I/O Channel Ready - This input is generated by an I/O device. When low, it indicates a not ready condition. This is used to extend memory or I/O accesses by inserting wait states. When high, this signal allows normal completion of a memory or I/O access. |
| CPUHLDA | 5 | I | CPU Bus Hold - This input indicates ownership of the local CPU bus. When high, this signal indicates that the CPU has three-stated its bus drivers in response to a hold request. When low, it indicates that the CPU bus drivers are active. |
| –S1 | 6 | I | Status 1 - An active low input/pull-up from the CPU in combination with –S0 and M/–IO determine which type of bus cycle to initiate. –S1 going active indicates a read cycle unless –S0 also goes active. Both status inputs active indicate an interrupt acknowledge cycle or halt/shutdown operation. |
| –S0 | 7 | I | Status 0 - An active low input/pull-up from the CPU in combination with –S1 and M/–IO determine which type of bus cycle to initiate. –S0 going active indicates a write cycle unless –S1 also goes active. Both status inputs active indicate an interrupt acknowledge cycle or a halt/shutdown operation. |
| M/–IO | 8 | I | Memory or I/O Select - This input indicates the type of bus cycle to be performed. If high, a memory cycle or halt/shutdown cycle is started. If low, then an I/O cycle or an interrupt acknowledge cycle will be initiated. |
| SWRST | 9 | I | This active high input signal will force a CPU reset when a low to high transition is detected. |
| A1 | 10 | I | CPU Address Bus Bit 1 - This input is used to determine when to initiate a shutdown operation. A shutdown will be started when A1 is low, M/–IO is high, and both –S0 and –S1 go low. |
| –IOCS16 | 11 | I | I/O Chip Select 16 - This active low input is generated by an I/O device for a 16-bit data bus access. This signal is used to determine the number of wait states and whether data conversion is necessary for I/O accesses. |
| –WS0 | 12 | I | Wait State 0 - This active low input signal should have an external pull-up. A peripheral device can pull this signal low to force a zero wait state cycle. |
| –ROMCS | 13 | I | ROM Chip Select - This active low input is a signal generated from –LCS0ROM and –LCS1ROM and is used to indicate a ROM memory access. |
| F16 | 14 | I | This input indicates an on-board memory access. It is used along with –ROMCS to determine whether a memory access is to ROM, on-board RAM or off-board RAM. It is also used to inhibit a command delay for memory accesses. |
| A0 | 15 | I | CPU Address Bus Bit 0 - This input is used to generate enable signals for the data bus transceivers. |
| ENMODL | 16 | I | Enable Modulation - Is an input used to control the clock modulator on the VL82C201. When this signal is high, normal clock modulation can occur. When ENMODL is low, clock modulation is disabled and PROCCLK is forced to 1/4 the frequency of FCLK. |

## SIGNAL DESCRIPTIONS (Cont.)

| Signal Name | Pin Number | Signal Type | Signal Description |
|---|---|---|---|
| ROMWTST | 17 | I | ROM Wait State - This input is used to select the desired number of ROM access wait states. ROMWTST low indicates two waits while ROMWTST high indicates three wait states. |
| RAMRDWT | 18 | I | RAM Read Wait State - This input indicates the number of wait states to be used for on-board RAM read cycles. A high indicates one wait state reads while a low indicates zero wait state reads. RAMRDWT also controls the timing on RAS and CAS during memory read cycles. |
| –BUSY287 | 19 | I | Busy - A busy status input that is asserted by the 80287 to indicate that it is currently executing a command. |
| OSC | 20 | O | This is the buffered output of the XTAL1 oscillator. |
| MHZ119 | 21 | O | This output is the OSC output clock divided by 12. |
| –XBHE | 22 | I/O | Transfer Byte High Enable - This active low I/O is used to enable –DENHI and determine when a 16-bit to 8-bit data conversion is needed. –XBHE is driven as an output during all DMA cycles. It is forced low if –AEN2 is active and it is driven as the inversion of SA0 if –AEN1 is active. |
| –NPCS | 23 | O | Numerical Processor Chip Select - This active low output is the chip select for the 80287 numerical processor. |
| RESET287 | 24 | O | Reset 287 - This active high output is used to reset the 80287 numerical processor. |
| –DENHI | 25 | O | Data Bus Enable High - This active low output is used to enable the data bus transceiver on the high byte of the data bus. |
| –DENLO | 26 | O | Data Bus Enable Low - This active low output is used to enable the data bus transceiver on the low byte of the data bus. |
| DT/–R | 28 | O | Data Transmit/Receive - An output that determines the data direction to and from the local data bus. A high indicates a write bus cycle and a low indicates a read bus cycle. DT/–R is high when no bus cycle is active. –DENLO and –DENHI are always inactive when DT/–R changes state. |
| ALE | 29 | O | Address Latch Enable - A positive edge output that controls the address latches which hold the address during a bus cycle. ALE is not issued for a halt bus cycle. |
| RAMALE | 30 | O | RAMALE is used to latch RAM address buffers. It is forced high at the end of any bus cycle. This allows the address for the next bus cycle to be passed to the system memory sooner than the ALE signal. RAMALE will go back low at the end of the status cycle for any bus cycle to latch the memory address until the end of the bus cycle. |
| –DMAAEN | 31 | O | DMA Address Enable - An active low output that is active whenever an I/O device is making a DMA access to the system memory. It will go low anytime –AEN1 or –AEN2 go low. |
| RESCPU | 33 | O | Reset CPU - This is the active high output system reset for the CPU. It is generated from POWERGOOD, SWRST or when a shut down status is generated by the CPU. |
| –XMEMW | 34 | I/O | Peripheral Bus Memory Write - An active low I/O that is the memory write command to and from the peripheral bus. This pin is configured as an output when –DMAAEN is high and an input when –DMAAEN is low. |
| –XMEMR | 35 | I/O | Peripheral Bus Memory Read - An active low I/O that is the memory read command to and from the peripheral bus. This pin is configured as an output when –DMAAEN is high and an input when –DMAAEN is low. |

## SIGNAL DESCRIPTIONS (Cont.)

| Signal Name | Pin Number | Signal Type | Signal Description |
|---|---|---|---|
| –XIOW | 36 | I/O | Peripheral Bus Input/Output Write - This active low I/O is the read command to and from the peripheral bus. This pin is configured as an output when –DMAAEN is high and an input when –DMAAEN is low. |
| –XIOR | 37 | I/O | Peripheral Bus Input/Output Read - This active low I/O is the read command to and from the peripheral bus. This pin is configured as an output when –DMAAEN is high and an input when –DMAAEN is low. |
| –MEMW | 39 | I/O | Memory Write - This active low I/O is the memory write command from the bus controller portion of the chip. It will be three-stated when CPUHLDA is asserted and CNTLOFF is inactive. |
| –MEMR | 40 | I/O | Memory Read - This active low I/O is the memory read command from the bus controller portion of the chip. It will be three-stated when CPUHLDA is asserted and CNTLOFF is inactive. –MEMR is also active during a refresh cycle. |
| –IOW | 41 | I/O | Input/Output Write - This is the active low I/O write command from the bus controller portion of the chip. It will be three-stated when CPUHLDA is asserted and CNTLOFF is inactive. |
| –IOR | 42 | I/O | Input/Output Read - This is the active low I/O read command from the bus controller portion of the chip. It will be three-stated when CPUHLDA is asserted and CNTLOFF is inactive. |
| –BUSY286 | 43 | O | Processor Extension Busy - This output goes to the –BUSY input of the 80286. If pulled low, this signal stops the 80286 program execution on all WAIT and some ESC instructions until it returns inactive (high). |
| –INTA | 44 | O | Interrupt Acknowledge - This active low output that is three-stated is the interrupt acknowledge command from the bus controller portion of the chip. It will be three-stated when CPUHLDA is asserted and CNTLOFF is inactive. |
| RESET | 45 | O | Reset - This active high output signal is the system reset generated from a POWERGOOD. It is synchronized to PROCCLKIN. |
| PROCCLK | 46 | O | Processor Clock - This is the output of the on-board clock modulator. When the clock modulator is enabled the frequency of PROCCLK will be FCLK/2 except for I/O cycles, off-board memory cycles, and DMA cycles. The frequency of PROCCLK will switch to FCLK/4 during those cycles. |
| SYSCLK | 47 | O | System Clock - This output is the main system clock. It is equal to half the PROCCLKIN frequency and is synchronized to the processor's T-states. |
| SA0 | 49 | I/O | System Address Bus Bit 0 - SA0 is driven as an output anytime CPUHLDA is low, and will be an input at all other times. It is used internally to control the data bus enable signals and to determine the state of –XBHE during 8-bit DMA cycles. |
| –SMEMW | 50 | O | Memory Write - An active low three-stated output that is the memory write command to the expansion bus. Drives when –LMEGCS is low. |
| –SMEMR | 51 | O | Memory Read - An active low three-stated output that is the memory read command to the expansion bus. Drives when –LMEGCS is low. |
| –READY | 52 | O | Ready - When active, indicates that the current bus cycle is to be completed. –READY is an open drain output requiring an external pull-up resistor. |
| MHZ7 | 53 | O | This output is the OSC output divided by 2. It is generated to provide a fixed clock frequency for the keyboard controller and 80287 coprocessor. |

## SIGNAL DESCRIPTIONS (Cont.)

| Signal Name | Pin Number | Signal Type | Signal Description |
|---|---|---|---|
| –ENAS | 55 | O | Enable Address Strobe - This active low output is used to enable the address strobe on the real time clock device. It will go low the first time –S0 is asserted after a system reset. |
| –REFEN | 56 | O | Refresh Enable - An active low output. It will be asserted when a refresh cycle is needed for the DRAMs. It is used to clock a refresh counter which provides addresses during the refresh cycle. |
| Q1 | 57 | | This active high output will go active during the second phase of a CPU bus cycle following the Ts state. |
| DIR245 | 58 | O | Direction 245 - This output determines the direction of the data bus transceiver which does conversions from high to low byte or low to high byte for 8-bit peripherals. |
| GATE245 | 60 | O | Gate 245 - This output enables the data bus transceiver which does conversions from high to low byte or low to high byte for 8-bit peripherals. |
| CNTLOFF | 61 | O | Control Off - This output is used to latch the lower byte data bus during high byte to low byte conversions. |
| XDATADIR | 62 | O | Transfer Data Direction - This output controls the direction of data flow through the transceiver between the X data bus and the lower byte of the S data bus. A high indicates data flow from the S bus to the X bus. A low indicates data flow from the X bus to the S bus. |
| –PPICS | 63 | O | Programmable Peripheral Interface Chip Select - This active low output is a decode of the XA bus. The decode is for address space 060 to 09F. –PPICS can only go active if CPUHLDA is low or –MASTER is low. |
| CAS | 64 | O | This is the output used to control the timing of the CAS signal to the DRAMs. CAS will go active (high) one clock cycle after RAS if a zero wait state cycle is selected, or 1 1/2 clock cycles if a one wait state cycle is selected. CAS will go back low at the end of the bus cycle. |
| RAS | 65 | O | This is the output used to control the timing of the row address strobe signal to the DRAMs. RAS will go high during the second phase of any memory status cycle. It will go back low two clock cycles later if a zero wait state cycle is selected or three clocks later if a one wait state cycle is selected. |
| –ERAMW | 66 | O | Early RAM Write - It is used to get an early write enable signal to the DRAMs to support zero wait state write cycles. It will go low during the second phase of any memory write status cycle. –ERAMW returns high at the end of the bus cycle. |
| –ERROR | 67 | I | Error - An error status input from the 80287. This reflects the ES bit of the 80287 status word and indicates that an unmasked error condition exists. |
| –MASTER | 68 | I | Master - This active low input is asserted by devices on the expansion bus to get control of the bus. |
| –MEMCS16 | 69 | | Memory Chip Select 16 - A low on this pin indicates that the off-board memory is 16-bits wide. |
| –LMEGCS | 70 | I | Lower Megabyte Chip Select - This input indicates that the lower memory address space (0-1 megabyte) is selected. When low, it enables the three-state drivers on –SMEMR and –SMEMW. |
| –REFRESH | 71 | I | Refresh - This active low input is used to initiate a refresh cycle for the dynamic RAMs. |

## SIGNAL DESCRIPTIONS (Cont.)

| Signal Name | Pin Number | Signal Type | Signal Description |
|---|---|---|---|
| –AEN2 | 72 | I | Address Enable 2 - This active low input is from the DMA controllers and is used to generate –DMAAEN, control –XBHE, and disable the clock modulator. |
| –AEN1 | 73 | I | Address Enable 1 - This active low input is from the DMA controllers and is used to generate –DMAAEN, control –XBHE, and disable the clock modulator. |
| XA5-XA9 | 78-74 | I | Peripheral Address Bus Bits 5-9 - These inputs are used to decode chip select and reset signals for the coprocessor. |
| XA3 | 79 | I | Peripheral Address Bus Bit 3 - This input is used in control of the coprocessor reset and chip select signals. |
| RAMWRWT | 80 | I | RAM Write Wait State - Indicates the number of wait states to be used for on-board RAM write cycles. A high indicates one wait state writes while a low indicates zero wait state writes. RAMWRWT also controls the timing on RAS and CAS during memory write cycles. |
| FCLK | 81 | I | This is the fast clock input to the clock modulator circuit. It should be driven from an external crystal oscillator at twice the frequency of the desired PROCCLK output. |
| POWERGOOD | 83 | I | System Power-on Reset - This input signal indicates that power to the board is stable. A Schmitt-trigger input is used so the input can be connected directly to an RC network. |
| PROCCLKIN | 84 | I | This is the main clock input to the VL82C201 and should be connected to the signal that drives the 80286 CLK pin. It can be connected to the PROCCLK output (Pin 46) if the internal clock modulator is used or can be connected to an externally generated clock. |
| VDD | 32, 54, 82 | | System Power: 5 V |
| VSS | 1, 27, 38, 48, 59 | | System Ground |

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## FUNCTIONAL DESCRIPTION

The VL82C201 chip generates all the major clocks for an AT-compatible system design along with the command and control signals for both the system and peripheral buses. It interfaces with the CPU to determine the type of bus cycle to execute and generates the –READY signal to indicate that the current bus cycle can be terminated. It also contains logic to make conversions between 16-bit and 8-bit data accesses. Finally, it generates some of the control signals necessary for the 80287 Numerical Processor.

### CLOCK GENERATION

The VL82C201 contains a clock modulator to control the processor clock signal and an oscillator to generate the OSC, MHZ7 and MHZ119 signals.

The oscillator is designed to use an external parallel resonant fundamental mode crystal. A 14.318 MHz crystal should be used to maintain compatibility and connected as shown in Figure 1. The variable capacitor is optional. It is used to make slight adjustments to the output frequency. The OSC output is generated directly from this oscillator for the system bus. The MHZ7 output is the oscillator frequency divided by 2 and can be used to drive the 8042 keyboard controller. The MHZ119 output is the oscillator frequency divided by 12 and is used by the Peripheral Controller chip.

The clock modulator portion of the VL82C201 is designed to gracefully switch the speed of the processor clock based on which type of bus cycle is going to be performed. The FCLK input to the modulator should be driven from an external crystal oscillator at a frequency that is two times the desired PROCCLK frequency. The clock modulator can be disabled by driving the input signal ENMODL low. When the clock modulator is disabled the PROCCLK output will be 1/4 the frequency of the FCLK input.

The clock modulator circuit uses the CPU status signals –S0, –S1, and M/–IO along with the signal F16 from the Memory Controller chip to determine which type of bus cycle is needed. Normally the PROCCLK output will be running at 1/2 the frequency of FCLK. When the processor signals an I/O

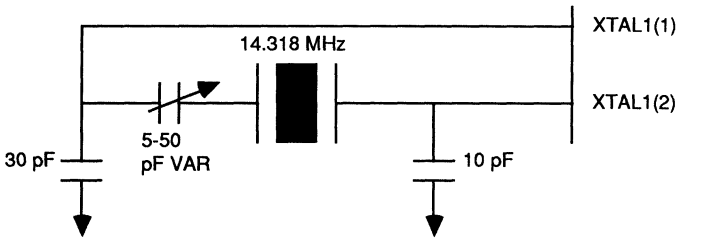
cycle, INTA cycle or off-board memory cycle the modulator will switch the processor clock to 1/4 the frequency of FCLK. The transition is made such that during the second phase of the status cycle PROCCLK will be three FCLK cycles long and all subsequent PROCCLK cycles will be four FCLK cycles long. If the bus cycle is an off-board memory access, the clock modulator will sample –READY to determine when to return PROCCLK to 1/2 the frequency of FCLK. If the bus cycle is an I/O access, the clock modulator will remain at the slow rate until a memory cycle occurs. The clock modulator will then speed up when it samples –READY at the end of the memory cycle.

The inputs –AEN1 and –AEN2 are also sampled by the clock modulator and PROCCLK is slowed to FLCK/4 anytime either of these signals are active.

To reduce clock skew and increase flexibility for the user the PROCCLKIN input is provided. This input should be connected to the same signal that is used to drive the CLK input of the processor. This guarantees that the VL82C201 is referenced to the same clock as the processor with no internal skews. The user can connect this input to the PROCCLK output if the clock modulator is to be used. PROCCLKIN can also be driven from a user supplied source if the clock modulator is not needed.

The SYSCLK output is derived from the PROCCLKIN input and is 1/2 the frequency of PROCCLKIN. SYSCLK is held low during reset and will not begin running until the first bus cycle is initiated by the CPU. It will then make its first low to high transition on the falling edge of PROCCLKIN during the start of the first TC cycle (see timing waveforms). This synchronization is done to ensure that the system clock is synchronized with the 80286 internal system clock.

**FIGURE 1. OSCILLATOR CIRCUIT**




### RESET AND READY CONTROL

The 82284 megacell along with some support logic is used to control the system reset signals and –READY signal for the CPU. Two basic reset signals are generated for the system.

RESET is the system reset out of the 82284 megacell and is synchronized to PROCCLK. It is generated from the POWERGOOD input signal. The POWERGOOD pin has a Schmitt-trigger input so that an RC network can be used to generate the reset signals. RESCPU, the other reset output, is connected to the input on the 80286 processor. RESCPU will be active anytime RESET is active. It can also be generated from two other possible sources. The first is the SWRST input from the Memory Controller chip. A low to high transition is detected on this pin. When this occurs, RESCPU will go active after a minimum delay of 6.72 microseconds. RESCPU will also be generated if a shutdown command is issued from the CPU. In either case, the RESCPU output will pulse high for 16 PROCCLKIN cycles.

The –READY output is synchronized and controlled by the 82284 megacell. –READY is an open drain output connected directly to the CPU and requires an external pull-up resistor. A resistor value of 330 Ω is recommended. Bus cycle length is controlled by the –READY output. Bus cycles are lengthened and shortened internally by the VL82C201 depending on the type of bus cycle being executed. The length of a bus cycle can be shortened externally by pulling the –WS0 input low or lengthened by pulling the IOCHRDY input low. If IOCHRDY is pulled low the bus cycle will not be terminated until IOCHRDY is returned high.

### COMMAND AND BUS CONTROL

The VL82C201 contains an 82288 bus controller megacell to generate all the bus command and control signals. The 82288 megacell generates the –MEMR, –MEMW, –IOR, and –IOW command signals and the DT/–R control signal.

The DEN output from the megacell is split into –DENLO and –DENHI for enables on the upper and lower bytes of the data bus. Internal circuitry is used to insert one PROCCLK cycle of command delay for all I/O cycles and off-board 8-bit memory cycles. Refer to the 82288 data sheet for complete operation of the 82288 megacell.

### OPERATING MODES

The VL82C201 operates in four basic modes. First, and most common, is the CPU mode. This mode is active any time the input CPUHLDA is low. While in CPU mode the VL82C201 will drive both the CMD (–MEMR, –MEMW, –IOR, –IOW) bus and XCMD (–XMEMR, –XMEMW, –XIOR, –XIOW) bus. While in CPU mode, the outputs –MEMR, –MEMW, –SMEMR, and –SMEMW are disabled from going low for on-board memory accesses. They will go low for off-board memory cycles only. The outputs –XMEMR and –XMEMW will still go active for any memory cycle.

The other modes can only be active when CPUHLDA is high. Then the VL82C201 can be in DMA mode, –MASTER mode, or REFRESH mode. If the inputs –AEN1 or –AEN2 are active, the VL82C201 is in DMA mode and the CMD bus is driven from the inputs on the XCMD bus. If the –MASTER input is active, the VL82C201 is in –MASTER mode and the XCMD bus is driven from the inputs on the CMD bus. When the –REFRESH mode is active the –MEMR output will be driven to generate the refresh for the DRAMs but –MEMW, –IOR, and –IOW will be in a high impedance state. The XCMD pins will be configured as outputs driving whatever value is on the CMD pins.

**SYSTEM BOARD MEMORY CONTROL**

Timing control for the system board memory is controlled by four signals: RAMALE, RAS, CAS, and –ERAMW.

RAMALE is used by both the Memory Controller and Address Buffer chips to latch in current address values for generating address and chip select signals for the DRAMs. The RAMALE signal is forced high during reset to pass through the first address from the CPU. At the end of the first status cycle RAMALE will go low and will remain low until –READY is sampled low. After the first memory access RAMALE will always go high at the end of any bus cycle, when –READY is sampled low. RAMALE will go low latching in the current address at the end of any status cycle. This configuration will leave the RAMALE signal high during CPUHLDA cycles to allow addresses and chip select decodes to pass directly to the DRAMs for DMA or –MASTER accesses.

The RAS signal is used to generate the timing control for the DRAMs. It is an active high signal and should be gated with the RAS0 and RAS1 chip select signals out of the Memory Controller chip to generate the RAS signals to the DRAMs. The timing of RAS is controlled by the RAMWRWT, RAMRDWT, and CPUHLDA inputs.

The VL82C201 samples RAMRDWT during memory read cycles and RAMWRWT during memory write cycles to determine whether the cycle should be a zero or one wait state access. A low on these inputs selects zero wait states, while a high will select one wait state. Whenever CPUHLDA is low (inactive) RAS will always go active during the second phase of any memory access status cycle. If the current memory access should be a zero wait state cycle, RAS will return low two PROCCLKIN cycles later. For a one wait state access, RAS will return low three PROCCLKIN cycles later. This is done to generate timing that will meet specifications for the slower DRAMs typically used in one wait state designs. When CPUHLDA is high, the memory control logic samples the inputs on –XMEMR and –XMEMW for DMA cycles, or –MEMR and –MEMW for –MASTER cycles. RAS will go high on the first falling edge of PROCCLKIN when any memory read or write command is sampled active. RAS will return low two or three PROCCLKIN cycles later depending on the states of RAMRDWT and RAMWRWT as described above for the CPU accesses.

The CAS signal is also used to generate timing control for the DRAMs. It is an active high signal and should be gated with CAS0 and CAS1 chip select signals out of the Memory Controller chip to generate the CAS signals to the DRAMs. The timing of CAS is controlled by the RAMWRWT and RAMRDWT inputs.

RAMRDWT and RAMWRWT function the same as described above for the RAS signal to determine whether the current memory access should be zero or one wait states. For a zero wait state access CAS will go active one PROCCLKIN clock cycle after RAS goes active. During a one wait state access CAS will go active 1 1/2 PROCCLKIN clock cycles after RAS goes active. This is done to allow more row address hold time for the slower DRAMs that can be used in a one wait state system. CAS goes inactive (low) at the same time for both zero and one wait state accesses. When CPUHLDA is low, CAS will return inactive at the end of the bus cycle when –READY is sampled low. When CPUHLDA is high, CAS will return inactive on the falling edge of the first PROCCLKIN cycle when all the memory read and write commands are sampled inactive.

–ERAMW is an early write signal for the DRAMs to make sure the write signal is present before CAS. It will go low during the second phase of any memory write status cycle. –ERAMW returns high at the end of the bus cycle.

Note: Although RAMRDWT and RAMWRWT can be changed dynamically for each memory cycle, care must be taken to never allow RAMRDWT to be high and RAMWRWT to be low at the same time for more than 60 ns. This results in zero wait state write cycles and one wait state read cycles. This was determined to be an unrealistic operating mode and is used to put the VL82C201 into a test mode that will disrupt normal system operation.

**WAIT STATE LOGIC**

Wait states can be controlled from a number of different sources within the VL82C201. It is internally programmed to generate the wait states shown in Table 1 based on the appropriate input signals.

Any of these programmed values can be overridden by the inputs IOCHRDY and –WS0. IOCHRDY can be used to extend any bus cycle. When IOCHRDY is pulled low the current bus cycle will be maintained until it is returned high. A low on –WS0 will terminate the current bus cycle as soon as it is recognized by the VL82C201. These inputs need only be pulled low to modify the values shown in Table 1. IOCHRDY and –WS0 are mutually exclusive and only one of them should be pulled low within a given bus cycle. Refer to the timing diagrams for setup and hold requirements.

**REFRESH CONTROL**

The VL82C201 contains circuitry to control a refresh cycle in an AT-compatible design. When the input –REFRESH is pulled low, the VL82C201 will issue –REFEN to clock the refresh counter and enable the refresh addresses onto the memory address bus. It will also issue a –MEMR command. For correct operation –REFRESH should not be pulled low unless CPUHLDA is active.

**DATA CONVERSION**

A state machine for controlling the conversion between 16-bit data accesses from the CPU and 8-bit peripherals is contained in the VL82C201. This state machine will generate the control signals DIR245, GATE245, and CNTLOFF to the Data Buffer chip to route the data correctly for both read and write conversions. The conversion logic will signal the wait state logic to hold the CPU and start the read/write of the low data byte. It will then latch the low byte for a read operation, negate the bus control signals, switch SA0 to a high, and then perform the read/write operation for the high data byte. The VL82C201 also uses the DIR245 and GATE245 during 8-bit DMA cycles to route the lower byte on the system data

bus to or from the high or low byte of on-board memory.

**NUMERICAL PROCESSOR AND PERIPHERAL CONTROL**

The VL82C201 generates a reset signal and chip select signal for the 80287 Numerical Processor. The signal RESET287 is used to reset the 80287 and can be activated by a system reset or an I/O write to address 0F1 hex. –NPCS is used as a chip select for the 80287 and is decoded at addresses 0F8-0FF hex.

The VL82C201 also controls the –BUSY286 signal sent to the 80286 from the Numerical Processor. The 80287 will assert –BUSY287 whenever it is performing a task. This signal is passed to the 80286 by asserting the –BUSY286 output. Normally –BUSY286 will follow –BUSY287. However, if the –ERROR signal is asserted while the –BUSY287 signal is active, the –BUSY286 output will be latched low and will remain active until cleared by an I/O write cycle to address 0F0 hex or 0F1 hex.

## TABLE 1. WAIT STATES

| Access Type | RAM RDWT | RAM WRWT | ROM WTST | F16 | –MEM CS16 | –IO CS16 | Number of Waits | Command Delay |
|---|---|---|---|---|---|---|---|---|
| INTA Cycles | X | X | X | X | X | X | 4 | Yes |
| 8-Bit I/O | X | X | X | X | X | 1 | 4 | Yes |
| 16-Bit I/O | X | X | X | X | X | 0 | 1 | Yes |
| Off-board 8-Bit Memory | X | X | X | 0 | 1 | X | 4 | Yes |
| Off-board 16-Bit Memory | X | X | X | 0 | 0 | X | 1 | No |
| On-board ROM Read | X | X | 1 | 1 | X | X | 3 | No |
| On-board ROM Read | X | X | 0 | 1 | X | X | 2 | No |
| On-board RAM Write | 0 | 0 | X | 1 | X | X | 0 | No |
| On-board RAM Write | X | 1 | X | 1 | X | X | 1 | No |
| On-board RAM Read | 0 | X | X | 1 | X | X | 0 | No |
| On-board RAM Read | 1 | 1 | X | 1 | X | X | 1 | No |

## AC CHARACTERISTICS: TA = QC: 0°C to +70°C, QI: –40°C to +85°C, VDD = 5 V ±5%, VSS = 0 V

### CPU MODE TIMIING

| Symbol | Parameter | 16 MHz | | 20 MHz | | Unit | Condition |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | |
| t1 | PROCCLKIN Period | 31 | | 25 | | ns | |
| t2 | PROCCLKIN High Pulse Width | 11 | | 9 | | ns | |
| t3 | PROCCLKIN Low Pulse Width | 7 | | 6 | | ns | |
| t4 | PROCCLK Rise Time | | 5 | | 4 | ns | 1.0 V to 3.6 V, CL = 75 pF |
| t5 | PROCCLK Fall Time | | 4 | | 4 | ns | 3.6 V to 1.0 V, CL = 75 pF |
| t6 | FCLK Period | 15 | | 12 | | ns | |
| t7 | FCLK High Pulse Width | 6 | | 5 | | ns | |
| t8 | FCLK Low Pulse Width | 6 | | 5 | | ns | |
| t9 | OSC Rise/Fall Time | | 15 | | 15 | ns | |
| tD10 | MHZ7 from OSC Delay | | 15 | | 15 | ns | |
| tD11 | MHZ119 from OSC Delay | | 20 | | 20 | ns | |
| tD12 | PROCCLK from FCLK Delay | | 20 | | 17 | ns | |
| tSU13 | –S0, –S1 to PROCCLKIN Setup Time | 11 | | 9 | | ns | |
| tH14 | –S0, –S1 from PROCCLKIN Hold Time | 1 | | 1 | | ns | |
| tSU15 | M/–IO to PROCCLKIN Setup Time | 20 | | 20 | | ns | |
| tH16 | M/–IO from PROCCLKIN Hold Time | 3 | | 3 | | ns | |
| tSU17 | F16 to PROCCLKIN Setup Time | 7 | | 6 | | ns | |
| tH18 | F16 from PROCCLKIN Hold Time | 5 | | 5 | | ns | |
| tSU19 | POWERGOOD to PROCCLKIN Setup Time | 20 | | 20 | | ns | Note 1 |
| tH20 | POWERGOOD to PROCCLKIN Hold Time | 5 | | 5 | | ns | Note 1 |
| tD21 | RESET from PROCCLKIN Delay | | 24 | | 24 | ns | |
| tD22 | RESCPU from PROCCLKIN Delay | | 17 | | 15 | ns | |
| tD23 | SYSCLK from PROCCLKIN Delay | | 26 | | 23 | ns | |
| tD24 | –ENAS from PROCCLKIN Delay | | 26 | | 26 | ns | |
| tSU25 | M/–IO, A1 to –S0, –S1 Setup Time | 15 | | 15 | | ns | |
| tSU26 | SWRST to PROCCLKIN Setup Time | 20 | | 20 | | ns | Note 1 |
| t27 | SWRST Pulse Width | 60 | | 60 | | ns | |
| tD28 | ALE from PROCCLKIN Delay | | 18 | | 16 | ns | |

**Notes:** 1. POWERGOOD and SWRST are asynchronous inputs. This specification is given for testing purposes only, to assure recognition at a specific PROCCLKIN edge.

**CPU MODE TIMING (Cont.)**

| Symbol | Parameter | 16 MHz | | 20 MHz | | Unit | Condition |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | |
| tD29 | DT/–R Low from PROCCLKIN Delay | | 30 | | 30 | | |
| tD30 | DT/–R High from PROCCLKIN Delay | | 40 | | 35 | | |
| tD31 | –DENLO, –DENHI Low from PROCCLKIN Delay | | 33 | | 30 | ns | Write Cycles |
| tD32 | –DENLO, –DENHI Low from PROCCLKIN Delay | | 40 | | 35 | ns | Read Cycles |
| tD33 | –DENLO, –DENHI High from PROCCLKIN Delay | | 33 | | 30 | ns | Read and Write Cycles |
| tD34 | –READY Active from PROCCLKIN Delay | | 16 | | 15 | ns | |
| tD35 | –READY Inactive from PROCCLKIN Delay | 5 | | 3 | | ns | Note 2 |
| tD36 | XDATADIR from PROCCLKIN Delay | | 35 | | 35 | | |
| tSU37 | –IOCS16 to PROCCLKIN Setup Time | 17 | | 15 | | ns | |
| tH38 | –IOCS16 from PROCCLKIN Hold Time | 2 | | 2 | | ns | |
| tSU39 | IOCHRDY to PROCCLKIN Setup Time | 15 | | 12 | | ns | |
| tH40 | IOCHRDY from PROCCLKIN Hold Time | 2 | | 2 | | ns | |
| tD41 | –CMD, –XCMD, –SCMD from PROCCLKIN Delay | | 30 | | 30 | ns | Note 3 |
| tSU42 | –WS0 to PROCCLKIN Setup Time | 15 | | 12 | | ns | |
| tH43 | –WS0 from PROCCLKIN Hold Time | 3 | | 3 | | ns | |
| tSU44 | –MEMCS16 to PROCCLKIN Setup Time | 15 | | 12 | | ns | |
| tH45 | –MEMCS16 from PROCCLKIN Hold Time | 4 | | 4 | | ns | |
| tSU46 | A0 to PROCCLKIN Setup Time | 20 | | 20 | | ns | |
| tD47 | SA0 from PROCCLKIN Delay | | 30 | | 25 | | |
| tSU48 | –XBHE to PROCCLKIN Setup Time | 20 | | 15 | | | |
| tD49 | –DENLO, –DENHI from PROCCLKIN Delay | | 45 | | 40 | | Note 4 |
| tD50 | –CMD, –XCMD, –SCMD from PROCCLKIN Delay | | 40 | | 35 | ns | Note 4 |
| tD51 | Q1 from PROCCLKIN Delay | | 30 | | 30 | ns | |

**Notes:** 2. –READY is an open drain output and requires a pull-up resistor that pulls the signal high within two PROCCLKIN cycles. A 330 Ω resistor is recommended. This specification for –READY inactive indicates when the VL82C201 stops driving the output. It does not indicate that –READY has reached a certain voltage level.

3. –CMD refers to the signal pins –MEMR, –MEMW, –IOR, and –IOW. –SCMD refers to the signal pins –SMEMR and –SMEMW. –XCMD refers to the signal pins –XMEMR, –XMEMW, –XIOR, and –XIOW.

4. Caused by CNTLOFF during 16 to 8 bit conversions.

**CPU MODE TIMING (Cont.)**

| Symbol | Parameter | 16 MHz | | 20 MHz | | Unit | Condition |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | |
| tD52 | CNTLOFF from PROCCLKIN Delay | | 30 | | 30 | ns | |
| tD53 | DIR245 from PROCCLKIN Delay | | 45 | | 45 | ns | |
| tD54 | GATE245 from PROCCLKIN Delay | | 45 | | 45 | ns | |
| tSU55 | –ROMCS to PROCCLKIN Setup Time | 15 | | 12 | | ns | |
| tH56 | –ROMCS from PROCCLKIN Hold Time | 4 | | 4 | | ns | |
| tSU57 | ROMWTST to PROCCLKIN Setup Time | 15 | | 12 | | ns | |
| tH58 | ROMWTST from PROCCLKIN Hold Time | 8 | | 8 | | ns | |
| tSU59 | RAMRDWT, RAMWRWT to PROCCLKIN Setup Time | 15 | | 12 | | ns | |
| tH60 | RAMRDWT, RAMWRWT from PROCCLKIN Hold Time | 2 | | 2 | | ns | |
| tD61 | RAMALE from PROCCLKIN Delay | | 18 | | 16 | ns | |
| tD62 | –ERAMW from PROCCLKIN Delay | | 18 | | 16 | ns | |
| tD63 | RAS from PROCCLKIN Delay | | 18 | | 16 | ns | |
| tD64 | CAS High from PROCCLKIN Low Delay | | 18 | | 16 | ns | 0 Wait State Only |
| tD65 | CAS High from PROCCLKIN High Delay | | 18 | | 16 | ns | 1 Wait State Only |
| tD66 | CAS Low from PROCCLKIN Low Delay | | 18 | | 16 | ns | 0 and 1 Wait State |
| tD67 | –INTA from PROCCLKIN Delay | | 30 | | 30 | ns | |
| tD68 | –BUSY286 from –BUSY287 Delay | | 20 | | 20 | ns | |
| tH69 | –ERROR form –BUSY287 Hold Time | 5 | | 5 | | ns | |
| tSU70 | –ERROR to –BUSY287 Setup Time | 10 | | 10 | | ns | |
| tD71 | –BUSY286 from –IOW Delay | | 25 | | 25 | ns | |
| tD72 | RESET287 from –IOW Delay | | 25 | | 25 | ns | |
| tSU73 | XA Input to –IOW Setup Time | 10 | | 10 | | ns | |
| tH74 | XA Inputs from –IOW Hold Time | 5 | | 5 | | ns | |
| tD75 | XA Inputs to –NPCS Delay | | 30 | | 30 | ns | |
| tD76 | XA Inputs to –PPICS Delay | | 25 | | 25 | ns | |

**DMA MODE TIMING**

| Symbol | Parameter | 16 MHz | | 20 MHz | | Unit | Condition |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | |
| tD79 | –DMAAEN from –AEN1, –AEN2 Delay | | 20 | | 20 | ns | |
| tD80 | XDATADIR from –XIOR Delay | | 30 | | 30 | ns | |
| tD81 | –CMD, –SCMD from –XCMD Delay | | 30 | | 30 | ns | |
| tD82 | –XBHE from SA0 Delay | | 30 | | 30 | ns | Note |
| tD83 | DIR245 from –XMEMR Delay | | 30 | | 30 | ns | |
| tD84 | GATE245 from –XMEMR, –XMEMW, or –XIOR Delay | | 35 | | 35 | ns | |

**Note:** During –AEN2, –XBHE is low. During –AEN1, –XBHE follows SA0 inverted.

**BUS MASTER MODE TIMING**

| Symbol | Parameter | 16 MHz | | 20 MHz | | Unit | Condition |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | |
| tD85 | –XCMD from –CMD Delay | | 25 | | 25 | ns | |
| tD86 | –SCMD from –CMD Delay | | 30 | | 30 | ns | |
| tD87 | XDATADIR from –IOR Delay | | 30 | | 30 | ns | |

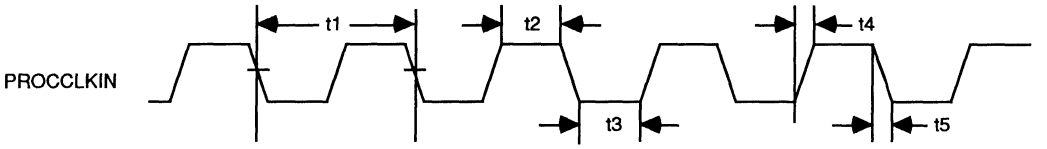
**REFRESH MODE TIMING**

| Symbol | Parameter | 16 MHz | | 20 MHz | | Unit | Condition |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | |
| tSU88 | –REFRESH to PROCCLKIN Setup Time | 20 | | 20 | | ns | |
| tD89 | –REFEN from PROCCLKIN Delay | | 30 | | 30 | ns | |
| tD90 | –MEMR, –XMEMR, –SMEMR from PROCCLKIN Delay | | 40 | | 40 | ns | During –REFRESH |

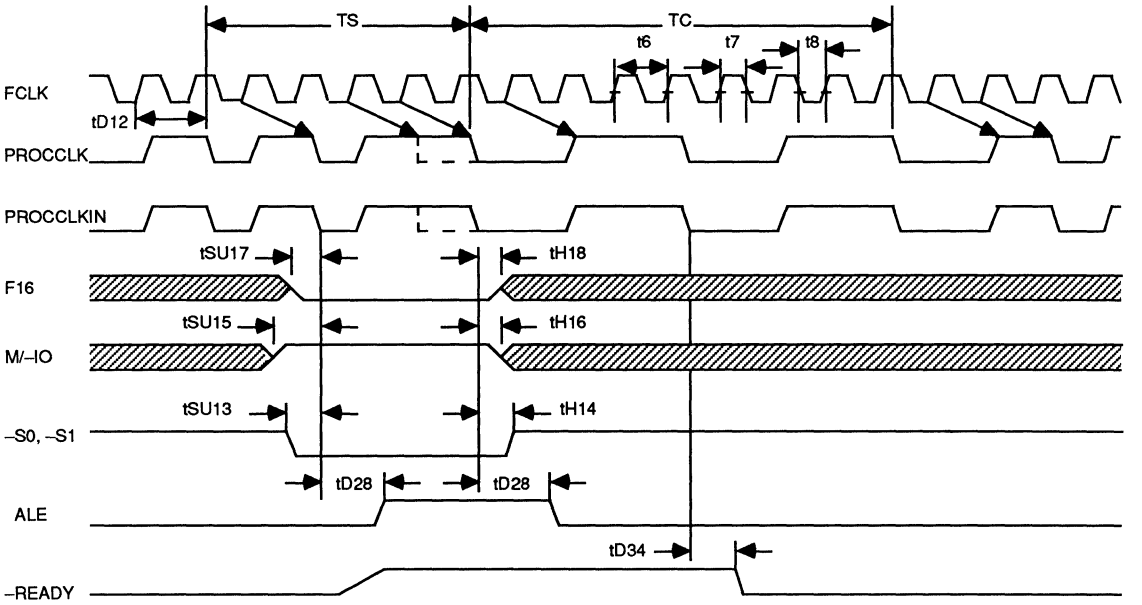
**MEMORY CONTROL TIMING DURING DMA OR MASTER MODES**

| Symbol | Parameter | 16 MHz | | 20 MHz | | Unit | Condition |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | |
| tSU91 | –MEMR, –XMEMR, –MEMW, –XMEMW to PROCCLKIN Setup Time | 17 | | 17 | | ns | |
| tH92 | –MEMR, –XMEMR, –MEMW, –XMEMW to PROCCLKIN Hold Time | 2 | | 2 | | ns | |
| tSU93 | F16 to –MEMR, –XMEMR Setup Time | 5 | | 5 | | ns | |
| tH94 | F16 from –MEMR, –XMEMR Hold Time | 10 | | 10 | | ns | |
| tD95 | DT/–R from –MEMR, –XMEMR Delay | | 30 | | 30 | ns | |
| tD96 | –DENLO from SA0 Delay | | 30 | | 30 | ns | |
| tD97 | –DENHI from –XBHE Delay | | 35 | | 35 | ns | |

**PROCCLK TIMING WAVEFORMS**

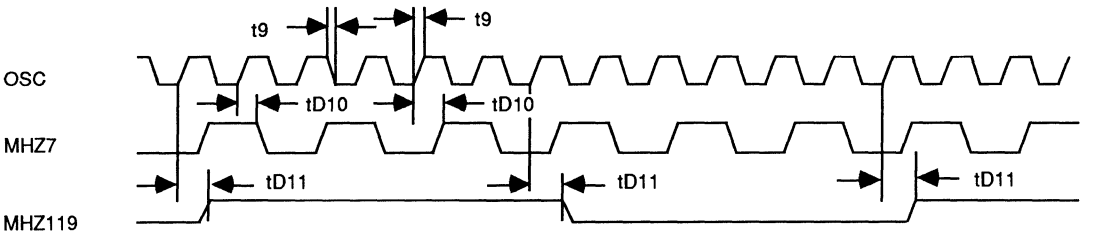



**CLOCK MODULATION WAVEFORM**

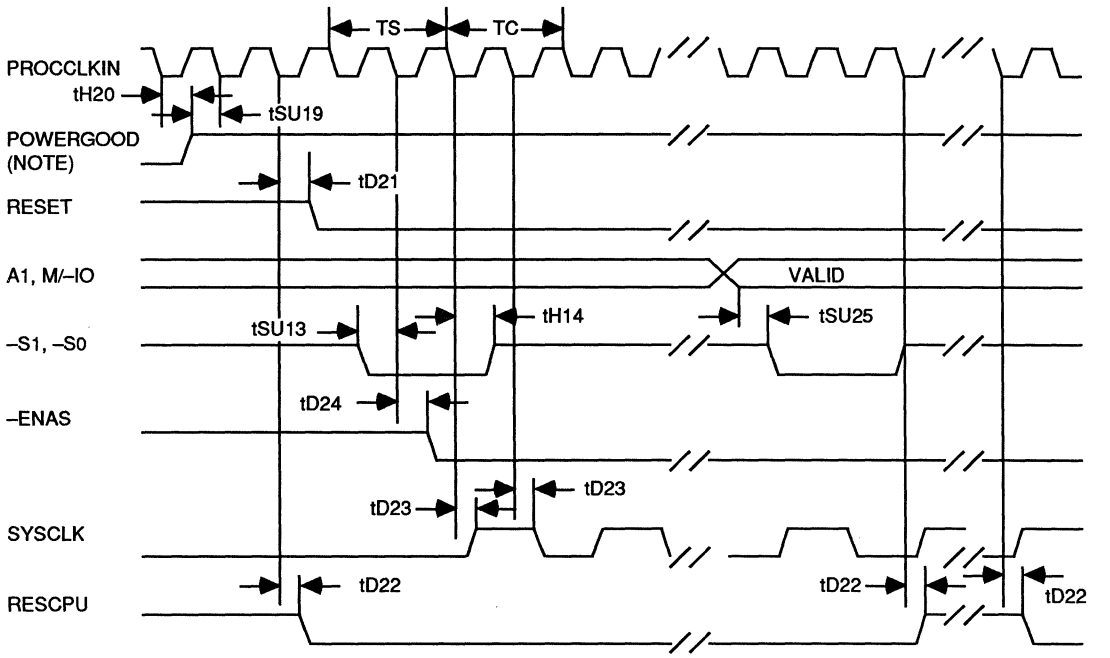


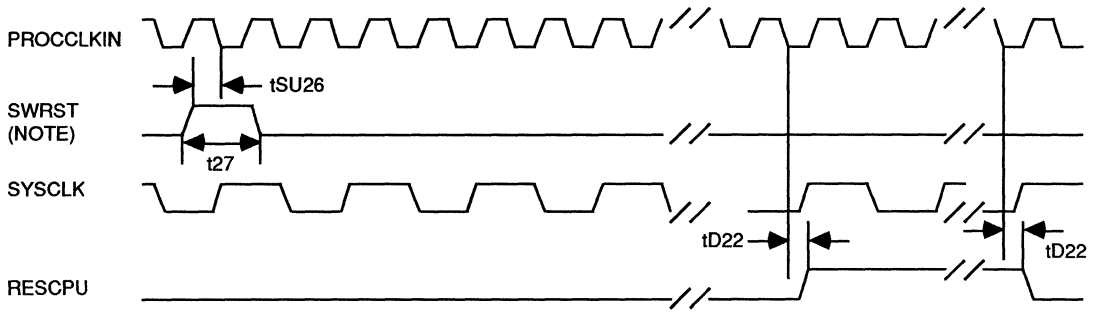

**Note:** Timing is shown for an off-board memory cycle. The same clock transitions will occur if M/–IO is sampled low, regardless the state of F16.

**CRYSTAL DERIVED CLOCK WAVEFORMS**



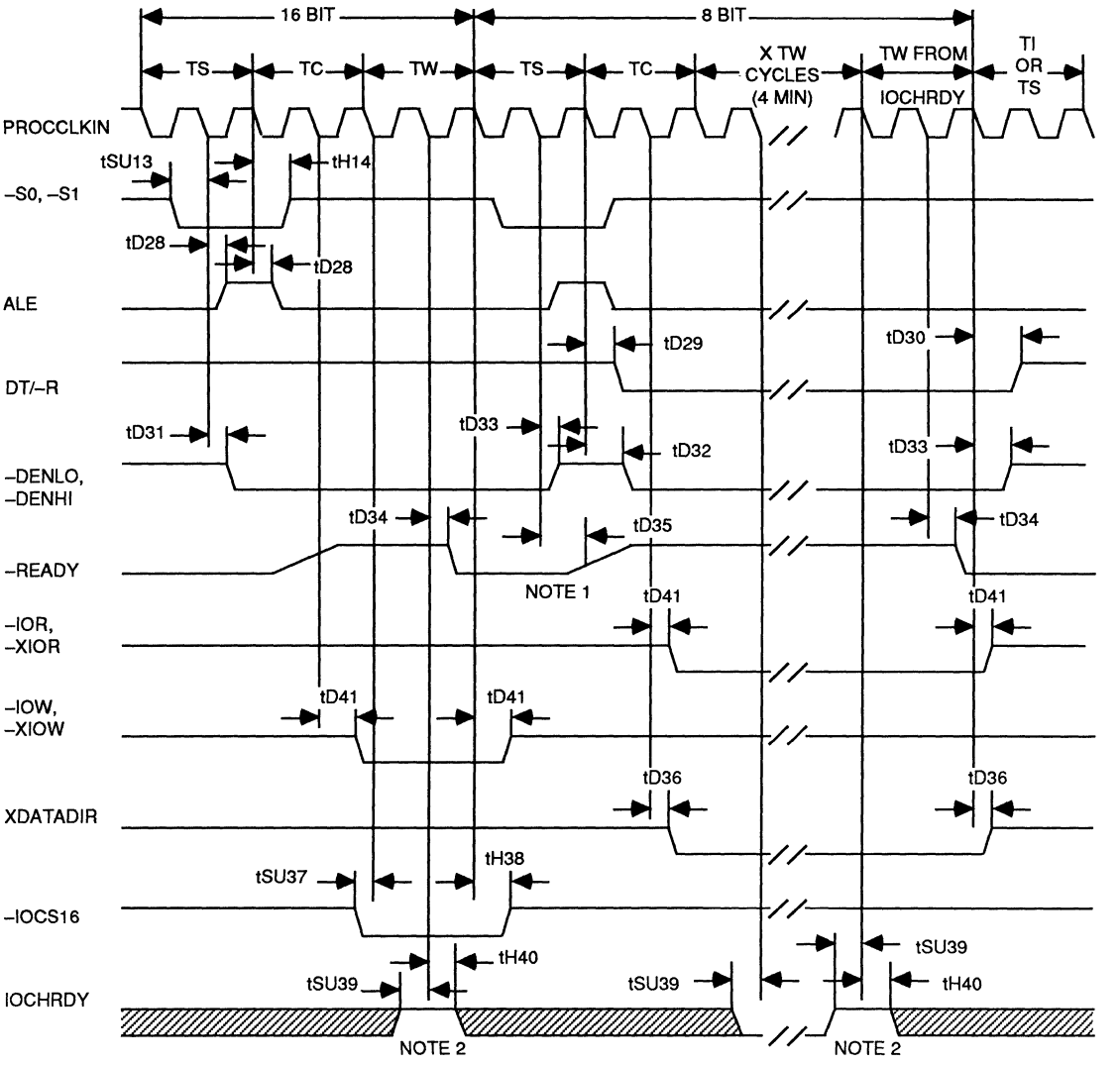
**RESET AND CLOCK TIMING WAVEFORMS**




**Note:** POWERGOOD and SWRST are asynchronous inputs. This specification is given for testing purposes only, to assure recognition at a specific PROCCLKIN edge.

**I/O TIMING WAVEFORM**

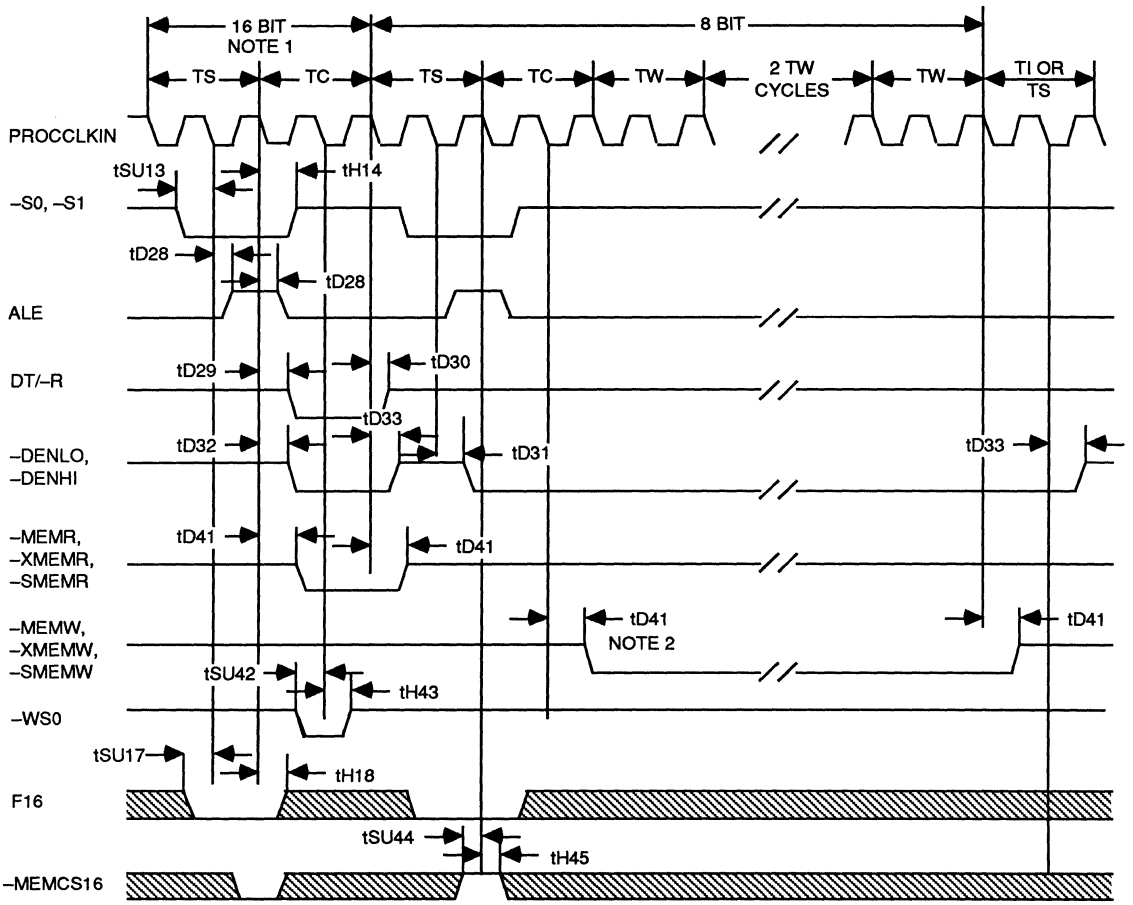



**Notes:** 1. –READY is an open drain output and requires a pull-up resistor that pulls the signal high within two PROCCLK cycles. A 300 Ω resistor is recommended.

2. IOCHRDY is sampled for the first time in the middle of the first wait state. If it is sampled high, 16-bit bus cycles will terminate with only one wait state. From then on IOCHRDY is sampled at the end of each wait state cycle. When IOCHRDY is sampled high, the bus cycle will terminate one wait state cycle later.

   For 8-bit bus cycles IOCHRDY is sampled for the first time at the end of the third wait state cycle. If it is sampled high, the bus cycle will terminate in four wait states. Otherwise, the bus cycle will be extended until IOCHRDY is sampled high.

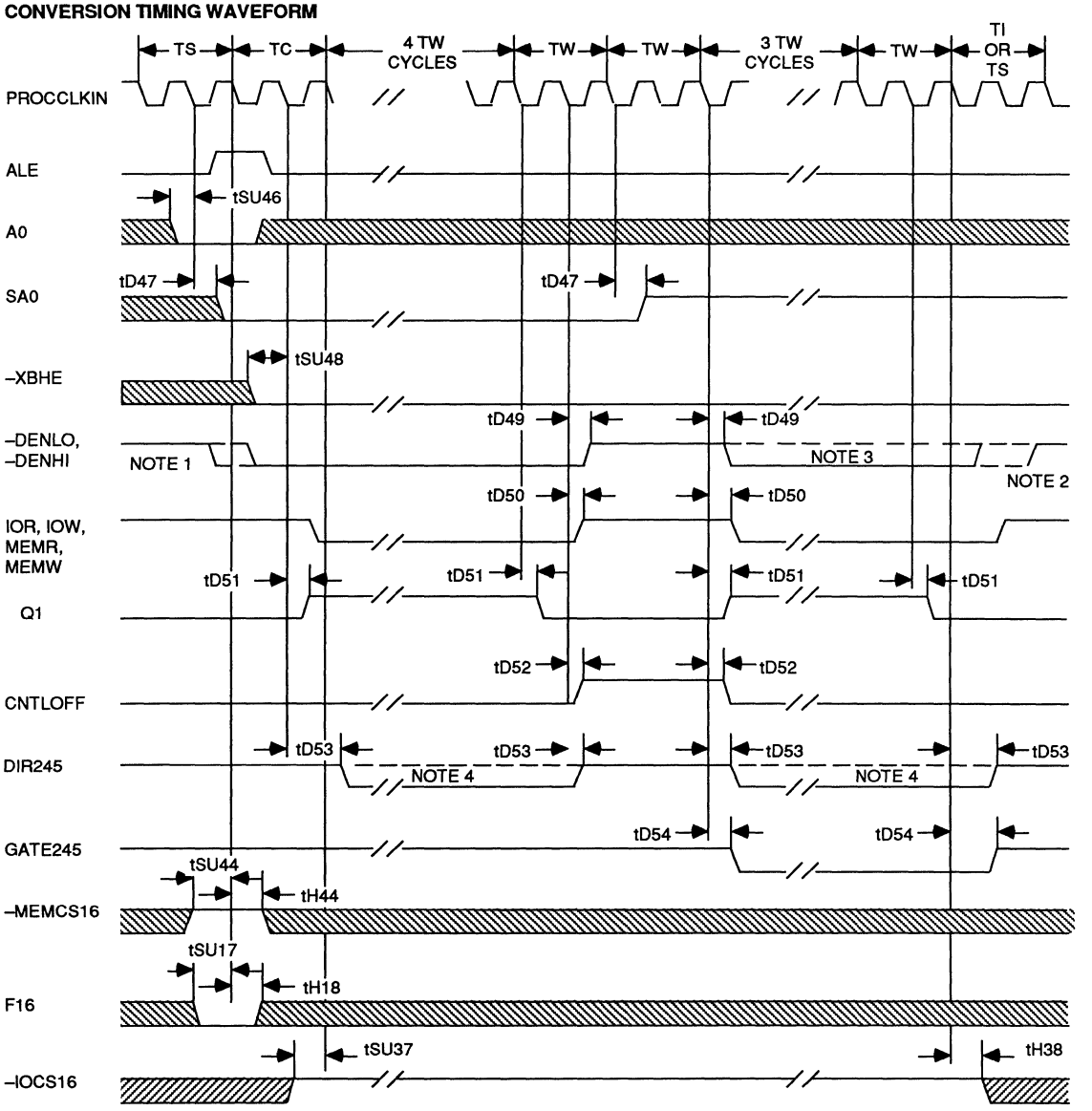
**OFF-BOARD MEMORY TIMING WAVEFORM**




**Notes:** 1. This 16-bit cycle is shown as zero wait states terminated by the –WS0 input. Normal off-board memory cycles are one wait state.

2. A command delay is shown on the 8-bit write cycle. Command delays will exist for both reads and writes on the 8 bit cycles. A command delay is not generated for 16-bit reads or writes.

**CONVERSION TIMING WAVEFORM**



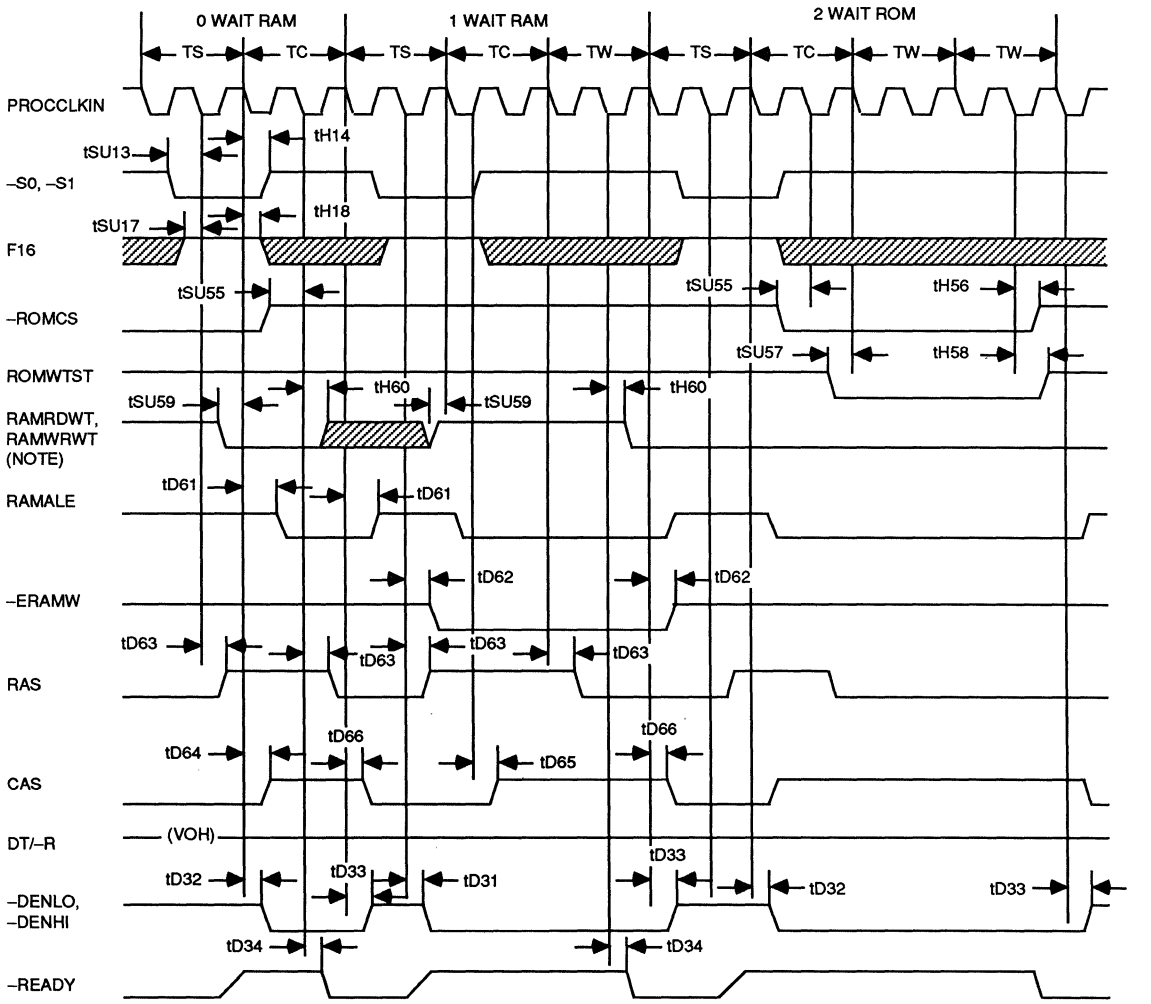

**Notes:** 1. The first transition shown here is for write cycles. The –DEN signals will go active one PROCCLKIN cycle later for read cycles.

2. The first transition shown here is for read cycles. The –DEN signals will go inactive one PROCCLKIN cycle later for write cycles.

3. –DENLO will not go active during the second half of a conversion cycle for I/O write or memory write commands.

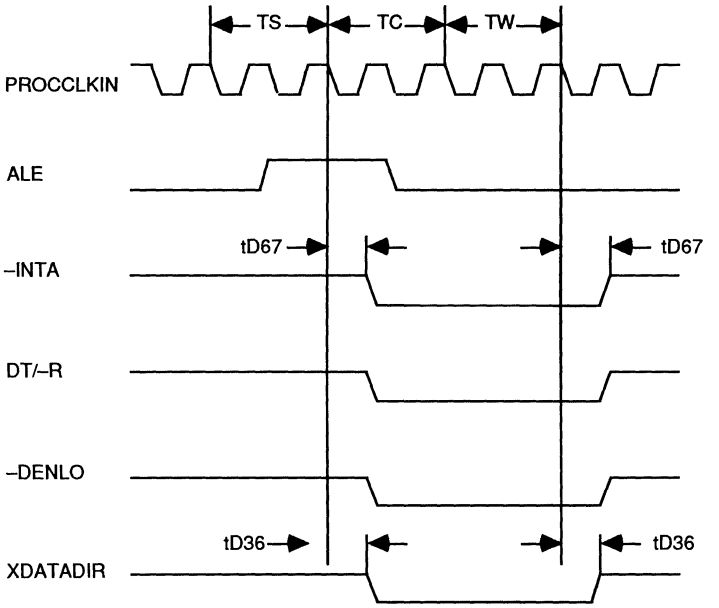
4. DIR245 goes low for a write cycle. It will remain high for read cycles.

**ON-BOARD MEMORY TIMING**

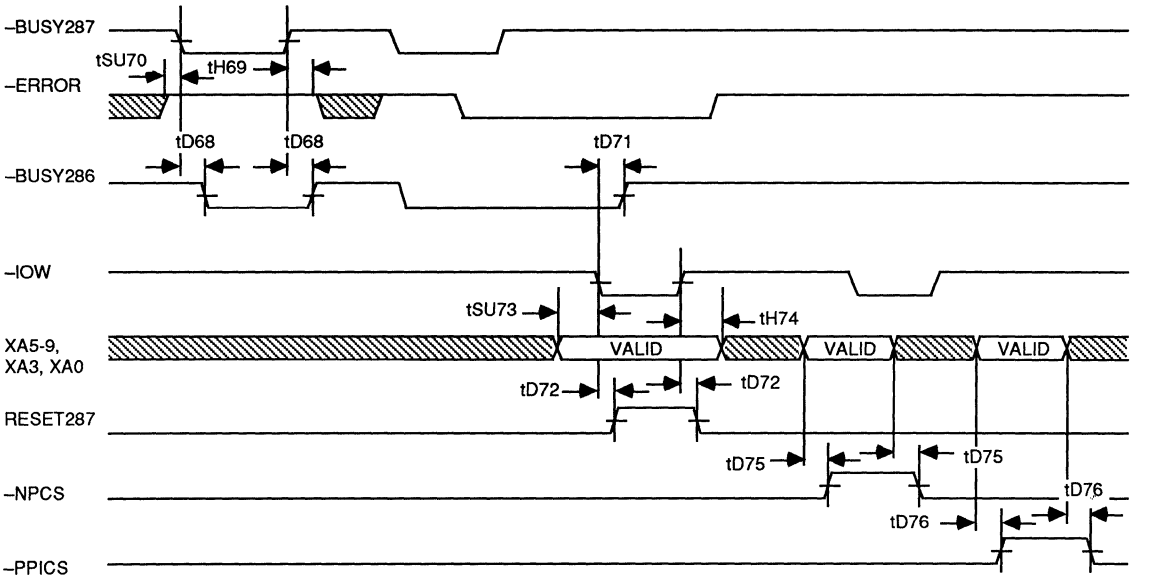



**Note:** Although RAMRDWT and RAMWRWT can be changed dynamically for each memory cycle, care must be taken to never allow RAMRDWT to be high and RAMWRWT to be low at the same time for more than 60 ns. This results in zero wait state write cycles and one wait state read cycles. This was determined to be an unrealistic operating mode and is used to put the VL82C201 into a test mode that will disrupt normal system operation.

**INTA TIMING WAVEFORM**

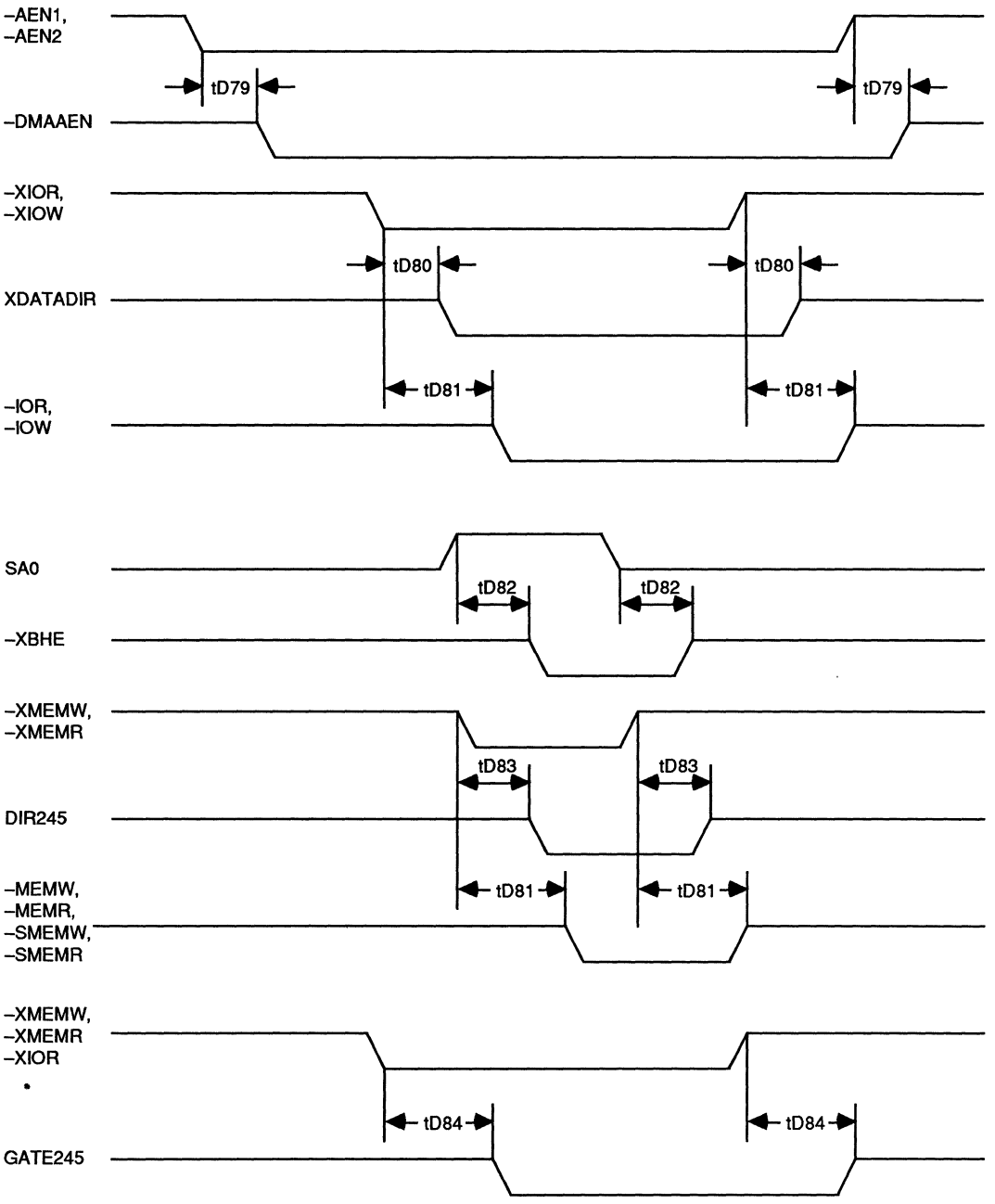



**NUMERICAL PROCESSOR INTERFACE TIMING WAVEFORM**

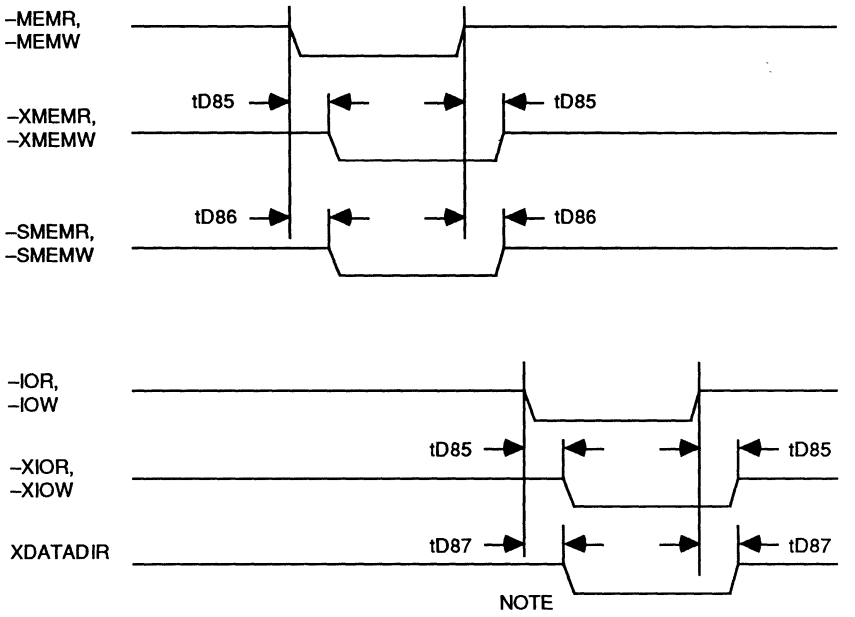



4

**DMA MODE TIMING WAVEFORMS**

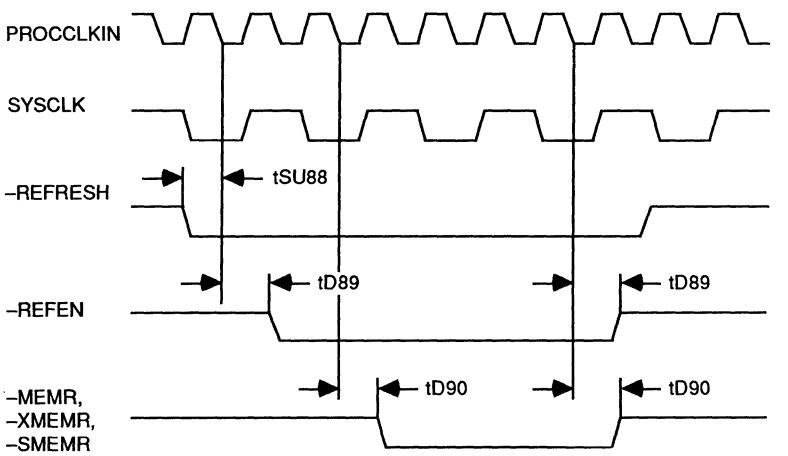


**BUS MASTER MODE TIMING WAVEFORM**

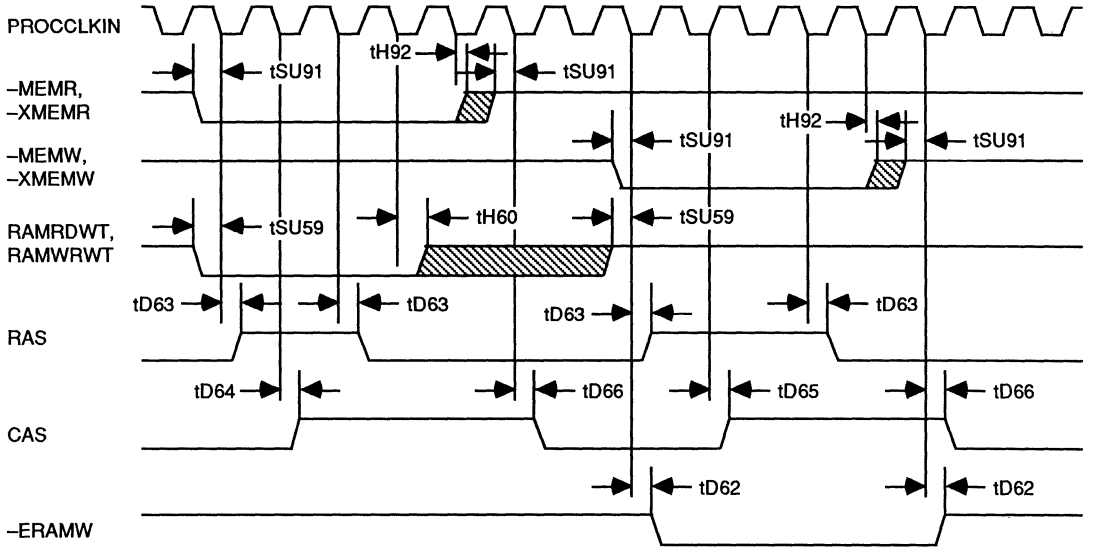



**Note:** XDATADIR goes low only for -IOR when XA9, XA8 are low and -NPCS is not active.

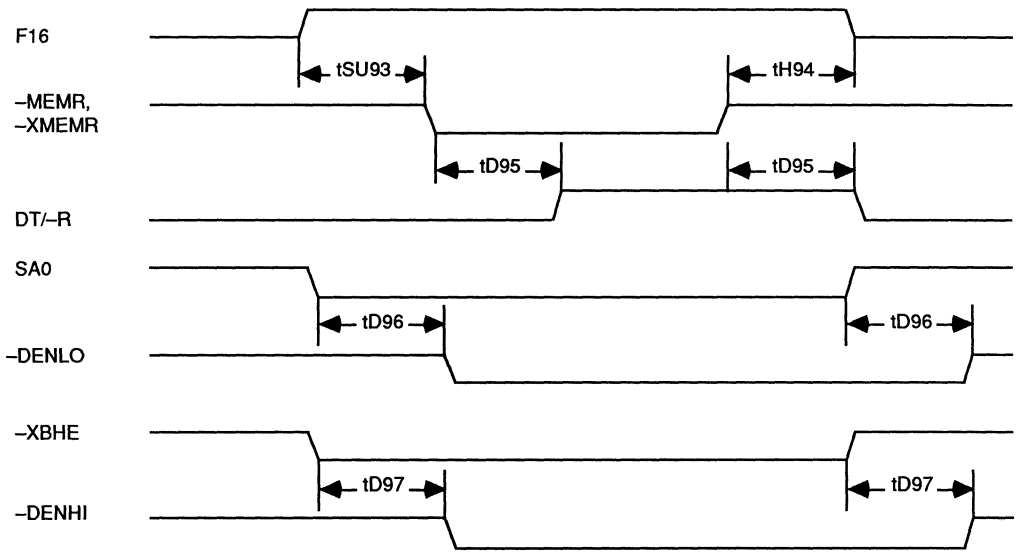
**REFRESH TIMING WAVEFORM**



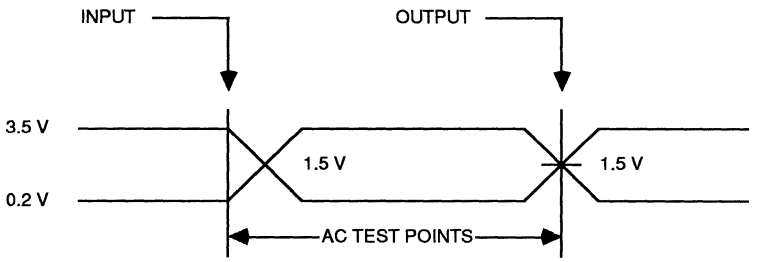
**MEMORY CONTROL TIMING WAVEFORMS DURING DMA OR MASTER MODES**



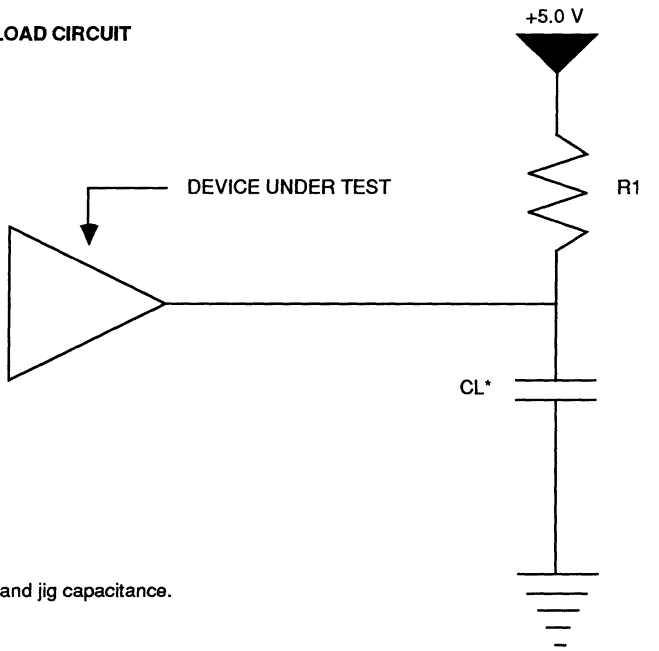

**BUS CONTROL TIMING WAVEFORMS DURING DMA OR MASTER MODES**



**AC TESTING - INPUT, OUTPUT WAVEFORM**




**AC TESTING - LOAD CIRCUIT**




*Includes scope and jig capacitance.

**AC TESTING - LOAD VALUES**

| Test Pin | CL (pF) |
|---|---|
| 20, 39-42, 45, 47, 49-51 | 200 |
| 46, 52 | 75 |
| 21-26, 28-31, 33-37, 43, 44, 53, 55-58, 60-66 | 50 |

| Test Pin | R1 (Ω) |
|---|---|
| 71 | 600 |
| 34-37, 39-42, 44, 50, 51 | 10K |

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Ambient Operating Temperature | QC = 0°C to +70°C<br>QI = –40°C to +85°C |
| Storage Temperature | –65°C to +150°C |
| Supply Voltage to Ground Potential | –0.5 V to +7.0 V |
| Applied Input Voltage | –0.5 V to +7.0 V |
| Power Dissipation | 500 mW |

Stresses above those listed may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## DC CHARACTERISTICS: TA = QC: 0°C to +70°C, QI: –40°C to +85°C, VDD = 5 V ±5%, VSS = 0 V

| Symbol | Parameter | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| VOH | Output High Voltage | 2.4 | | V | IOH = –3.3 mA |
| VOL1 | Output Low Voltage | | 0.45 | V | IOL = 24 mA, Note 1 |
| VOL2 | Output Low Voltage | | 0.45 | V | IOL = 8 mA, Note 2 |
| VIH | Input High Voltage | 2.0 | VDD + 0.5 | V | Except POWERGOOD, PROCCLKIN |
| VIL | Input Low Voltage | –0.5 | 0.8 | V | |
| VIHS | Input High Voltage | 4.0 | VDD + 0.5 | V | POWERGOOD, Schmitt-trigger |
| VIHC | Input High Voltage | 3.8 | VDD + 0.5 | V | PROCCLKIN |
| VILC | Input Low Voltage | –0.5 | 0.6 | V | PROCCLKIN |
| CO | Output Capacitance | | 8 | pF | |
| CI | Input Capacitance | | 8 | pF | |
| CIO | Input/Output Capacitance | | 16 | pF | |
| ILOL | Three-state Leakage Current | –100 | 100 | µA | |
| ILI | Input Leakage Current | –10 | 10 | µA | Except –S1, –S0, XTAL1(1) |
| ILIS | Input Leakage Current | –0.5 | 0.01 | µA | –S1, –S0, Note 3 |
| ILIX | Input Leakage Current | –40 | 40 | µA | XTAL1(1) |
| ICC | Power Supply Current | | 40 | mA | Note 4 |

**Notes:** 1. Pins 20, 39-42, 45, 47, 49-52.
2. All other pins.
3. –S1 and –S0 have small pull-up resistors to VDD and source up to 0.5 mA when pulled low.
4. Inputs = VSS or VDD, outputs are not loaded.