SiS900

Fast Ethernet PCI Bus 10/100 Mbps LAN Single Chip with OnNow Support

Preliminary

Revision 1.0

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Silicon Integrated System Corp.

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Features

- Integrated Fast Ethernet controller and 10/100 megabit per second (Mbps) Physical Layer Transceivers for the PCI local bus
  - PCI specification revision 2.1 compliant
  - 32-bit glueless PCI host interface
  - Plug and Play compatible
  - Supports PCI clock frequency from DC to 33 MHz independent of network clock
  - Supports network operation with PCI clock from 25Mhz to 33Mhz
  - Supports both +3.3v and +5v PCI signaling
  - High-performance 32-bit PCI bus master architecture with integrated Direct Memory Access (DMA) Controller for low CPU and bus utilization
  - Supports an unlimited PCI burst length
  - Supports big endian and little endian byte alignments
  - Supports PCI Device ID, Vendor ID/Subsystem ID, Subsystem Vendor ID programming through the EEPROM interface
  - Implements optional PCI 3.3v auxiliary power source 3.3Vaux pin and optional PCI power management event (PME#) pin
  - IEEE 802.3 and 802.3u standard compatible
  - IEEE 802.3u Auto Negotiation and Parallel detection for automatic speed selection
  - Full duplex and half duplex mode for both 10 and 100 Mbps.
  - Fully compliant ANSI X3.263 TP-PMD physical sub-layer which includes adaptive equalization and Baseline Wander compensation.
  - Automatic Jam and IEEE 802.3x Auto-Negotiation for flow control
  - Single access to complete PHY register set
  - Built-in waveform shaping requires no external filters
  - Single 25Mhz clock for 10 and 100 Mbps operation.
  - Power down of 10Base-T/100Base-TX sections when not in use
  - Jabber control and auto-polarity correction for 10Base-T.
  - User programmable LED function mapping
  - Supports software, enhanced software, and automatic polling schemes to internal PHY status monitor and interrupt
  - Supports 10BASE-T, 100BASE-TX, and any future

- Supports PC97, PC98, and Net PC requirements – Green PC compatible
  - Supports Advanced Configuration and Power Interface Specification (ACPI) Revision 1.0
  - Supports PCI Bus Power Management Interface Specification Version 1.0a
  - Supports Network Device Class Power Management Specification Version 1.0a
  - Supports PCI Hot-Plug Specification Revision 1.0
  - Implements full OnNow features including pattern matching and link status wake-up with automatic internal PHY status polling
  - Implements optional Magic Packet™ remote wake-up scheme
  - Implements IEEE 802.3x compliant Flow Control

- Additional features
  - Internal 128-bit Multicast Hash Table address filter
  - Serial EEPROM support
  - Boot ROM supports up to 128 Kbytes
  - Extensive programmable internal/external loopback capabilities
  - +3.3V power supply with +5V tolerant I/Os
  - 128pin PQFP package. Low-Power CMOS 0.35um Technology

1. INTRODUCTION

1.1 SiS900 Overview

SiS900 is a single chip 10/100Mbps Fast Ethernet LAN solution, which fully integrates both the Media Access Controller (MAC) with PCI bus master interface and 802.3u compliant 10/100Mbps physical layer interface into a 128 pins PQFP, 0.35um process chip. It is targeted at low-cost, low-power, high volume desktop PC motherboards, mobile PC module, adapter cards, and embedded systems.

SiS900 fully implements the PCI bus version 2.1 interface for host communications. Packet descriptors and data are transferred via bus-mastering DMA channels, reducing the burden on the host CPU. The buffer management scheme utilized by SiS900 optimizes the use of memory space and the system bus. Descriptor information, describing the buffer space in which packet information is held, is symmetrical between transmit and receive operations. SiS900 supports both half-duplex and full-duplex operations with minimum inter frame gap and IEEE802.3x full-duplex flow control. In order to meet the PC 98 and the Green PC power saving requirements, SiS900 supports ACPI and Network Device Class Power Management specification. All the device states of D0, D1, D2, D3hot, and D3cold are implemented. SiS900 also supports Remote Wake On LAN and OnNow for the Desktop PC management. Additional features include a serial EEPROM interface for device information access and a Boot ROM interface up to 128K bytes for remote boot functions support.

SiS900 also integrates analog interface for twisted pair Fast Ethernet applications. SiS900 can be configured for either 100 Mbps (100Base-TX) or 10 Mbps (10Base-T) Ethernet operation. SiS900 consists of 4B5B/Manchester encoder/decoder, scrambler/descrambler, 100Base-TX/10Base-T twisted pair transmitter with wave shaping and output driver, 100Base-TX/10Base-T twisted pair receiver with on chip equalizer and baseline wander correction, clock and data recovery, and Auto Negotiation capability. The addition of internal output wave shaping circuitry and on-chip filters eliminates the need for external filters normally required in 100Base-TX and 10Base-T applications. SiS900 can automatically configure itself for 100 or 10 Mbps and Full or Half Duplex operation with the on-chip Auto Negotiation algorithm. SiS900 PHY can access eleven 16-bit registers through the internal Management Interface (MI) serial port. These registers contain configuration inputs, status outputs, and device capabilities.

1.1.1 Document Organization

The document is organized in the following sections:

Chapter 1 - Introduction, provides a general description of SiS900 with system diagrams.

Chapter 2 - Pin Description, describes SiS900 package, pin out and each of SiS900 pins.

Chapter 3 - Functional Description, describes the operation of SiS900 in detail.

Chapter 4 – Registers Description, specifies the register sets and register bit definitions.

Chapter 5 - DC and AC Specifications, specifies timing parameters for SiS900.

Chapter 6 - Application Circuit Information, specifies the guideline for application circuit layout.

Chapter 7 – Physical Dimensions, specifies the SiS900 package outline and dimensions

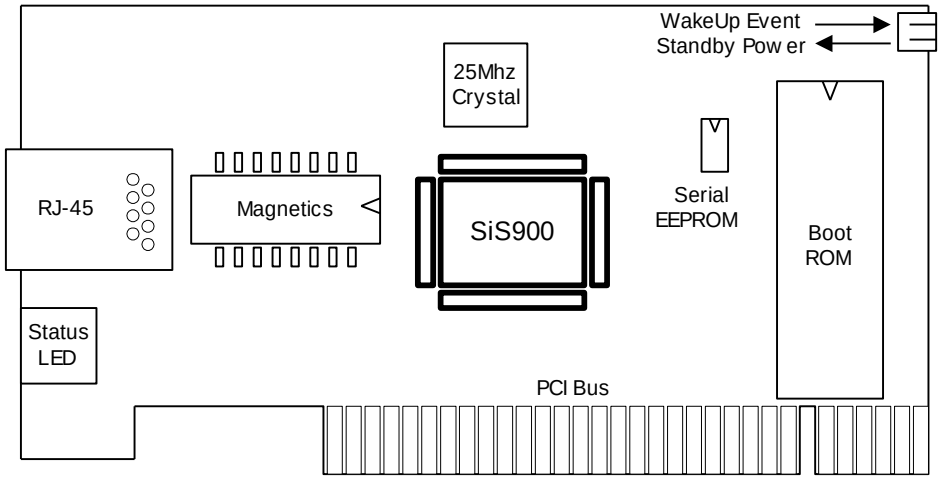


Figure 1-1 SiS900 System Diagram

2. PIN ASSIGNMENT

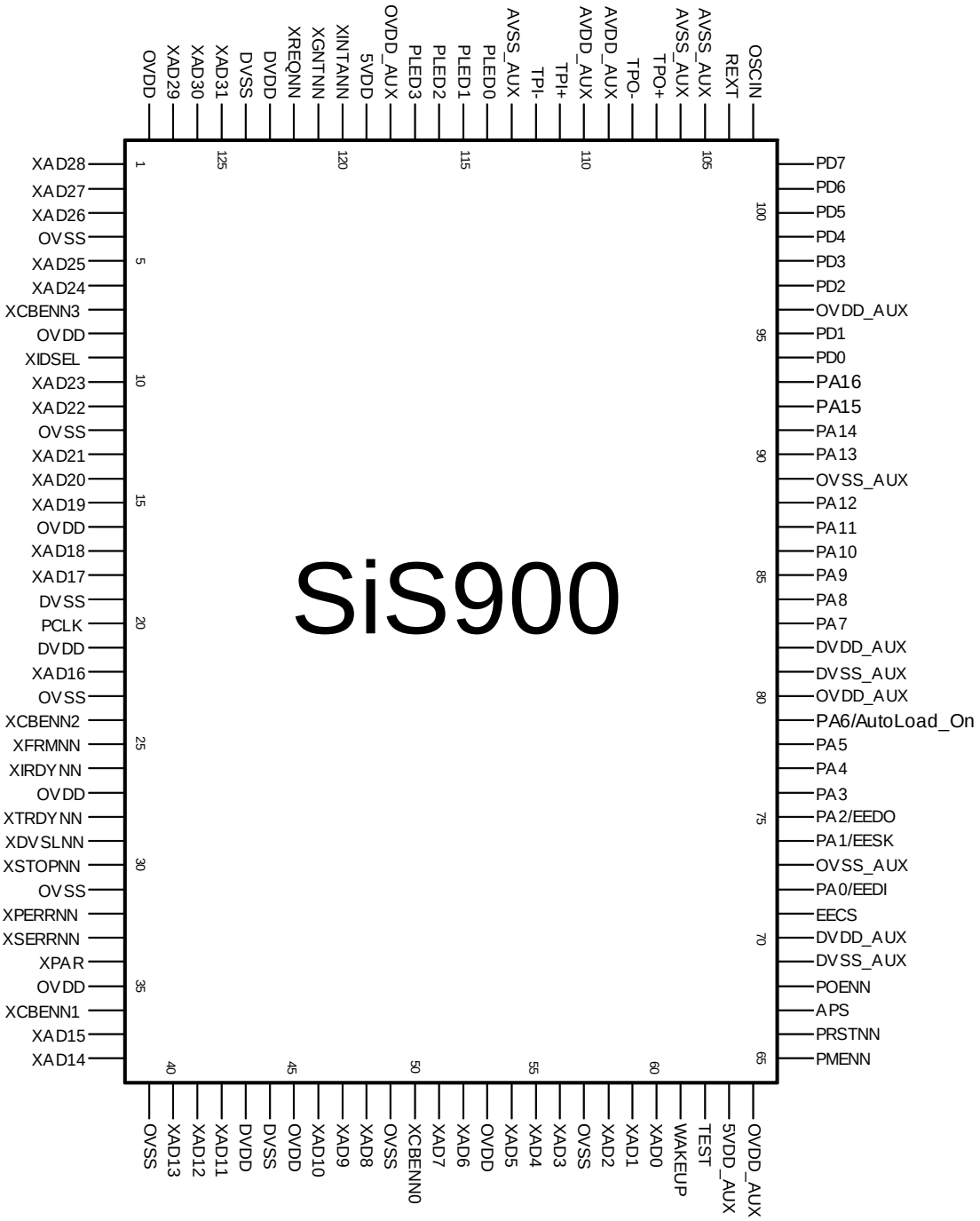


Figure 2-1 Pin Assignment

2.1 Signal Type Definition

I	Input is a standard input only signal.
O	Totem Pole Output is a standard active driver.
I/O	Input/Output signal.
T/S	Tri-State is a bi-directional, tri-state input/output pin.
S/T/S	Sustained Tri-State is an active low tri-state signal owned and driven by one agent at a time. The agent that drives an s/t/s pin low must drive it high for at least one clock before letting it float. A new agent can't start driving a s/t/s signal any sooner than one clock after the previous owner tri-states it.
O/D	Open Drain allows multiple devices to share as a wired OR.

2.2 PCI Bus Interface

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
AD[31::0]	125-127, 1-3, 5-6, 10-11, 13-15, 17-18, 22, 37-38, 40-42, 46-48, 51-52, 54-56, 58-60	T/S	**Address and Data** Multiplexed address and data bus. As a bus master, the SiS900 will drive address during the first bus phase. During subsequent phase, the SiS900 will either read or write data expecting the target to increment its address pointer. As a bus target, the SiS900 will decode each address on the bus and respond if it is the target being addressed.
CBE[3::0]#	7, 24, 36, 50	T/S	**Bus Command/Byte Enable** During the address phase these signals define the "bus command" or the type of bus transaction that will take place. During the data phase these pins indicate which byte lanes contain valid data. CBE[0]# applies to byte 0 (bits7-0) and CBE[3]# applies to byte 3 (bits31-24) in the Little Endian Mode. In Big Endian Mode, CBE[0]# applies to byte 0 (bits31-24) and CBE[3]# applies to bytes 3 (bits7-0).
DEVSEL#	29	S/T/S	**Device Select** As a target, the SiS900 asserts this signal low when it recognizes its address after FRAME# is asserted. As a bus master, the SiS900 samples this signal to insure that a PCI target recognizes destination address for the data transfer.
FRAME#	25	S/T/S	**Frame** As a bus master, this signal is asserted low to indicate the beginning and duration of a bus transaction. Data transfer takes place when this signal is asserted. It is de-asserted before the transaction is in its final phase. As a target, the device monitors this signal before decoding the address to check if the current transaction is addressed to it.
GNT#	121	T/S	**Grant** This signal is asserted low to indicate to the SiS900 that it has been granted ownership of the bus by the central arbiter. This input is used when the SiS900 is acting as a

			bus master.
IDSEL	9	I	**Initialization Device Select** This pin is sampled by the SiS900 to identify when configuration read and write accessed are intended for it.
INTA#	120	O/D	**Interrupt A** This signal is asserted low when an interrupt condition as defined in the Interrupt Status Register, Interrupt Mask, and Interrupt Enable registers occurs.
IRDY#	26	S/T/S	**Initiator Ready** As a bus master, this signal will be asserted low when the SiS900 is ready to complete the current data phase transaction. This signal is used in conjunction with the TRDY# signal. Data transaction takes place at the rising edge of PCLK when both IRDY# and TRDY# are asserted low. As a target, this signal indicates that the master has put the data on the bus.
PAR	34	T/S	**Parity** This signal indicates even parity across AD[31-0] and C/BE[3-0]# including the PAR pin. As a master, PAR is asserted during address and write data phases. As a target, PAR is asserted during read data phases.
PCLK	20	I	**PCI Bus Clock** This PCI bus clock provides timing for all bus phases. The rising edge defines the start of each phase. The clock frequency ranges from 0 to 33MHz.
PERR#	32	S/T/S	**Parity Error** The SiS900 as a master or target will assert this signal low to indicated a parity error on any incoming data (except for special cycles). As a bus master, it will monitor this signal on all write operations (except for special cycles).
PME#	65	O/D	**Power Management Event** The SiS900 may asserts PME# only when both PME_En and PME_Status in PMCSR are set. It is de-asserted when PME_En or PME_Status is cleared by software. The SiS900 will assert PME# when it generates or detects an event that requires the system to change its power state. If auxiliary power source exists, PME# can be asserted even when main power is off.
REQ#	122	T/S	**Request** The SiS900 will assert this signal low to request the ownership of the PCI bus to the central arbiter.
RST#	66	I	**Reset** When this signal is asserted all outputs of SiS900 will be tri-stated and the device will be put into a known state.
SERR#	33	O/D	**System Error** This signal is asserted low by SiS900 during address parity errors and system errors if enabled.
STOP#	30	S/T/S	**Stop** This signal is asserted low by the target device to request

			the master device to stop the current transaction.
TRDY#	28	S/T/S	**Target Ready** As a target, this signal will be asserted low when the (slave) device is ready to complete the current data phase transaction. This signal is used in conjunction with the IRDY# signal. Data transaction takes place at the rising edge of PCLK when both IRDY# and TRDY# are asserted low. As a master, this signal indicates that the target is ready for the data during write operation and with the data during read operation.

2.3 Boot ROM/Serial EEPROM Interface

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
PA16	93	I/O	**Boot ROM Address 16** As an output, this pin is for Boot ROM Address 16. PA16-PA0 provides access up to 128K bytes Boot ROM. This pin also acts as hardware trap to enable MAC test mode during power-up stage if pull-up resistor is used in this pin. MAC test mode is for engineering testing only. For normal operation, this pin shall be pulled-down.
PA15	92	I/O	**Boot ROM Address 15** As an output, this pin is for Boot ROM Address 15. At power-up stage, if pull-up resistor is used in this pin, PHY test mode is enabled. PHY test mode is for engineering testing only. For normal operation, this pin shall be pulled-down.
PA14	91	O	**Boot ROM Address 14** In normal mode, this pin is for Boot ROM Address 14.
PA13	90	O	**Boot ROM Address 13** In normal mode, this pin is for Boot ROM Address 13.
PA12	88	O	**Boot ROM Address 12** In normal mode, this pin is for Boot ROM Address 12.
PA11	87	O	**Boot ROM Address 11** In normal mode, this pin is for Boot ROM Address 11.
PA10	86	O	**Boot ROM Address 10** In normal mode, this pin is for Boot ROM Address 10.
PA9	85	O	**Boot ROM Address 9** In normal mode, this pin is for Boot ROM Address 9.
PA8	84	O	**Boot ROM Address 8** In normal mode, this pin is for Boot ROM Address 8.
PA7	83	O	**Boot ROM Address 7** In normal mode, this pin is for Boot ROM Address 7.
PA6 /Auto_Load	79	I/O	**Boot ROM Address 6/Hardware Trap for Enable EEPROM Auto Load Function** As an output, this pin is for Boot ROM Address 6. At power-up stage, if pull-up resistor is used in this pin, auto load EEPROM function is enabled. If pull-down resistor

			is used in this pin, auto load EEPROM function is disabled. For normal operation, this pin shall be pulled-up or pulled-down depend on the need of auto loading EEPROM.
PA5	78	O	**Boot ROM Address 5** In normal mode, this pin is for Boot ROM Address 5.
PA4	77	O	**Boot ROM Address 4** In normal mode, this pin is for Boot ROM Address 4.
PA3	76	O	**Boot ROM Address 3** In normal mode, this pin is for Boot ROM Address 3.
PA2/EEDO	75	O	**Boot ROM Address 2/Serial EEPROM Data Output** This is a multiplexed pin. During Serial EEPROM access, the SiS900 will read the contents of the EEPROM serially through this pin. Require external pull-up resister. During Boot ROM access, it acts as Boot ROM Address 2 output.
PA1/EESK	74	O	**Boot ROM Address 1/Serial EEPROM Clock** This is a multiplexed pin. During Serial EEPROM access, this pin provides the clock for the Serial EEPROM. During Boot ROM access, it acts as Boot ROM Address 1 output.
PA0/EEDI	72	I/O	**Boot ROM Address 0/Serial ROM Data In** This is a multiplexed pin. During Serial EEPROM access, the SiS900 will use this pin to serially write op codes, addresses and data into the serial EEPROM. During Boot ROM access, it acts as Boot ROM Address 0 output.
EECS	71	O	**Serial EEPROM Chip Select** This enables the EEPROM during loading of the Ethernet configuration data.
PD[7::0]	102-97, 95, 94	I/O	**Boot ROM Data [7::0]** In normal mode, this group of 4 signals is for Boot ROM Data 7-0.
POE#	68	O	**Boot ROM Output Enable** It is asserted low during read operation of boot device.

2.4 Transmit/Receive Signals

PIN NAME	PINNUMBER	TYPE	DESCRIPTION
TPO+	107	O	**Twisted Pair Transmit Output, Positive.**
TPO-	108	O	**Twisted Pair Transmit Output, Negative.**
TPI+	111	I	**Twisted Pair Receive Input, Positive.**
TPI-	112	I	**Twisted Pair Receive Input, Negative.**
REXT	104	I	**Transmit Current Set** An external resistor connected between this pin and GND will set the output current level for the twisted pair outputs.

OSCIN	103	I	**Clock Oscillator Input** There must be either 25 Mhz crystal between this pin and GND or a 25 Mhz clock applied to this pin. TX_CLK is generated from this input.
PLED3#	117	I/O O.D. Pullup	**Programmable LED Output** The default function of this pin is to be a 100 Mbps Link Detect output. This pin can also be programmed through the MI serial port to indicate other events or by user controlled. This pin can drive an LED from VCC. When programmed as 100 Mbps Link Detect Output (default): 1 = No Detect 0 = 100 Mbps Link Detected
PLED2#	116	I/O O.D. Pullup	**Programmable LED Output** The default function of this pin is to be an Activity Detect output. This pin can also be programmed through the MI serial part to indicate other events or by user controlled. This pin can drive an LED from VCC. When programmed as an Activity Detect Output (default): 1 = No Activity 0 = Transmit or Receive packet Occurred, Hold Low for 100 ms.
PLED1#	115	I/O O.D. Pullup	**Programmable LED Output** The default function of this pin is to be a Full Duplex Detect output. This pin can also be programmed through the MI serial part to indicate other events or by user controlled. This pin can drive an LED from both VCC and GND. When programmed as Full Duplex Detect Output (default). 1 = Half Duplex 0 = Full Duplex
PLED0#	114	I/O O.D. Pullup	**Programmable LED Output** The default function of this pin is to be a 10 Mbps Link Detect output. This pin can also be programmed through the MI serial port to indicate other events or by user controlled. This pin can drive an LED from both VCC and GND. When programmed as 10 Mbps Link Detect Output (default): 1 = No Detect 0 = 10 Mbps Link Detected

2.5 Power Management Signals

PIN NAME	PINNUMBER	TYPE	DESCRIPTION
APS	67	I	**Auxiliary Power Source** This pin indicates the presence of auxiliary power source. When “1” it indicates the presence of auxiliary power source, SiS900 is capable of asserting PME# from D3cold. When “0” it indicates the absence of auxiliary

			power source, SiS900 can't assert PME# from D3cold.
TEST	62	I	**Internal Testing Pin** THIS PIN WILL RESERVE FOR FUTURE TESTING USE. USER CAN TIE THIS PIN LOW TO PREVENT FROM FLOATING.
WAKEUP	61	O	**Wake Up** This pin is a high active power management event indication. The SiS900 will assert WAKEUP when it generates or detects an event, which requires the system to change its power state. It is de-asserted when main power is turned on.

2.6 Power and Ground Pins

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
DVDD	21, 43, 123		Digital supply: +3.3Vdc is required. This power is used for internal logic except sleepless logic and may be from PCI connector pins or 3.3V regulator output from +5Vdc.
DVSS	19, 44, 124		Digital ground.
DVDD_AUX	70, 82		Digital supply: +3.3Vdual is required. This power is used for internal sleepless logic and may be from PCI connector pin A14 or 3.3V regulator output from +5Vdual.
DVSS_AUX	69, 81		Digital ground for internal sleepless logic.
OVDD	8, 16, 27, 35, 45, 53, 128		Digital supply: +3.3Vdc is required.
OVSS	4, 12, 23, 31, 39, 49, 57		Digital ground.
OVDD_AUX	64, 80, 96, 118		Digital supply (sleepless): +3.3Vdual is required.
OVSS_AUX	73, 89		Digital ground (sleepless).
5VDD*	119		Digital supply: +5Vdc is required. This power is from PCI connector pins.
5VDD_AUX*	63		Digital supply: +5Vdual is required. This power is from LAN WAKE-UP header.
AVDD_AUX	109, 110		Analog supply: +3.3Vdual is required.
AVSS_AUX	105, 106, 113		Analog ground.

* These two pins are used for 5V Tolerated I/O buffers in main power plane and dual power plane. For any application that works in pure 3.3 V signaling environments, these two pins can accept +3.3V digital supply.

3. FUNCTIONAL DESCRIPTION

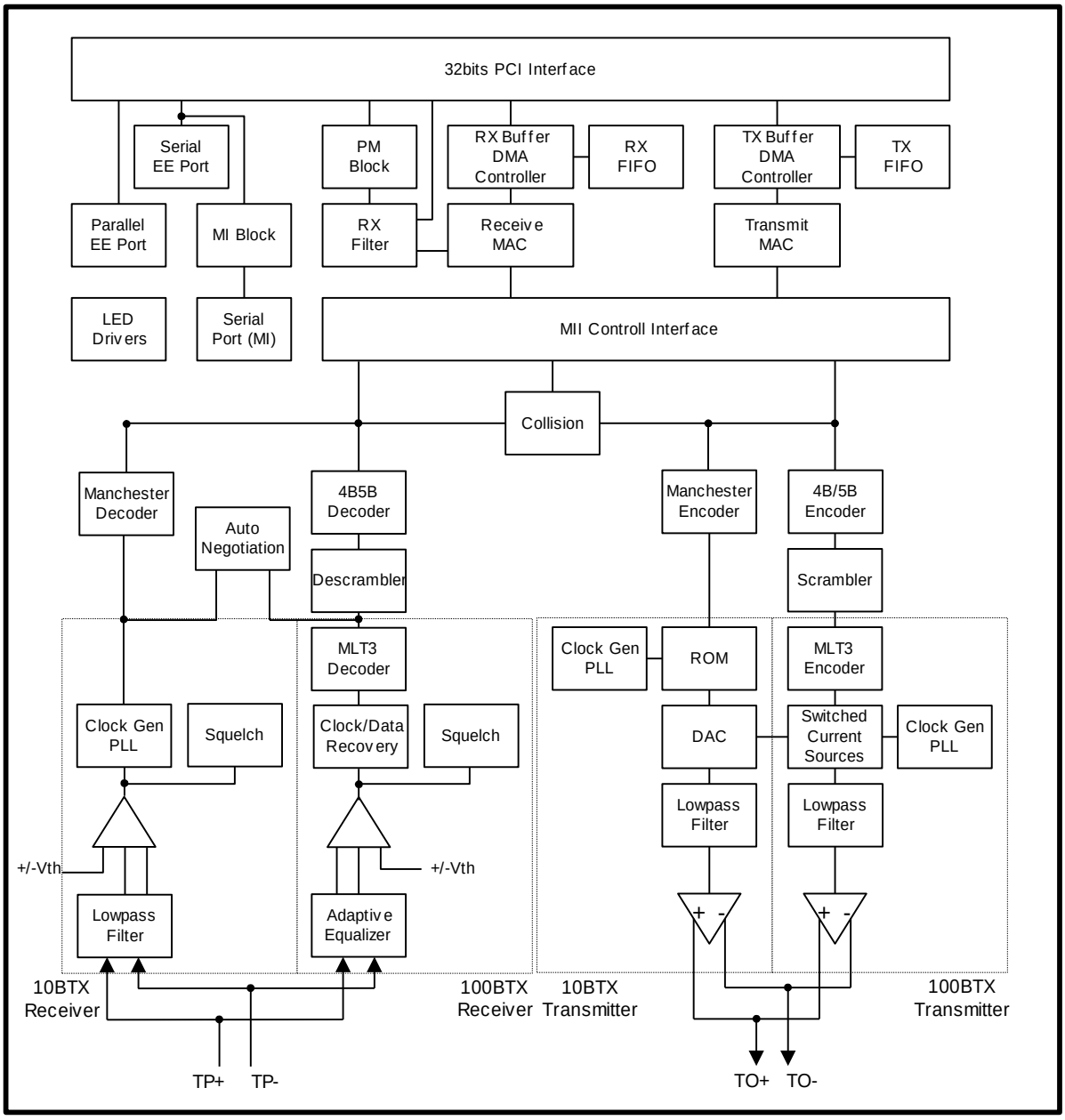


Figure 3-1 SiS900 Functional Block Diagram

3.1 Media Access controller

As a Media Access Controller, SiS900 consists of:

- a PCI bus interface,

- a serial EEPROM interface,
- a Boot ROM interface,
- a buffer management scheme that is simple, efficient and flexible,
- separate receive and transmit FIFOs and DMA controllers,
- a 10/100 Mbps Ethernet Media Access Control (MAC),
- a Media Independent Interface (MII),
- power management block,

Section 3.1 provides a functional overview of the Media Access Controller portion for SiS900.

3.1.1 PCI Bus Interface

SiS900 implements the Peripheral Component Interconnect (PCI) bus interface as defined in PCI Local Bus Specification Version 2.1. When internal registers are being accessed, SiS900 acts as a PCI target (slave). When accessing host memory for descriptor or packet data transfer, SiS900 acts as a PCI bus master. All required pins and functions are implemented. The optional interface pin INTA# for support of interrupt requests is implemented as well. For more information, refer to the PCI Local Bus Specification version 2.1, June 1, 1995.

3.1.1.1 Byte Ordering

SiS900 can be configured to order the bytes of data on the AD[31::0] bus to conform to Little Endian or Big Endian ordering through the use of the OP register offset 04h bit0. Byte ordering only affects bus mastered packet data transfers. Register information remains bit aligned (i.e. AD[31] maps to bit 31 in any register space, AD[0] maps to bit 0, etc.) when registers are accessed with 32-bit operations. Bus mastered transfers of buffer descriptor information also remain bit aligned.

When configured for Little Endian (OP register offset 04h bit0 = 0), the byte orientation for receive and transmit data and descriptors in system memory is as follows:

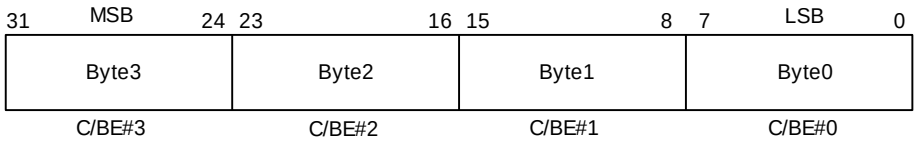


Figure 3-2 Little Endian Byte Ordering

When configured for Big Endian mode (OP register offset 04h bit0 =1), the byte orientation for receive and transmit data and descriptors in system memory is as follows:

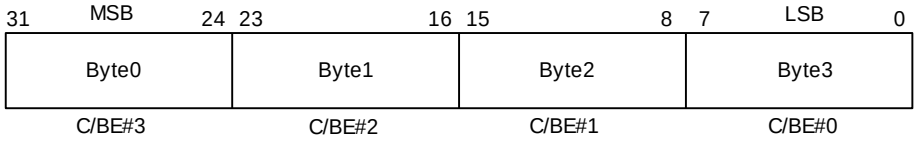


Figure 3-3 Big Endian Byte Ordering

3.1.1.2 Interrupt Control

Interrupts are performed by asynchronously asserting the INTA# pin. This pin is an open drain output. The source of the interrupt can be determined by reading the Interrupt Status Register (ISR) (OP register offset 10h). One or more bits in the ISR will be set, denoting all currently pending interrupts. Reading of the ISR clears ALL bits. Masking of specific interrupts can be accomplished by using the Interrupt Mask Register (IMR) (OP register offset 14h). Assertion of INTA# can be prevented by

clearing the Interrupt Enable bit in the Interrupt Enable Register (OP register offset 18h). This allows the system to defer interrupt processing as needed.

3.1.1.3 Latency Timer

The *Latency Timer* described in CFGLAT:LAT (PCI Configuration Register offset 0Ch) defines the maximum number of bus clocks that the device will hold the bus. Once the device gains control of the bus and issues FRAME#, the Latency Timer will begin counting down. If GNT# is de-asserted before SiS900 has finished with the bus, the device will maintain ownership of the bus until the timer reaches zero (or has finished the bus transfer). The timer is an 8-bit counter, with the lower 4 bits hard-coded to 1111b. This means that the timer value can only be incremented in units of 16 clocks.

3.1.2 Bus Operation

3.1.2.1 Target Read

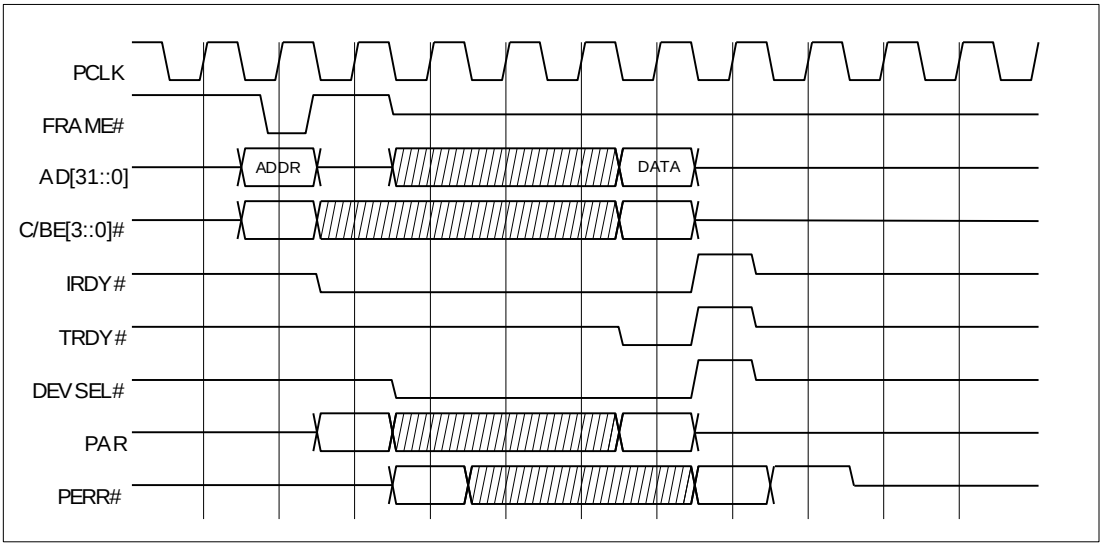


Figure 3-4 Target Read Operation

A Target Read operation starts with the system generating FRAME#, Address, and either an IO read (0010b) or Memory Read (0110b) command. See Figure 3-4. If the 32-bit address on the address bus matches the IO address range specified in CFGIOA:IOBASE (for I/O reads) or the memory address range specified in CFGMA:MEMBASE (for memory reads), SiS900 will generate DEVSEL# 2 clock cycles later (medium speed).

The system must tri-state the Address bus, and convert the C/BE bus to byte enables, after the address cycle. On the 2nd cycle after the assertion of DEVSEL#, all 32-bits of data and TRDY# will become valid. If IRDY# is asserted at that time, TRDY# will be forced HIGH on the next clock for 1 cycle, and then tri-stated.

If FRAME# is asserted beyond the assertion of IRDY#, SiS900 will still make data available as described above, but will also issue a Disconnect. That is, it will assert the STOP# signal with TRDY#. STOP# will remain asserted until FRAME# is detected as de-asserted.

3.1.2.2 Target Write

A Target Write operation starts with the system generating FRAME#, Address, and Command (0011b or 0111b). See Figure 3-5. If the upper 24 bits on the address bus match CFGIOA:IOBASE (for I/O

reads) or CFGMA:MEMBASE (for memory reads), SiS900 will generate DEVSEL# 2 clock cycles later.

On the 2nd cycle after the assertion of DEVSEL#, the device will monitor the IRDY# signal. If IRDY# is asserted at that time, the DP83810 will assert TRDY#. On the next clock the 32-bit double word will be latched in, and TRDY# will be forced HIGH for 1 cycle and then tri-stated.

Note: Target write operations must be 32-bits wide.

If FRAME# is asserted beyond the assertion of IRDY#, SiS900 will still latch the first double word as described above, but will also issue a Disconnect. That is, it will assert the STOP# signal with TRDY#. STOP# will remain asserted until FRAME# is detected as de-asserted.

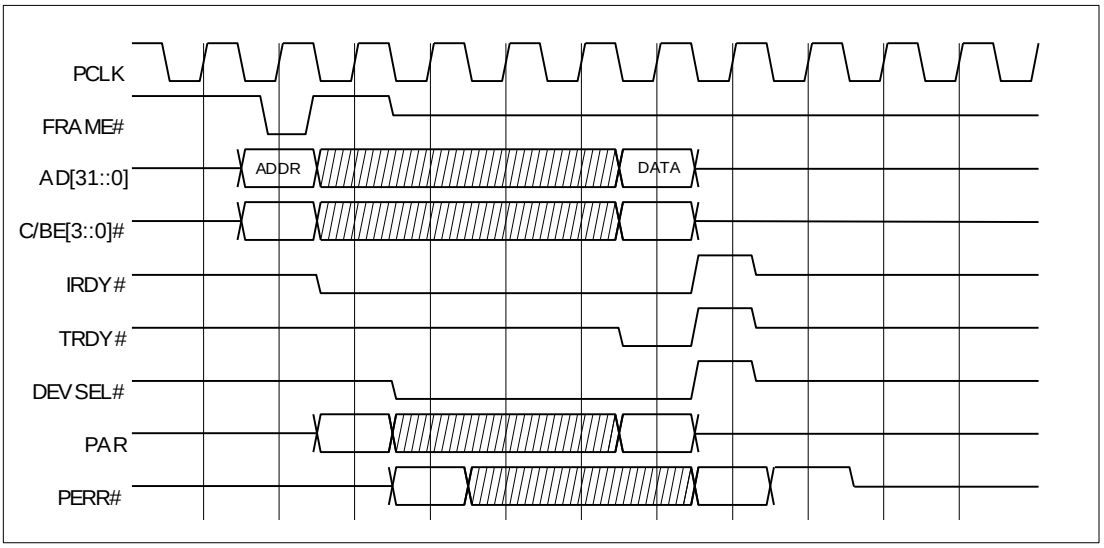


Figure 3-5 Target Write Operation

3.1.2.3 Master Read

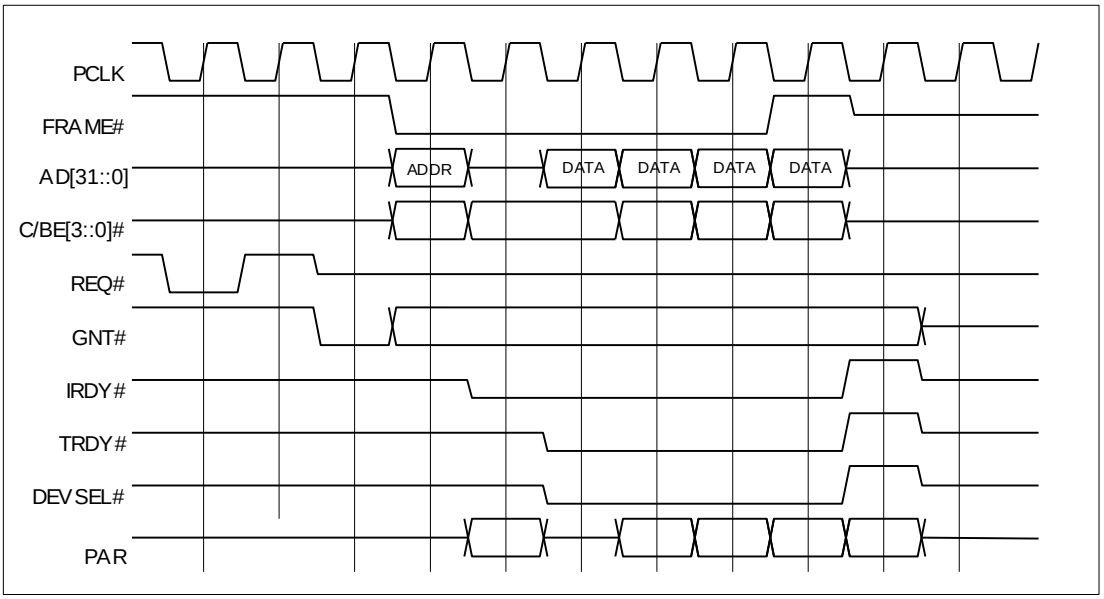
A Master Read operation starts with SiS900 asserting REQ#. See Figure 3-6. If GNT# is asserted within 2 clock cycles, FRAME#, Address, and Command will be generated 2 clocks after REQ# (Address and FRAME# for 1 cycle only). If GNT# is asserted 3 cycles or later, FRAME#, Address, and Command will be generated on the clock following GNT#.

The device will wait for 8 cycles for the assertion of DEVSEL. After 8 clocks without DEVSEL#, the device will issue a Master Abort by asserting FRAME# HIGH for 1 cycle. IRDY# will be forced HIGH on the following cycle. Both signals will become tri-state on the cycle following their de-assertion.

On the clock edge after the generation of Address and Command, the address bus will become tri-state, and the C/BE# bus will contain valid byte enables. On the clock edge after FRAME# was asserted, IRDY# will be asserted (and FRAME# will be de-asserted if this is to be a single read operation). On the clock where both TRDY# and DEVSEL# are detected as asserted, data will be latched in (and the byte enables will change if necessary). This will continue until the cycle following the de-assertion of FRAME#.

On the clock where the second to last read cycle occurs, FRAME# will be forced HIGH (it will be tri-stated 1 cycle later). On the next clock edge that the device detects TRDY# asserted, it will force IRDY# HIGH. It, too, will be tri-stated 1 cycle later. This will conclude the read operation. SiS900 will never force a wait state during a read operation.

Figure 3-6 Master Read Operation



3.1.2.4 Master Write

A Master Write operation starts with SiS900 asserting REQ#. See Figure 3-7. If GNT# is asserted within 2 clock cycles, FRAME#, Address, and Command will be generated 2 clocks after REQ# (Address and FRAME# for 1 cycle only). If GNT# is asserted 3 cycles or later, FRAME#, Address, and Command will be generated on the clock following GNT#.

The device will wait for 8 cycles for the assertion of DEVSEL#. After 8 clocks without DEVSEL#, the device will issue a Master Abort by asserting FRAME# HIGH for 1 cycle. IRDY# will be forced HIGH on the following cycle. Both signals will become tri-state on the cycle following their de-assertion.

On the clock edge after the generation of Address and Command, the data bus will become valid, and the C/BE# bus will contain valid byte enables. On the clock edge after FRAME# was asserted, IRDY# will be asserted (and FRAME# will be de-asserted if this is to be a single read operation). On the clock where both TRDY# and DEVSEL# are detected as asserted, valid data for the next cycle will become available (and the byte enables will change if necessary). This will continue until the cycle following the de-assertion of FRAME#.

On the clock where the second to last write cycle occurs, FRAME# will be forced HIGH (it will be tri-stated 1 cycle later). On the next clock edge that the device detects TRDY# asserted, it will force IRDY# HIGH. It, too, will be tri-stated 1 cycle later. This will conclude the write operation. SiS900 will never force a wait state during a write operation.

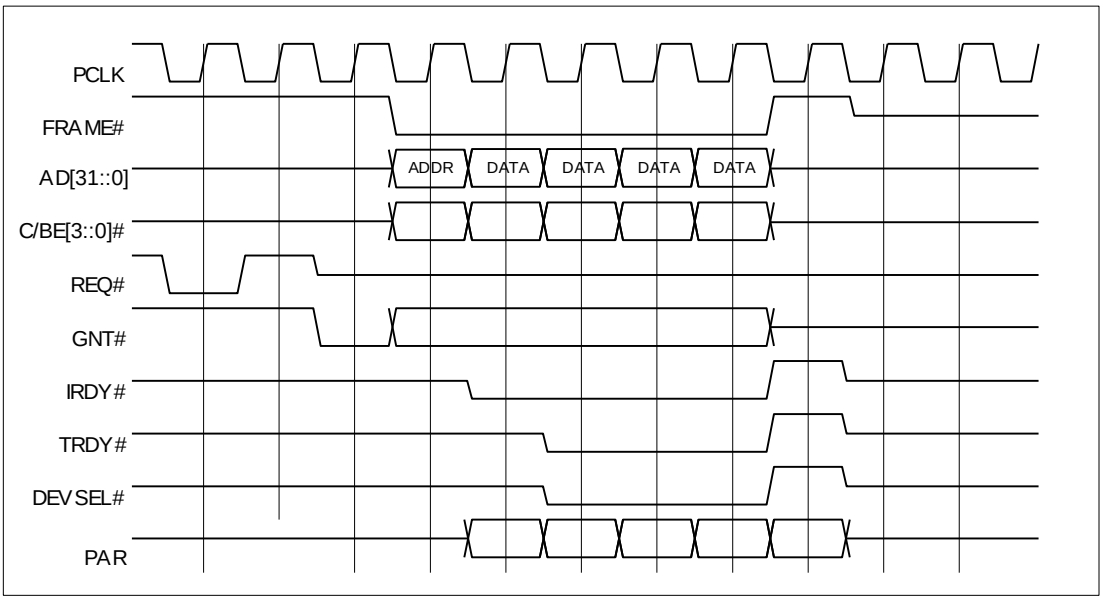


Figure 3-7 Master Write Operation

3.1.2.5 Configuration Access

Configuration register accesses are similar to Target reads and writes in that they are single data word transfers and are initiated by the system. For the system to initiate a Configuration access, it must also generate IDSEL as well as the correct Command (1010b or 1011b) during the Address phase. SiS900 will respond as it does during Target operations.

Note: Configuration reads must be 32-bits wide, but writes may access individual bytes.

3.1.3 Buffer Management

The buffer management scheme used on SiS900 allows quick, simple and efficient use of the frame buffer memory. Frames are saved in similar formats for both transmit and receive. The buffer management scheme also uses separate buffers and descriptors for packet information. This allows effective transfers of data from the receiver buffer to the transmitter buffer by simply transferring the descriptor from the receive queue to the transmit queue.

The format of the descriptors allows the packets to be saved in a number of configurations. A packet can be stored in memory with a single descriptor and a single packet fragment, or multiple descriptors with single fragments. This flexibility allows the user to configure SiS900 to maximize efficiency. Architecture of the specific system's buffer memory, as well as the nature of network traffic, will determine the most suitable configuration of packet descriptors and fragments.

3.1.3.1 Overview

The buffer management design has the following goals:

- simplicity,
- efficient use of the PCI bus (the overhead of the buffer management technique is minimal),
- low CPU utilization,
- flexibility.

Descriptors may be either per-packet or per-packet-fragment. Each descriptor may describe one packet fragment. Receive and transmit descriptors are symmetrical.

3.1.3.1.1 Descriptor Format

SiS900 uses a symmetrical format for transmit and receive descriptors. In bridging and switching applications this symmetry allows software to forward packets by simply moving the list of descriptors that describe a single received packet from the receive list of one MAC to the transmit list of another. Descriptors must be aligned on an even long-word (32-bit) boundary. SiS900 supports a single fragment per descriptor.

Table 3-1 SiS900 Descriptor Format

OFFSET	TAG	DESCRIPTION
0000h	link	32-bit "link" field to the next descriptor in the linked list. Bits 1-0 must be 0, as descriptors must be aligned on 32-bit boundaries.
0004h	cmdsts	32-bit Command/Status Field (bit-encoded)
0008h	bufptr	32-bit pointer to the first fragment or buffer. In transmit descriptors, the buffer can begin on any byte boundary. In receive descriptors, the buffer must be aligned on a 32-bit boundary.

Some of the bit definitions in the CMDSTS field are common to both receive and transmit descriptors:

Table 3-2 CMDSTS Common Bit Definitions

BIT	TAG	DESCRIPTION	USAGE
31	OWN	Descriptor Ownership	Set to 1 by the data producer of the descriptor to transfer ownership to the data consumer of the descriptor. Set to 0 by the data consumer of the descriptor to return ownership to the data producer of the descriptor. For transmit descriptors, the driver is the data producer, and SiS900 is the data consumer. For receive descriptors, SiS900 is the data producer, and the driver is the data consumer.
30	MORE	More descriptors	Set to 1 to indicate that this is NOT the last descriptor in a packet (there are MORE to follow). When 0, this descriptor is the last descriptor in a packet. Completion status bits are only valid when this bit is zero.
29	INTR	Interrupt	Set to 1 by software to request a "descriptor interrupt" when SiS900 transfers the ownership of this descriptor back to software.
28	SUPCRC INCCRC	Suppress CRC / Include CRC	In transmit descriptors, it indicates that CRC should not be appended by SiS900 if this bit is set. On receives, this bit is always set to 0, as the CRC is always copied to the end of the buffer by the hardware.
27	OK	Packet OK	In the last descriptor in a packet, this bit indicates that the packet was either sent or received successfully.
26-16			The usage of these bits differ in receive and transmit descriptors. See below for details.
15-12			(reserved)
11-0	SIZE	Descriptor Byte Count	Set to the size in bytes of the data.

Table 3-3 Transmit Status Bit Definitions

BIT	TAG	DESCRIPTION	USAGE

26	TXA	Transmit Abort	Transmission of this packet was aborted.
25	TFU	Transmit FIFO Underrun	The transmit FIFO was exhausted during the transmission of this packet.
24	CRS	Carrier Sense Lost	Carrier was lost during the transmission of this packet. This condition is not reported if TXCFG:CSI is set.
23	TD	Transmit Deferred	Transmission of this packet was deferred.
22	ED	Excessive Deferral	The length of deferral during the transmission of this packet was excessive (> 3.2ms), indicating transmission failure.
21	OWC	Out of Window Collision	The MAC encountered an "out of window" collision during the transmission of this packet.
20	EC	Excessive Collisions	The number of collisions during the transmission of this packet was excessive, indicating transmission failure.
19-16	CCNT	Collision Count	The number of collisions encountered during the transmission of this packet.

Table 3-4 Receive Status Bit Definitions

BIT	TAG	DESCRIPTION	USAGE
26	RXA	Receive Aborted	Set to 1 by SiS900 when the receive was aborted. If RXO is set, then the receive was aborted due to an RX overrun. If RXO is clear, the a receive descriptor error occurred. SIZE will be set to the amount of data that was transferred to memory when the error was detected.
25	RXO	Receive Overrun	Set to 1 by SiS900 to indicate that a receive overrun condition occurred. RXA will also be set.
24-23	DEST	Destination Class	When the receive filter is enabled, these bits will indicate the destination address class as follows: 00 - Packet was rejected 01 - Destination matched the Receive Filter Node Address Register 10 - Destination is a multicast (but not broadcast) 11 - Destination is a broadcast address If the Receive Filter is enabled, 00 indicates that the packet was rejected. Normally packets that are rejected do not cause any bus activity, nor do they consume receive descriptors. However, this condition could occur if the packet is rejected by the Receive Filter later in the packet than the receive drain threshold (RXCFG:DRTH)
22	LONG	Too Long Packet Received	The size of the receive packet exceeded 1518 bytes.
21	RUNT	Runt Packet Received	The size of the receive packet was smaller than 64 bytes (including CRC).
20	ISE	Invalid Symbol Error	(100Mb only) An invalid symbol was encountered during the reception of this packet.
19	CRCE	CRC Error	The CRC appended to the end of this packet was invalid.
18	FAE	Frame Alignment	The packet did not contain an integral number of

		Error	octets.
17	LBP	Loopback Packet	The packet is the result of a loopback transmission.
16	COL	Collision Activity	The received packet had a collision during reception.

3.1.3.1.2 Single Descriptor Packets

To represent a packet in a single descriptor, the MORE bit in the CMDSTS field is set to 0.

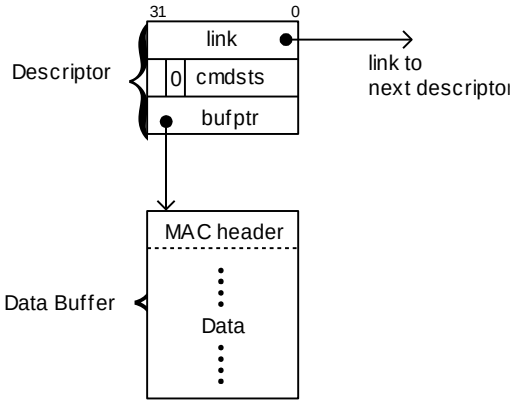


Figure 3-8 Single Descriptor Packets

3.1.3.1.3 Multiple Descriptor Packets

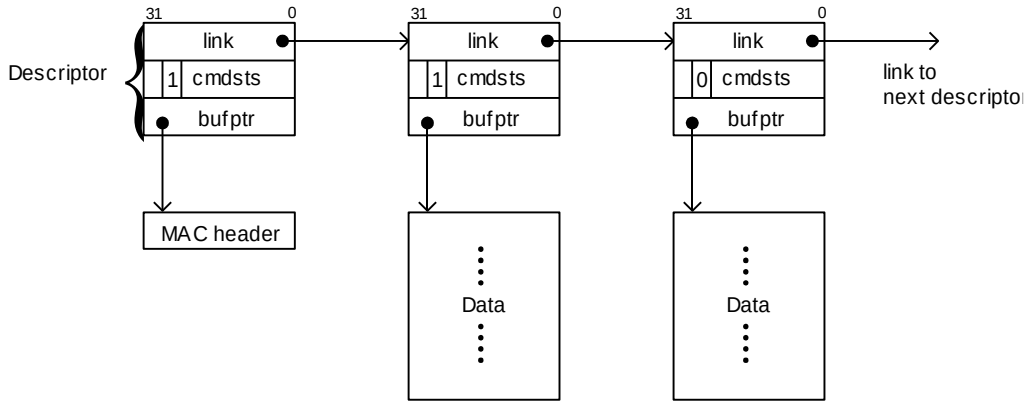


Figure 3-9 Multiple Descriptor Packets

A single packet may also cross descriptor boundaries. This is indicated by setting the MORE bit in all descriptors except the last one in the packet. Ethernet internetworking applications (bridges, switches, routers, etc.) can optimize memory utilization by using a single small buffer per receive descriptor, and allowing SiS900 hardware to use the minimum number of buffers necessary to store an incoming packet.

3.1.3.1.4 Descriptor Lists

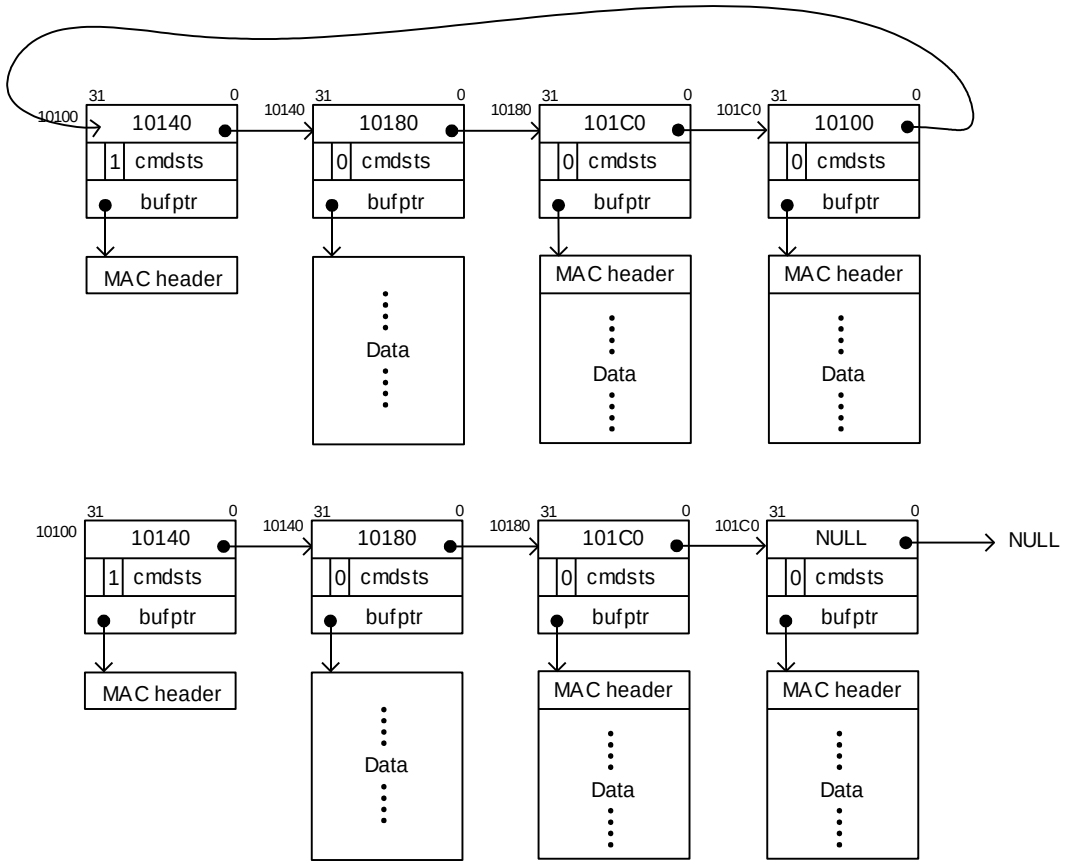


Figure 3-10 Ring and List Descriptor Organization

Descriptors are organized in linked lists using the link field. The system designer may also choose to implement a "ring" of descriptors by linking the last descriptor in the list back to the first. A list of descriptors may represent any number of packets or packet fragments.

3.1.3.2 Transmit Architecture

The following figure illustrates the transmit architecture of SiS900.

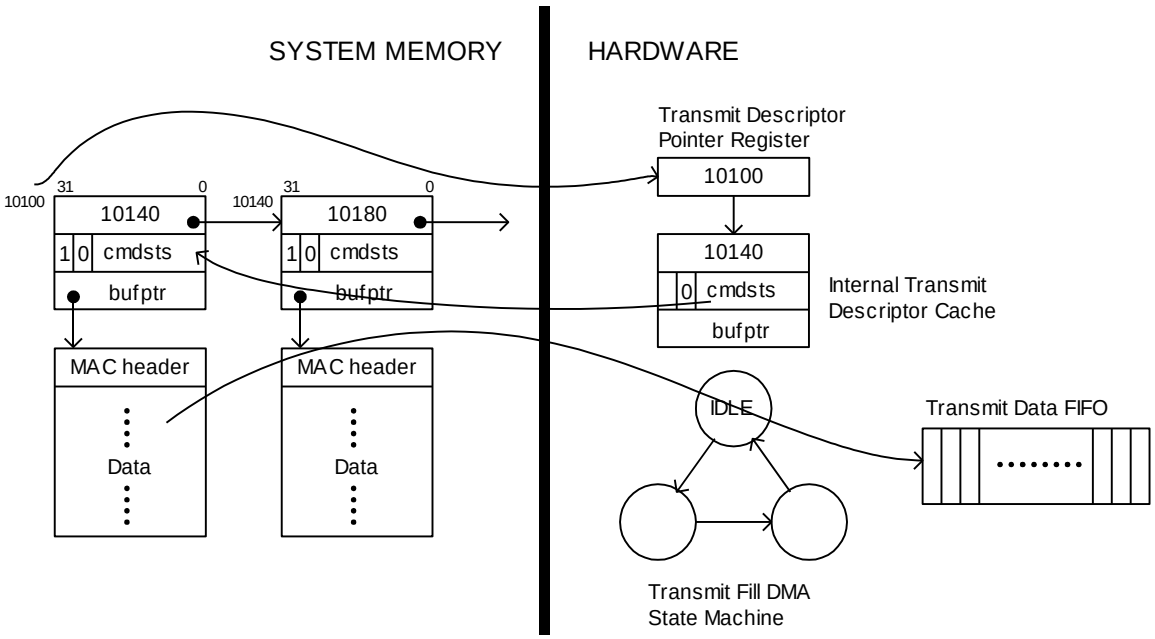


Figure 3-11 Transmit Architecture

When the CR:TXEN(OP register offset 00h bit0) bit is set to 1 (regardless of the current state), and SiS900 Transmit Buffer Manager is idle, then SiS900 will read the contents of the current transmit descriptor into the internal TxDescCache. SiS900 TxDescCache can hold a single fragment pointer/count combination.

3.1.3.2.1 Transmit Data Flow

In SiS900 transmit architecture, packet transmission involves the following steps:

1. The device driver receives packets from an upper layer.
2. An available SiS900 transmit descriptor is allocated. The fragment information is copied from the NOS (Network Operating System) specific data structure(s) to SiS900 transmit descriptor.
3. The driver adds this descriptor to it's internal list of transmit descriptors awaiting transmission. For transmit descriptor the OWN bit shall be set to 1 to show that this descriptor will be transferred to hardware for transmission.
4. If the internal list was empty (this appended descriptor represents the only outstanding transmit packet), then the driver must set the TXDP register (OP register offset 20h) to the address of this descriptor, else the driver will append this descriptor to the end of the list.
5. The driver sets the TXEN bit in the CR register to insure that the Transmit Buffer Manager Fill state machine is active.
6. If idle, the transmit fill state machine reads the descriptor into the TxDescCache which are the internal register to store the current CMDSTS information for process by SiS900.
7. The state machine then moves through the fragment described within the descriptor, filling the TxDataFIFO with data. The hardware handles all aspects of byte alignment; no alignment is assumed. Fragments may start and/or end on any byte address. The transmit fill state machine uses the fragment pointer and the SIZE field from the CMDSTS field of the current descriptor to keep the TxDataFIFO full. It also uses the MORE bit and the SIZE field from the CMDSTS field of the

current descriptor to know when packet boundaries occur.

8. When a packet has completed transmission (either successful or unsuccessful), the state machine updates the CMDSTS field of the current descriptor in main memory (by bus-mastering a single 32-bit word), relinquishing ownership, and indicating the packet completion status. If more than one descriptor was used to describe the packet, then completion status is updated only in the last descriptor. Intermediate descriptors only have the OWN bits modified.
9. If the link field of the descriptor is non-zero, the state machine advances to the next descriptor and continues.
10. If the link field is NULL, the transmit fill state machine suspends, waiting for the TXEN bit in the CR register to be set.

3.1.3.3 Receive Architecture

The receiver architecture is as "symmetrical" to the transmit architecture as possible. The receiver buffer manager prefetches receive descriptors to prepare for incoming packets. When the amount of receive data in the RxDataFIFO is more than the RxDrainThreshold, or the RxDataFIFO contains a complete packet, then the state machine begins filling received buffers in host memory.

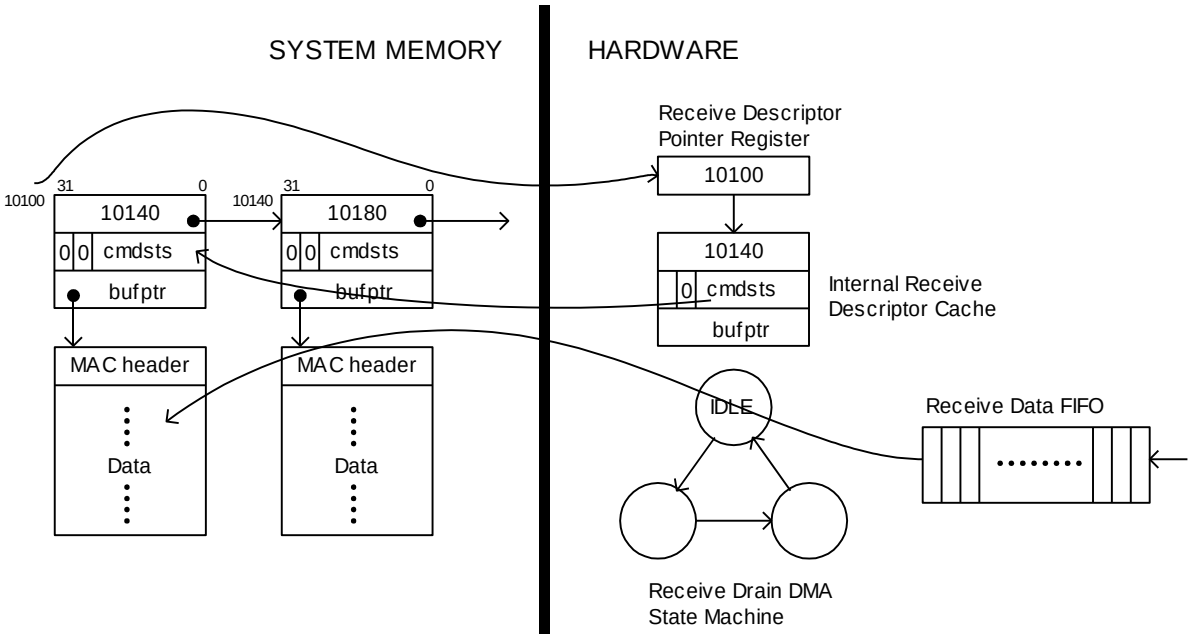


Figure 3-12 Receive Architecture

When the RXEN bit is set to 1 in the CR register (regardless of the current state), and SiS900 receive state machine is idle, then SiS900 will read the contents of the descriptor referenced by RXDP into the Rx Descriptor Cache. The Rx Descriptor Cache allows SiS900 to read an entire descriptor in a single burst, and reduces the number of bus accesses required for fragment information to 1. SiS900 Rx Descriptor Cache holds a single buffer pointer/count combination.

3.1.3.3.1 Receive Data Flow

1. With a bus mastering architecture, some number of buffers and descriptors for received packets must be pre-allocated when SiS900 is initialized. The number allocated will directly affect the system's tolerance to interrupt latency. The more buffers that you pre-allocate, the longer the

system will survive an incoming burst without losing receive packets, if receive descriptor processing is delayed or preempted.

2. Prior to packet reception, receive buffers must be described in a receiver descriptor list (or ring, if preferred). In each descriptor, the driver assigns ownership to the hardware by clearing the OWN bit. Receive descriptors may describe a single buffer.
3. The address of the first descriptor in this list is then written to the RXDP register. As packets arrive, they are placed in available buffers. A single packet may occupy one or more receive descriptors, as required by the application. The device reads in the first descriptor into the RxDescCache, which store the current packet information for processing by the chip.
4. As data arrives in the RXDataFIFO, the receiver buffer management state machine places the data in the receive buffer described by the descriptor. This continues until either the end of packet is reached, or the descriptor byte count for this descriptor is reached.
5. If end of packet was reached, the status in the descriptor (in main memory) is updated by setting the OWN bit and clearing the MORE bit, by updating the receiver status bits as indicated by the MAC, and by updating the SIZE field. The status bits in CMDSTS are only valid in the last descriptor of a packet (with the MORE bit clear). Also for the last descriptor of a packet, the SIZE field will be updated to reflect the actual amount of data written to the buffer (which may be less the full buffer size allocated by the descriptor).
6. If the receive buffer management state machine runs out of descriptors while receiving a packet, data will buffer in the receive FIFO. If the FIFO overflows, the driver will be interrupted with an RxOVR error.

3.1.4 Receive and Transmit FIFOs

SiS900 incorporates 2048-byte Transmit FIFOs and 2048-byte Receive FIFOs for transferring data to/from the system interface and from/to the network. The FIFOs, providing temporary storage of data, free the host system from the real-time demands of the network.

The way in which the FIFOs are emptied and filled is controlled by the FIFO threshold values in the TXCFG and RXCFG registers (OP register offset 24h and 34h). These values determine how full or empty the FIFOs must be before the device requests the bus. Additionally, there is a threshold value that determines how full the transmitter FIFO must be before beginning transmission. Once SiS900 requests the bus, it will attempt to empty or fill the FIFOs as allowed by the respective MXDMA settings in TXCFG and RXCFG.

3.1.4.1 Receive FIFO

To accommodate the different transfer rates, the receiver FIFO serves as a buffer between receive MAC and the system interface. The FIFO is arranged as a 512 by 32-bit (2KB) memory array controlled by three sections of logic. During reception, the MAC interface logic directs dwords of packet data from the MAC into the FIFO. As data enters the FIFO, the Threshold Logic monitors the number of long words transferred. The programmable threshold (OP register offset 34h) determines the number of long words written into the FIFO from the MAC unit before a DMA request for system memory access occurs. When the threshold is reached, the Threshold Logic enables the Buffer Management Engine to read the long words from the FIFO and transfer them to system memory. The transfer to system memory will stop once the data in the FIFO is less than one long word. This process continues until the end of the packet or MXDMA is reached.

3.1.4.2 Transmit FIFO

Similar to the receive FIFO, the transmitter FIFO serves as a buffer between the system interface and the transmit MAC. The transmitter FIFO is also arranged as a 512 by 32-bit (2KB) memory array controlled by three sections of logic. Before the start of transmission, the Buffer Management Engine

fetches data from the system interface, performing byte/dword alignment as necessary, until the FIFO is full or a complete packet has been fetched. The Threshold Logic monitors the number of bytes as they are written into the FIFO. When the drain threshold (OP register offset 24h) has been reached, the MAC Interface Logic begins reading dwords of packet data from the FIFO to provide a data stream for the transmit MAC.

After filling the FIFO, the Buffer Management Engine Threshold Logic monitors the FIFO available space. When this value is greater than or equal to the fill threshold (OP Register offset 24h), the Threshold Logic enables the Buffer Management Engine to fetch more data from memory. This process continues to the end of the packet.

3.1.5 Ethernet Media Access Controller (MAC)

The Media Access Control (MAC) unit performs the control functions for the media access of transmitting and receiving packets over MII. During transmission, the MAC unit sends out nibbles of framing information to the MII, and then reads dwords of packet data from the transmit FIFO, breaking them up into a nibble wide data stream that is sent to the MII interface. During reception, 4-bit wide nibble data comes in from the MII interface, the frame is checked for valid reception, and the data is de-nibblized (packed into 32-bit dwords) and transferred to the receive FIFO. Control and status registers in SiS900 govern the operation of the MAC unit.

The standard 802.3 Ethernet packet consists of the following fields: preamble, start of frame delimiter (SFD), destination address, source address, length, data, and frame check sequence (FCS). All fields are of fixed length except for the data field. During reception, the preamble and SFD are stripped from the incoming packet. During transmission, SiS900 generates and prepends the preamble and SFD. SiS900 normally appends the FCS, but software may disable FCS inclusion on a per-packet basis.

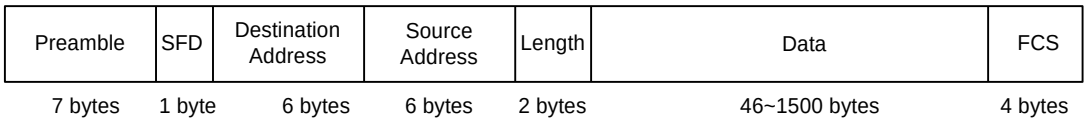


Figure 3-13 IEEE 802.3 Packet Structure

3.1.6 Receive MAC

The receive section controls the MAC receive operations during reception and loop back. During reception, the de-nibblizer goes active after detecting the SFD byte pattern 5Dh (the rest of preamble is ignored). It then transfers the data to the receive FIFO as dwords. Concurrently the 48-bit destination address is processed by the Receive Filter logic. If the Receive Filter Logic indicates that the packet should be accepted, the de-nibblizer passes the remainder of the packet to the receive FIFO. The packet is terminated when the carrier sense signal (CRS) goes inactive. At the end of reception the receive section checks the following:

- Frame alignment errors,
- Symbol errors,
- CRC errors,
- Length errors (runts or jabbers).

The appropriate status is indicated in the CMDSTS field of the receive descriptor. In loop back operations, the receive section operates the same as during normal reception.

The receive section consists of the following basic functional blocks:

- Receive State Machine (RSM),

- Receive Logic,
- De-nibblizer,
- Cyclical Redundancy Checker (CRC),
- Receive Filter,
- Flow Control.

3.1.6.1 Receive State Machine (RSM)

The RSM insures the proper sequencing for normal reception and self-reception during transmission. When the network is inactive, the RSM remains in an idle state continually monitoring for network activity. If the network becomes active, the RSM allows the de-nibblizer to write data into the receive FIFO. During this state, the following conditions may prevent the complete reception of the packet:

FIFO Overrun	The receiver FIFO has been completely filled before SiS900 could transfer the data to memory.
Rx Filter Reject	The packet is rejected because the destination address was not configured for reception in the Receive Filter.
Collision or Other Error	A collision occurred on the network or some other error, such as a CRC error occurred (this is true if SiS900 has been told to reject packets on a collision, or reject packets with errors).

If these conditions do not occur, the RSM processes the packet indicating the appropriate status in the descriptors' CMDSTS field.

3.1.6.2 Receive Logic

The receiver logic contains the command, control, and status registers that govern the operations of the receive section. It generates the control signals for writing data to the receive FIFO, processes error signals obtained from the CRC checker and the de-nibblizer, activates the "packet reject" signal to the RSM for rejecting packets, and posts the applicable status in the Receive Status Register.

3.1.6.3 De-nibblizer

This section gathers the nibble input data stream into 32-bit long words. It also synchronizes the CRC checker to begin operation (after the SFD is detected), and checks for proper FRAME# alignment with respect to CRS going inactive at the end of reception.

3.1.6.4 CRC Checker

The CRC checker calculates the 4-byte Frame Check Sequence (FCS) field from the incoming data stream and compares it with the last 4 bytes of the received packet. The polynomial used for all CRC calculations is

$$x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1.$$

3.1.6.5 Receive Filter

The Receive Filter logic is used to qualify incoming packets based on destination address. Refer to OP register RFCR and RFDR (offset 48h and 4Ch) for details.

3.1.7 Transmit MAC

The transmit section is responsible for reading data from the transmit FIFO and transmitting a serial data stream onto the network in conformance with the IEEE 802.3 Carrier Sense Multiple Access with Collision Detection (CSMA/CD) standard.

The transmit section consists of the following blocks:

- Transmit State Machine,
- Protocol State Machine,
- Serializer,
- Preamble Generator,
- CRC Generator,
- Jam Generator.

3.1.7.1 Transmit State Machine (TSM)

The TSM controls the functions of the serializer, preamble generator, and Jam generator. It determines the proper sequence of events that the transmitter follows under various network conditions. If no collision occurs, the transmitter prefixes a 7-byte preamble and 1 byte SFD at the beginning of each packet and then sends the nibblized data. At the end of the packet, an optional 4-byte CRC pattern is appended as the FCS. If a collision occurs, the transmitter switches from transmitting data to sending a 4-byte Jam pattern to notify all nodes that a collision has occurred. Should the collision occur during the preamble, the transmitter waits for it to complete before jamming. After the transmission has completed, the transmitter writes the status to the transmitter descriptor's CMDSTS field.

3.1.7.2 Protocol State Machine

The protocol state machine assures that SiS900 obeys the CSMA/CD protocol. Before transmitting, this state machine monitors the carrier sense and collision signals for network activity. If any other nodes are currently transmitting, SiS900 defers its transmission until the network is quiet. It then transmits after its Interframe Gap Timer (96 bit times) has expired. The Interframe Gap time is divided into two portions. During the first 64 bit times, any new network activity will restart the Interframe Gap Timer. Beyond this time, however, network activity is ignored and the state machine waits the remaining 32 bit times before transmitting. If SiS900 experiences a collision during a transmission, it switches from transmitting data to transmitting a 4-byte Jam pattern (4 bytes of 0101 each) before ceasing to transmit. SiS900 then waits a random number of slot times, as determined by the Truncated Binary Exponential Backoff Algorithm before attempting the transmission again. In this algorithm, the number of slot times to delay before the nth retransmission is chosen to be a random integer r in the range of:

$$0 <= r <= 2^k$$

where k = min(n,10)

If a collision occurs on the 16th transmit attempt, SiS900 aborts transmitting the packet and reports an "Excessive Collisions" error in the transmit descriptor's CMDSTS field.

3.1.7.3 Preamble Generator

The preamble generator prefixes a 60-bit alternating "1,0" pattern and a 4-bit 1011b SFD pattern at the beginning of each packet. This allows receiving nodes to synchronize to the incoming data. The preamble is always transmitted in its entirety even in the event of a collision. This assures that the minimum collision fragment is 96 bits (64 bits of normal preamble, and 4 bytes, or 32-bits of Jam pattern).

3.1.7.4 CRC Generator

The CRC generator calculates the 4 byte FCS field from the transmitted serial data stream. If enabled, the 4-byte FCS field is appended to the end of the transmitted packet.

For bridging or switched Ethernet applications, setting the SUPCRC bit in the Command/Status field in the Transmit Descriptor can inhibit the CRC Generator. This feature is used when an Ethernet segment has already received a packet with a CRC appended and needs to forward it to another Ethernet segment.

3.1.7.5 Jam Generator

The Jam generator produces a 4 byte pattern of 0101 each to assure that all nodes on the network sense the collision. When a collision occurs, SiS900 stops transmitting data and enables the Jam generator. If a collision occurs during the preamble, SiS900 finishes transmitting the preamble before enabling the Jam generator (See Preamble Generator above).

3.1.8 Flow Control

SiS900 supports IEEE 802.3x flow control. The PAUSE frame detection logic operates based on the Flow Control Register (OP register FLOWCTL offset 38h). If the Flow Control Enable bit is set to enable, SiS900 will detect the incoming PAUSE frame. If a PAUSE frame is recognized, the transmission will be paused for the period which PAUSE frame parameter specifies.

3.1.9 Full Duplex Operation

Full duplex operation is the simultaneous transmission and reception of packet data. This mode of operation is not within the IEEE 802.3 CSMA/CD specification in that receive activity (CRS) is ignored in the decision making process for transmission. During reception, collisions are also ignored.

To configure SiS900 to operate in full duplex, set TXCFG:CSI and TXCFG:HBI=1, and RXCFG:ATX = 1.

3.1.10 MI Registers Access

SiS900 internally provides MII management interface to communicate with MII PHY registers. The MII management interface utilizes a communication protocol similar to a serial EEPROM. This protocol provides capability for addressing up to 32 individual Physical Media Dependent (PMD) devices, which share the same serial interface, and for addressing up to 32 16-bit read/write registers within each PMD. The MII management protocol utilizes following frame format: start bits (SB), opcode (OP), PMD address (PA), register address (RA), line turnaround (LT) and data (See Figure 3-14).

Start Bits	Opcode	PMD Address	Register Address	Line Turn Around	Data
2 bits	2 bits	5 bits	5 bits	2 bits	16bits

Figure 3-14 MII Frame Format

- Start bits are defined as <01>.
- Opcode bits are defined as <01> for a Write access and <10> for a Read access.
- PMD address is the device address.
- Register address is address of the register within that device.
- Line turnaround bits will be <10> for Write accesses and will be <XX> for Read accesses. This allows time for the MII lines to “turn around”.
- Data is the 16 bits of data that will be written to or read from the PMD device.

The Enhanced PHY Access Register (OP register, offset 1ch) is used to provide access to the internal serial MII. Refer to Section 4.3.8 for complete details of the ENPHY.

3.1.11 Auto Load Operation

SiS900 supports the attachment of an external serial EEPROM. The serial EEPROM stores configuration data for SiS900. The EEPROM map is as shown in Appendix A. SiS900 performs an automatic read of 22 bytes of the EEPROM data after the auxiliary power up reset de-asserts if the auto load function is enabled. The auto load function is enabled by pulling-up PA6/Auto_Load pin and signing the signature field of EEPROM to 0900h. The auto load function can be disabled by pulling-down PA6/Auto_Load pin and if disabled, all data will use the default values

The auto load of PMC is for PCI Bus Power Management Interface Spec. revision 1.0a. If auto load function is enabled and bit 2 of EEPROM mask is 1, the PMC will be loaded to CFGPMC.

The auto load of Ethernet ID is for auxiliary power up Magic Packet™ wake up. If auto load function is enabled and bit 3 of EEPROM mask is 1, the auxiliary power on Magic Packet™ wake up feature is enabled and the MAC address is loaded from ethernet ID field of EEPROM.

During the auto load period, if BIOS begins to configure SiS900, all configuration cycles will be retried until auto load has completed.

3.1.12 Reset Operation

SiS900 enters the hardware reset state if the RST# pin is held low for a minimum of 8 consecutive PCI clock cycles. It leaves the hardware reset state if the RST# pin is held high for a minimum of 8 consecutive PCI clock cycles. This is done to prevent glitches from causing the device to go into or out of reset condition inadvertently.

3.1.13 Power Management

SiS900 supports ACPI specification, Network Device Power Management and PCI Power Management Specification.

3.1.13.1 SiS900 Device Power States

SiS900 supports the following power states:

SIS900 DEVICE STATE	AUX POWER PRESENT	ACTIONS TO FUNCTION FROM PCI	ACTIONS FROM FUNCTION
D0	Don't Care	Any PCI Transaction	Any PCI Transaction or Interrupt
D1	Don't Care	PCI Configuration Cycle	PME# only
D2	Don't Care	PCI Configuration Cycle	PME# only
D3hot	Don't Care	PCI Configuration Cycle if PCI Clock exists	PME# only
D3cold	Yes	PCI RST#	PME# only
D3cold	No	PCI RST#	None

3.1.13.2 SiS900 Wake-up Events

Three wake-up events including Link State change, Wake-up Frame received, Magic Packet™ received are supported in SiS900 and each can be enabled and disabled individually for waking up the system.

3.1.13.3 Link State Change Detected Event

Link state change includes link connect and disconnect. If this link state change event and PME_En bit are enabled, PME# will be generated when link state changes.

3.1.13.4 Wake-up Frame Received Event

SiS900 allows wake-up frames defined by the OS for waking up the system. Before enters the wake-up state, the OS passes a list of wake-up sample frames and byte masks to driver. Driver programs SiS900 registers according to the list. If both wake-up frame match bit and PME_En bit are enabled, PME# will be generated when the incoming frame matches the wake-up sample frame. SiS900 can accept three wake-up frames for packet matching simultaneously.

3.1.13.5 Magic Packet Received Event

If both Magic Packet™ match bit and PME_En bit are enabled, PME# will be generated when SiS900 receives a Magic Packet™.

3.2 Physical Layer Entity

SiS900 Physical Layer Entity has ten main functional blocks: controller interface, encoder, decoder, scrambler, descrambler, clock and data recovery, twisted pair transmitter, twisted pair receiver, MI serial port and Auto Negotiation. A block diagram is shown in Figure 3-1.

SiS900 can operate as a 100BaseTX device (hereafter referred to as 100 Mbps mode) or as a 10BaseT device (hereafter referred to as 10 Mbps mode). The difference between the 100 Mbps mode and 10 Mbps mode is data rate, signaling protocol, and allowed wiring. The 100 Mbps mode uses two pairs of category 5 or better UTP or STP twisted pair cable with 4B5B encoded, scrambled, and MLT-3 coded 62.5 MHz ternary data to achieve a throughput 100 Mbps. The 10 Mbps mode uses two pairs of category 3 or better UTP or STP twisted pair cable with Manchester encoded, 10 Mhz binary data to achieve a 10Mbps throughput. The data symbol format on the twisted pair cable for the 100 and 10 Mbps mode are defined in IEEE 802.3 specifications.

On the transmit side for 100 Mbps operation, data is received on the controller interface from SiS900 internal Ethernet controller per the format shown in Figure 3-15. The data is then sent to the 4B5B encoder for formatting. The encoded data is then sent to the scrambler. The scrambled and encoded data is then sent to the TP transmitter. The TP transmitter converts the encoded and scrambled data into MLT-3 ternary format, preshapes the output, and drives the twisted pair cable.

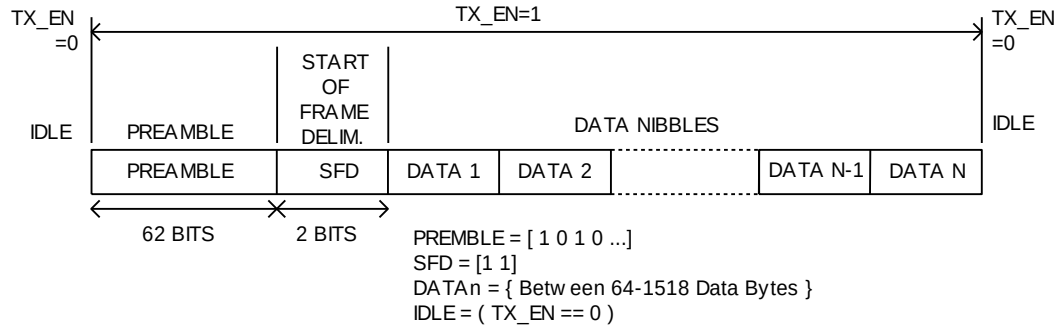
On the receive side for 100 Mbps operation, the twisted pair receiver receives incoming encoded and scrambled MLT3 data from the twisted pair cable, remove any high frequency noise, equalizes the input signal to compensate for the effects of the cable, qualifies the data with a squelch algorithm, and converts the data from MLT-3 coded twisted pair levels to internal digital levels. The output of the twisted pair receiver then goes to a clock and data recovery block which recovers a clock from the incoming data, uses the clock to latch in valid data into the device, and converts the data back to NRZ format. The NRZ data is then unscrambled and decoded by the 4B5B decoder and descrambler, respectively, and outputted to SiS900 internal Ethernet controller by the MI controller interface.

10 Mbps operation is similar to the 100 Mbps operation except, (1) there is no scrambler/descrambler, (2) the encoder/decoder is Manchester instead of 4B5B, (3) the data rate is 10 Mbps instead of 100 Mbps, and (4) the twisted pair symbol data is two level Manchester instead of ternary MLT-3.

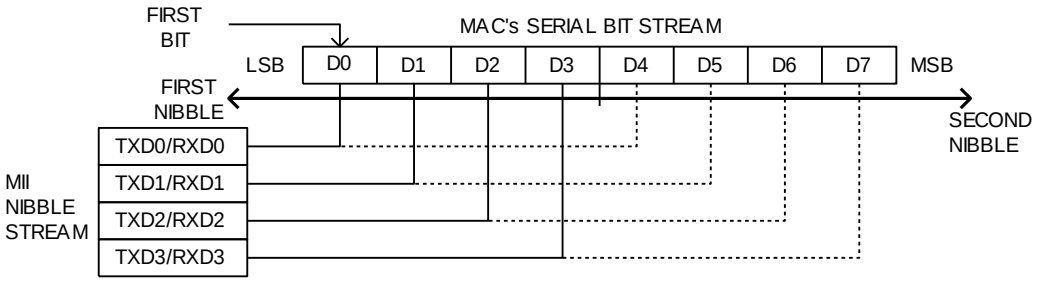
The AutoNegotiation block automatically configures the device for either 100Base-TX or 10Base-T, and for either Full or Half Duplex. This configuration is based on the capabilities selected for this device and the capabilities detected from a remote device.

The Management interface, (hereafter referred to as the MI serial port), is a two pin bi-directional link through which configuration inputs can be set and status outputs can be read.

Each block plus the operating modes are described in more detail in the following sections. Since SiS900 can operate either as a 100Base-TX or a 10Base-T device, each of the following sections describes the performance of the respective section in both the 100 and 10 Mbps modes.



a.) MII Frame Format



b.) MII Nibble Order

SIGNALS	BIT VALUE																		
TXDO	X	X	1[1]	1	1	1	1	1	1	1	1	1	1	1	1	1	1[2]	1	D0[3]	D4[4]
TXD1	X	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	D1	D5
TXD2	X	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	D2	D6
TXD3	X	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	D3	D7
TX_EN	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

1. 1st PREAMBLE nibble transmitted
2. 1st SFD nibble transmitted
3. 1st Data nibble transmitted
4. D0 thru D7 are the first 8 bits of the data field

c.) Transmit Preamble and SFD Bits

SIGNALS	BIT VALUE																		
RXDO	X	X	1[1]	1	1	1	1	1	1	1	1	1	1	1	1	1	1[2]	1	D0[3]	D4[4]
RXD1	X	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	D1	D5
RXD2	X	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	D2	D6
RXD3	X	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	D3	D7
RX_DV	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

1. 1st PREAMBLE receiced. Depending on mode, device may eliminate either all or some of the PREAMBLE nibbles, up to 1st SFD nibble.
2. 1st SFD nibble received
3. 1st Data nibble received
4. D0 thru D7 are the first 8 bits of the data field

d.) Receive Preamble and SFD Bits

Figure 3-15 MII Frame Format

3.2.1 Media Independent Interface

3.2.1.1 MII - 100 Mbps

The MII is a nibble wide packet data interface defined in IEEE 802.3 and shown in Figure 3-15. The internal communication between SiS900 media access controller and SiS 900 physical layer entity follows the MII requirements outlined in IEEE 802.3. The MII frame format is also shown in Figure 3-15.

The MII consists of seventeen signals: four transmit data bits (TXD[3::0]), transmit clock (TX_CLK), transmit enable (TX_EN), four receive data bits (RXD[3::0]), receive clock (RX_CLK), carrier sense (CRS), receive data valid (RX_DV), receive data error (RX_ER), and collision (COL). The transmit and receive clock operate at 25 MHz in 100 Mbps mode.

On the transmit side, the TX_CLK output runs continuously at 25Mhz. When no data is to be transmitted, TX_EN has to be deasserted. While TX_EN is deasserted, TXD[3::0] are ignored and no data is clocked into the physical entity. When TX_EN is asserted on the rising edge of TX_CLK, data on TXD[3:0] is clocked into the physical entity on the rising edges of the TX_CLK output clock, TXD[3::0] input data is nibble wide packet data whose format needs to be the same as specified in IEEE 802.3 and shown in Figure 3-15. When all data on TXD[3::0] has been latched into the physical entity, TX_EN has to be deasserted on the rising edge of TX_CLK.

Since OSCIN input clock generates the TX_CLK output clock, TXD[3::0], and TX_EN are also clocked in on rising edges of OSCIN.

On the receive side, as long as a valid data packet is not detected, CRS and RX_DV are deasserted and RXD[3::0] is held low. When the start of packet is detected, CRS and RX_DV are asserted on falling edge of RX_CLK. The assertion of RX_DV indicates that valid data is clocked out on RXD[3::0] on falling edges of the RX_CLK clock. The RXD[3::0] data has the same frame structure as the TXD[3::0] data and is specified in IEEE 802.3 and shown in Figure 3-15. When the end of packet is detected, CRS and RX_DV are deasserted, and RXD[3::0] is held low. CRS and RX_DV also stay deasserted if the device is in the Link Fail State.

RX_ER is a receive error output which is asserted when certain errors are detected on a data nibble. RX_ER is asserted on the falling edge of RX_CLK for the duration of that RX_CLK clock cycle during which the nibble containing the error is being outputted on RXD[3::0].

The collision output, COL, is asserted whenever the collision condition is detected.

3.2.1.2 MII - 10 Mbps

10 Mbps operation is identical to the 100 Mbps operation except, (1) TX_CLK and RX_CLK clock frequency is reduced to 2.5 MHz, (2) RX_ER is disabled and always held low, and (3) receive operation is modified as follows: On the receive side, when the squelch circuit determines that invalid data is present on the TP inputs, the receiver is idle. During idle, RX_CLK follows TX_CLK, RXD[3::0] is held low and CRS and RX_DV are deasserted. When a start of packet is detected on the TP receive inputs, CRS is asserted and the clock recovery process starts on the incoming TP input data. After the receive clock has been recovered from the data, the RX_CLK is switched over to the recovered clock and the data valid signal RX_DV is asserted on a falling edge of RX_CLK. Once RX_DV is asserted, valid data is clocked out on RXD[3::0] on falling edges of the RX_ CLK clock. The RXD[3::0] data has the same packet structure as the TXD[3::0] data and is formatted on RXD[3::0] as specified in IEEE 802.3 and shown in Figure 3-15. When the end of packet is detected, CRS and RX_DV are deasserted. CRS and RX_DV also stay deasserted as long as the device is in the Link Fail State.

3.2.2 Encoder

3.2.2.1 4B5B Encoder - 100 Mbps

100Base-TX requires that the data be 4B5B encoded. 4B5B coding converts the 4-Bit data nibbles into 5-Bit data code words. The mapping of the 4B nibbles to the 5B code words is specified in IEEE 802.3 and shown in Table 3-5. The 4B5B encoder on SiS900 takes 4B nibbles convert to 5B words according to Table 3-5, and sends the 5B words to the scrambler. The 4B5B encoder also substitutes the first 8 bits of the preamble with the SSD delimiters (a.k.a /J/K/ symbols) and adds an ESD delimiter (a.k.a /T/R/ symbols) to the end of every packet, as defined in IEEE 802.3 and shown in Figure 3-16. The 4B5B encoder also fills the period between packets, called the idle period, with a continuous stream of idle symbols, as shown in Figure 3-16.

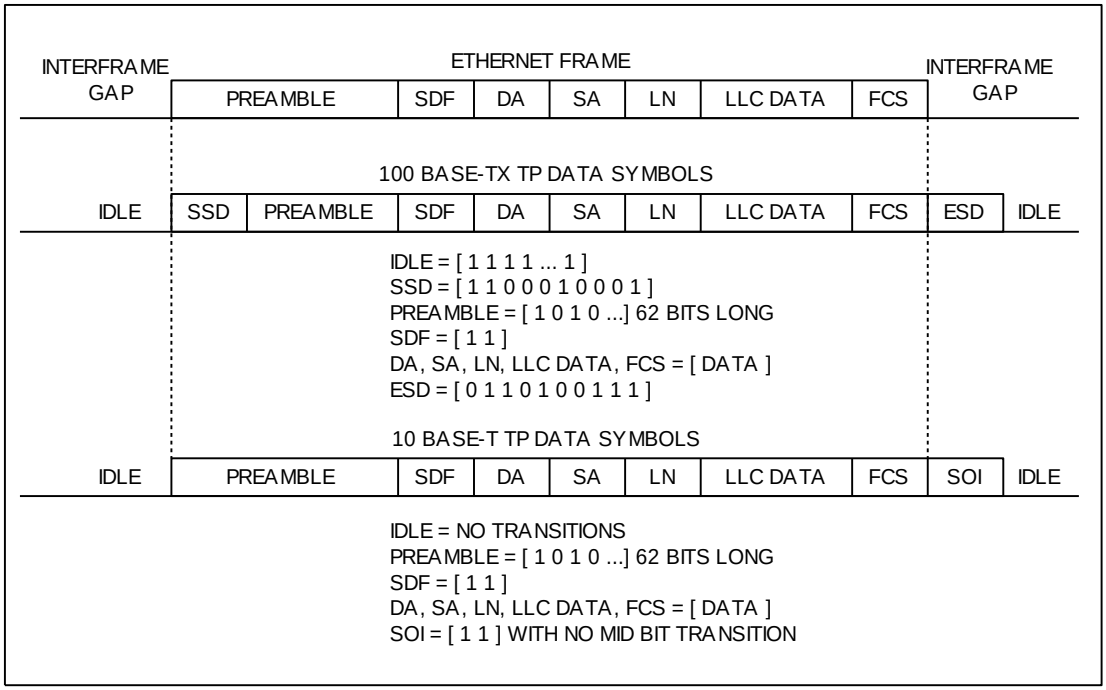


Figure 3-16 Twisted Pair Frame Format

3.2.2.2 Manchester Encoder - 10 Mbps

The Manchester encoding process combines clock and NRZ data such that the first half of the data bit contains the complement of the data, and the second half of the data bit contains the true data, as specified in IEEE 802.3. This guarantees that a transition always occurs in the middle of the bit cell. The Manchester encoder on SiS900 converts the 10 Mbps NRZ data from the controller interface into a Manchester Encoded data stream for the TP transmitter and adds a start of idle pulse (SOI) at the end of the packet as specified in IEEE 802.3 and shown in Figure 3.2-2. Manchester encoding of the NRZ data occurs only when TX_EN is asserted.

Table 3-5 4B/5B Symbol Mapping

SYMBOL NAME	DESCRIPTION	5B CODE	4B CODE
0	Data 0	11110	0000
1	Data 1	01001	0001
2	Data 2	10100	0010
3	Data 3	10101	0011
4	Data 4	01010	0100
5	Data 5	01011	0101
6	Data 6	01110	0110
7	Data 7	01111	0111
8	Data 8	10010	1000
9	Data 9	10011	1001
A	Data A	10110	1010
B	Data B	10111	1011
C	Data C	11010	1100
D	Data D	11011	1101
E	Data E	11100	1110
F	Data F	11101	1111
I	Idle	11111	0000
J	SSD #1	11000	0101
K	SSD #2	10001	0101
T	ESD #1	01101	0000
R	ESD #2	00111	0000
H	Halt	001 00	Undefined
--	Invalid codes	All others*	0000*

*These 5B codes are not used. For decoder, these 5B codes are decoded to 4B 0000. For encoder, 4B 0000 is encoded to 5B 11110, as shown in symbol Data 0.

3.2.3 Decoder

3.2.3.1 4B5B Decoder - 100 Mbps

Since the TP input data is 4B5B encoded on the transmit side, it must also be decoded by the 4B5B decoder on the receive side. The mapping of the 5B nibbles to the 4B code words is specified in IEEE 802.3 and shown in Table 3-5. The 4B5B decoder on SiS900 takes the 5B code words from the descrambler, converts them into 4B nibbles per Table 3-5. The 4B5B decoder also strips off the SSD delimiter (a.k.a./J/K/symbols) and replaces them with two 4B Data 5 nibbles (a.k.a/5/symbol), and strips off the ESD delimiter (a.k.a/T/R/symbols) and replaces it with two 4B Data 0 nibbles (a.k.a/I/symbol), per IEEE 802.3 specifications and shown in Figure 3-16.

The 4B5B decoder detects SSD, ESD and, codeword errors in the incoming data stream as specified in IEEE 802.3. These errors are indicated by asserting RX_ER output while the errors are being transmitted across RXD[3::0], and they are also indicated in the MI Register by setting SSD, ESD, and codeword error bits in the MI Status Output register.

3.2.3.2 Manchester Decoder - 10 Mbps

In Manchester coded data, the first half of the data bit contains the complement of the data, and the second half of the data bit contains the true data. The Manchester decoder in SiS900 converts the Manchester encoded data stream from the TP receiver into NRZ data for the controller interface by decoding the data and stripping off the SOI pulse. Since the clock and data recovery block has already separated the clock and data from the TP receiver, the Manchester decoding process to NRZ data is inherently performed by that block.

3.2.4 Clock and Data Recovery

3.2.4.1 Clock Recovery - 100 Mbps

Clock recovery is done with a PLL. If there is no valid data present on the TP inputs, the PLL is locked to the 25 MHz TX_CLK. When valid data is detected on the TP inputs with the squelch circuit and when the adaptive equalizer has settled, the PLL input is switched to the incoming data on the TP input. The PLL then recovers a clock by locking onto the transitions of the incoming signal from the twisted pair wire. The recovered data clock frequency is 125 MHz and is divided down to produce a 25 MHz clock that is sent to the controller interface signal RX_CLK. The PLL can reliably perform the clock and data recovery process with up to +/-3 ns or jitter on the TP input.

SiS900 has an internal PLL watchdog timer that monitors the receiver PLL output frequency. If the receive PLL output frequency deviates from the TX_CLK frequency by more that 3% over a 8 us interval, the device assumes that the receive PLL has not locked onto the TP input data properly and the PLL is reset. The PLL is reset by switching its input from the TP input data to the TX_CLK for a period of 200 us to retrain it to the 25 MHz frequency from the oscillator.

3.2.4.2 Data Recovery - 100 Mbps

Data recovery is performed by latching in valid data from the TP receiver with the recovered clock extracted by the PLL. When invalid data is detected on the TP input, the receive data is held low. When valid data is detected on the TP inputs, the clock recovery block extracts a 125 MHz clock from the data stream from the TP receiver. This 125 MHz recovered clock is then used to latch in valid data from the TP receiver.

3.2.4.3 Clock Recovery - 10 Mbps

The clock recovery process for 10 Mbps mode is identical to the 100 Mbps mode except, (1) the recovered clock frequency is 2.5 MHz nibble clock, (2) the PLL is switched from TX_CLK to the TP input when the squelch indicates valid data, (3) The PLL takes up to 12 transitions (bit times) to lock onto the preamble, so some of the preamble data symbols are lost, but the clock recovery block recovers enough preamble symbols to pass at least 6 nibbles of preamble to the receive controller interface as shown in Figure 3-15.

3.2.4.4 Data Recovery - 10 Mbps

The data recovery process for 10 Mbps mode is identical to the 100 Mbps mode. As mentioned in the Manchester Decoder section, the data recovery process inherently performs decoding of Manchester encoded data from the TP inputs.

3.2.5 Scrambler

3.2.5.1 100 Mbps

100Base-TX requires scrambling to reduce the radiated emissions on the twisted pair. SiS900 scrambler takes the encoded data from the 4B5B encoder scrambles it per the IEEE 802.3TP-PMD specifications, and sends it to the TP transmitter.

3.2.5.2 10 Mbps

A scrambler is not used in 10 Mbps mode.

3.2.6 Descrambler

3.2.6.1 100 Mbps

SiS900 descrambler takes the scrambled data from the data recovery block, descrambles it per the IEEE 802.3 TP-PMD specifications, aligns the data on the correct 5B word boundaries, and sends it to the 4B5B decoder.

The algorithm for synchronization of the descrambler is the same as the algorithm outlined in the IEEE 802.3 TP-PMD specification. Once the descrambler is synchronized, it will maintain synchronization as long as enough descrambled idle pattern 1's are detected within a given interval. To stay in synchronization, the descrambler needs to detect at least 25 consecutive descrambled idle pattern 1's in a 1 ms interval. If 25 consecutive descrambled idle pattern 1's are not detected within the 1 ms interval, the descrambler goes out of synchronization and restarts the synchronization process.

If the descrambler is in the unsynchronized state, the descrambler loss of synchronization detect bit is set in the MI Status Output register to indicate this condition. Once this bit is set, it will stay set until the descrambler achieves synchronization.

The output of the descrambler is also aligned according to the 4B/5B code groups. This alignment procedure is done by looking for the /J/K/ symbols at the beginning of the packet and then aligning all subsequent 4B/5B words relative tot he beginning of the /J/K/ symbols.

3.2.6.2 10 Mbps

A descrambler is not used in 10 Mbps mode.

3.2.7 Twister Pair Transmitter

3.2.7.1 Transmitter - 100 Mbps

The transmitter consists of an MLT-3 encoder, waveform generator and line driver.

The MLT-3 encoder converts the NRZ data from the scrambler into a three level MLT-3 code. MLT-3 coding uses three levels and converts 1's to transitions between the three levels, and converts 0's to no transitions or changes in level.

The purpose of the waveform generator is to shape the transmitter output pulse. The waveform generator takes the MLT-3 three level encoded waveform and uses an array of switched current sources to control the rise/fall time and level of the signal at the output. The output of the switched current sources then goes through a lowpass filter in order to "smooth" the current output and remove any high frequency components. In this way, the waveform generator preshapes the output waveform transmitted onto the twisted pair cable to meet the pulse template requirements outlined in IEEE 802.3. The waveform generator eliminates the need for any external filters on the TP transmit output.

The line driver converts the shaped and smoothed waveform to a current output that can drive 100 meters of category 5 unshielded twisted pair cable or 150 ohm shielded twisted pair cable.

3.2.7.2 Transmitter - 10 Mbps

The transmitter operation in 10 Mbps mode is much different than the 100 Mbps transmitter. Even so, the transmitter still consists of a waveform generator and line driver.

The purpose of the waveform generator is to shape the output transmit pulse. The waveform generator consists of a ROM, DAC, clock generator, and filter. The DAC generates a stair-stepped representation

of the desired output waveform. The stair stepped DAC output then goes through a low pass filter in order to "smooth" the DAC output and remove any high frequency components. The DAC values are determined from the ROM outputs; the ROM contents are chosen to shape the pulse to the desired template and are clocked into the DAC at high speed by the clock generator. In this way, the waveform generator preshapes the output waveform to be transmitted onto the twisted pair cable to meet the pulse template requirements outlined in IEEE 802.3 Clause 14 and also shown in Figure 3-17. The waveshaper replaces and eliminates external filters on the TP transmit output.

The line driver converts the shaped and smoothed waveform, to a current output that can drive 100 meters of category 3/4/5 100 Ohm unshielded twisted pair cable or 150 Ohm shielded twisted pair cable tied directly to the TP output pins without any external filters. During the idle period, no output signal is transmitted on the TP outputs (except link pulse).

SiS900 has special circuitry to reduce common mode noise on the twisted pair output. Common mode chokes may not be needed to meet emissions requirements in most 10 Mbps applications.

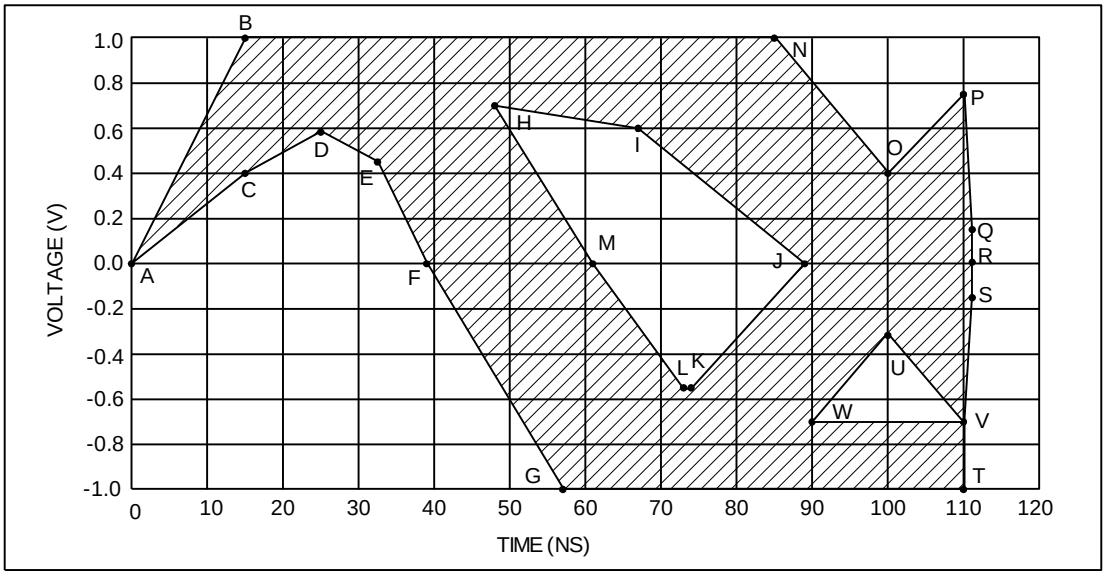


Figure 3-17 TP Output Voltage Template-10 Mbps

Table 3-6 Voltage Template Values for Figure 3-17

REFERENCE	TIME (NS) INTERNAL MAU	VOLTAGE(V)
A	0	0
B	15	1.0
C	15	0.4
D	25	0.55
E	32	0.45
F	39	0
G	57	-1.0
H	48	0.7

I	67	0.6
J	89	0
K	74	-0.55
L	73	-0.55
M	61	0
N	85	1.0
O	100	0.4
P	110	0.75
Q	111	0.15
R	111	0
S	111	-0.15
T	110	-1.0
U	100	-0.3
V	110	-0.7
W	90	-0.7

3.2.7.3 Transmit Level Adjust

The transmit output current level is derived from an internal reference voltage and the external resistor on REXT pin. The transmit level can be adjusted with either (1) the external resistor on the REXT pin, or (2) the four transmit level adjust bits in the MI Configuration 1 register as shown in Table 3-7. The adjustment range is approximately -14% to +16% in 2% steps.

Table 3-7 Transmit Level Adjust

TLVL[3::0]	GAIN
0000	1.16
0001	1.14
0010	1.12
0011	1.10
0100	1.08
0101	1.06
0110	1.04
0111	1.02
1000	1.00
1001	0.98
1010	0.96
1011	0.94
1100	0.92
1101	0.90
1110	0.88
1111	0.86

3.2.7.4 Transmit Rise And Fall Time Adjust

The transmit output rise and fall time can be adjusted with the two transmit rise/fall time adjust bits in the MI Configuration 1 register. The adjustment range is –0.25 ns to +0.50 ns in 0.25 ns steps (0 ns is the default).

3.2.7.5 STP (150 Ohm) Cable Mode

The transmitter can be configured to drive 150 ohm shielded twisted pair cable. The STP mode can be selected by appropriately setting the cable type select bit in the MI Configuration 1 register. When STP mode is enabled, the output current is automatically adjusted to comply with IEEE 802.3 levels.

3.2.7.6 Transmit Activity Indication

Transmit activity can be programmed to appear on some of the PLED[3::0]# pins by appropriately setting the programmable LED output select bits in the MI Configuration 2 register as describe in Table 3-11. When one or more of the PLED[3::0]# pins is programmed to be an activity or transmit activity detect output, that pin is asserted low for 100 ms every time a transmit packet occurs. The PLED[3::0]# output is open drain with resistor pull-up and can drive an LED from VCC or can drive another digital input.

3.2.7.7 Transmit Disable

The TP transmitter can be disabled by setting the transmit disable bit in the MI Configuration 1 register. When the transmit disable bit is set, the TP transmitter is forced into the idle state, no data is transmitted, no link pulses are transmitted, and internal loopback is disabled.

3.2.7.8 Transmit Power Down

The TP transmitter can be powered down by setting the transmit power down bit in the MI Configuration 1 register. When the transmit power down bit is set, the TP transmitter is powered down, the TP transmit outputs are high impedance, and the rest of SiS900 operates normally.

3.2.8 Twisted Pair Receiver

3.2.8.1 Receiver - 100 Mbps

The TP receiver detects input signals from the twisted pair input and convert it to a digital data bit stream ready for clock and data recovery. The receiver can reliably detect data from a 100Base-TX compliant transmitter that has been passed through 0-100 meters of 100 Ohm category 5 UTP or 150 Ohm STP.

The 100 Mbps receiver consists of a level shifter, low pass filter, adaptive equalizer, peak detector, comparator, baseline wander correction circuit, and MLT-3 decoder. A block diagram of the receiver is shown in Figure 3-21.

The TP receiver inputs are assumed to be transformer coupled and terminated by external resistors. The TP inputs are then level shifted and pass through a 2^{nd} order low pass filter designed to eliminate any high frequency noise on the input.

The signal then goes to an adaptive equalizer. The adaptive equalizer consists of a programmable bandpass filter and peak detector. The adaptive equalizer uses the bandpass filter characteristic to compensate for the low pass characteristics of the cable, and it uses the peak detector to capture the peak value of the input waveform and use it as a measure of cable length to adjust the pole and zero placement of the bandpass filter. The bandpass filter is digitally programmable and has a 5 bit digital input, called the equalizer setting, that adjusts the frequency response to one of 32 settings. The peak detector captures the peak voltage of the TP inputs, qualifies the input, and digitizes the qualified value to a 5 bit digital result. This digital result, called the equalizer setting, is used to adjust the

programmable bandpass filter characteristic. The peak detector qualifies the incoming data stream by only allowing single and double baud wide pulses to update the equalizer setting. If the digitized peak value of any single or double baud wide pulse deviates from the current equalizer setting in the same direction for more than 16 consecutive pulses, the equalizer setting is incremented by one digital step only. Independent of how much the new setting and current setting differ. The equalizer updating is only enabled when the receiver is in the unsquelch state (valid data detected by the TP squelch circuit).

The baseline wander correction circuit restores the DC component of the input waveform that was removed by external transformers by subtracting the filtered output of the data comparator from the filtered output of the equalizer and adding this difference back into the input of SiS900, as shown in Figure 3-21. The baseline wander correction circuit is only enabled when the descrambler is in the synchronized state.

The comparators are used to qualify and slice the data. There are two types of receive comparator, squelch and data. The squelch comparator compares the signal and the output of the LPF before the equalizer against a fixed threshold. The output of the squelch comparator is used for by the squelch circuit and link integrity blocks to qualify the data. The data comparators compare the signal at the output of the equalizer against fixed positive and negative thresholds.

The MLT-3 decoder takes the three level MLT-3 encoded output data from the comparators and converts it to normal NRZ data to be used for clock and data recovery.

3.2.8.2 Receiver - 10 Mbps

The 10 Mbps receiver is able to detect input signals from the twisted pair cable that are within the template shown in Figure 3-18. The inputs are biased by internal resistors. The TP inputs pass through a low pass filter designed to eliminate any high frequency noise on the input. The output of the receive filter goes to two different types of comparators, squelch and zero crossing. The squelch comparator determines whether the signal is valid, and the zero crossing comparator is used to sense the actual data transitions once the signal is determined to be valid. The output of the squelch comparator goes to the squelch circuit and is also used for link pulse detection, SOI detection, and reverse polarity detection; the output of the zero crossing comparator is used for clock and data recovery in the Manchester decoder.

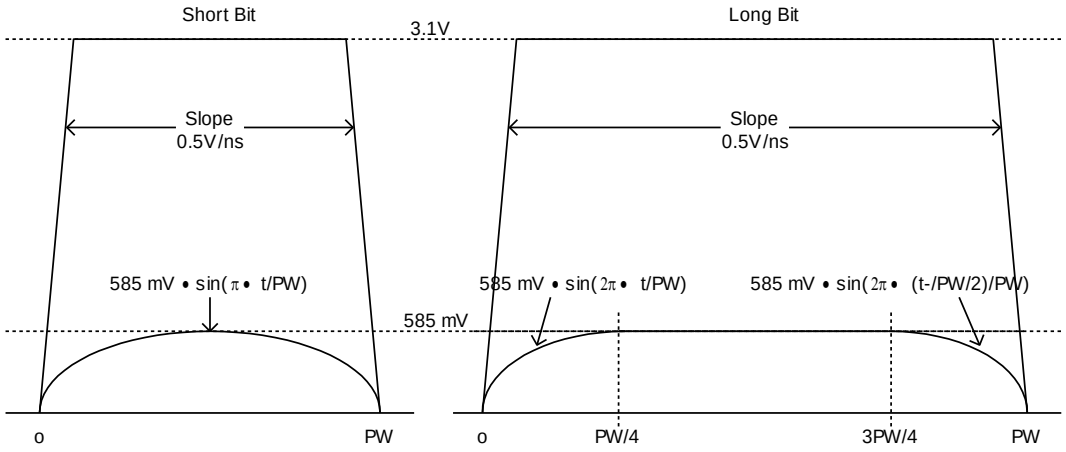


Figure 3-18 TP Input Voltage Template-10 Mbps

3.2.8.3 TP Squelch - 100 Mbps

The squelch block determines if the TP input contains valid data. The 100 Mbps TP squelch is one of the criteria used to determine link integrity. The squelch comparator compare the TP inputs against

fixed positive and negative thresholds, called squelch levels. The output from the squelch comparator goes to a digital squelch circuit which determines if the receive input data on that channel is valid. If the data is invalid, the receiver is in the squelched state. If the input voltage exceeds the squelch levels at least 4 times with alternating polarity within a 10 μs interval, the data is considered to be valid by the squelch circuit and the receiver now enters into the unsquelch state. In the unsquelch state, the receive threshold level is reduced by approximately 30% for noise immunity reasons and is called the unsquelch level. When the receiver is in the unsquelch state, then the input signal is deemed to be valid. The device stays in the unsquelch state until loss of data is detected. Loss of data is detected if no alternating polarity unsquelch transitions are detected during any 10 μs interval. When the loss of data is detected, the receive squelch is turned on again.

3.2.8.4 TP Squelch - 10 Mbps

The TP squelch algorithm for 10 Mbps mode is identical to the 100 Mbps mode except, (1) the 10 Mbps TP squelch algorithm is not used for link integrity but to sense the beginning of a packet, (2) the receiver goes into the unsquelch state if the input voltage exceeds the squelch levels for three bit times with alternating polarity with in a 50-250 ns interval, (3) the receiver goes into the squelch state when idle is detected, (4) unsquelch detection has no affect on link integrity, link pulses are used for that in 10 Mbps mode, (5) start of packet is determined when the receiver goes into the unsquelch state and CRS is asserted, and (6) the receiver meets the squelch requirements defined in IEEE 802.3 Clause 14.

3.2.8.5 Equalizer Disable

Setting the equalizer disable bit in the MI Configuration 1 register can disable the adaptive equalizer. When disabled, the equalizer is forced into the response it would normally have if zero cable length were detected.

3.2.8.6 Receive Level Adjust

The receiver squelch and unsquelch levels can be lowered by 4.5 dB by setting the receive level adjust bit in the MI Configuration 1 register. By setting the bit, the device may be able to support longer cable lengths.

3.2.8.7 Receive Activity Indication

Receive activity can be programmed to appear on some of the PLED[3::0]# pins by appropriately setting the programmable LED output select bits in the MI Configuration 2 register as shown in Table 3.2-7. When one or more of the PLED[3::0]# pins is programmed to be an receive activity or activity detect output, that pin is asserted low for 100 ms every time a receive packet occurs. The PLED[3::0]# outputs are open drain with resistor pull-up and can drive an LED from VCC or can drive another digital input.

3.2.9 Collision

3.2.9.1 100 Mbps

Collision occurs whenever transmit and receive occur simultaneously while the device is in Half Duplex.

Collision is sensed whenever there is simultaneous transmission (packet transmission on TPO±) and reception (non idle symbols detected on TP input). When collision is detected, the COL output is asserted, TP data continues to be transmitted on twisted pair outputs, TP data continues to be received on twisted pair inputs, and internal CRS loopback is disabled. Once collision starts, CRS is asserted and stays asserted until the receive and transmit packets that caused the collision are terminated.

The collision function is disabled if the device is in the Full Duplex mode, is in the Link Fail state, or if

the device is in the diagnostic loopback mode.

3.2.9.2 10 Mbps

Collision in 10 Mbps mode is identical to the 100 Mbps mode except, (1) reception is determined by the 10 Mbps squelch criteria, (2) the clock recovery PLL is switched from the RX data back tot he TX clock as soon as collision is sensed, (3) RXD[3::0] outputs are forced to all 0's, (4) collision is asserted when the jabber condition has been detected.

3.2.9.3 Collision Test

Setting the collision test register bit in the MI Control register can test the controller interface collision signal, COL. When this bit is set, TX_EN is looped back onto COL and the TP outputs are disabled.

3.2.9.4 Collision Indication

Collision can be programmed to appear on the PLED2# pin by appropriately setting the programmable LED output select bits in the MI Configuration 2 register, as shown in Table 3-11. When the PLED2# pin is programmed to be a collision detect output, this pin is asserted low for 100 ms every time a collision occurs. The PLED2# output is open drain with resistor pull-up and can drive an LED from VCC or can drive another digital input.

3.2.10 Start Of Packet

3.2.10.1 100 Mbps

Start of packet for 100 Mbps mode is indicated by a unique Start of Stream Delimiter (referred to as SSD). The SSD pattern consists of the two /J/K/ 5B symbols inserted at the beginning of the packet in place of the first two preamble symbols, as defined in IEEE 802.3 Clause 24 and shown in Figure 3-16.

The transmit SSD is generated by the 4B5B encoder and the /J/K/ symbols are inserted by the 4B4B encoder at the beginning of the transmit data packet in place of the first two 5B symbols of the preamble, as shown in Figure 3-16.

The receive pattern is detected by the 4B5B decoder by examining groups of 10 consecutive code bits (two 5B words) from the descrambler. Between packets, the receiver will be detecting the idle pattern, which is 5B /I/ symbols. While in the idle state, CRS and RX_DV are deasserted.

If the receiver is in the idle state and 10 consecutive code bits from the receiver consist of the /J/K/symbols, the start of packet is detected, data reception is begun, CRS and RX_DV are asserted, and /5/5/symbols are substituted in place of the /J/K/symbols.

If the receiver is in the idle state and 10 consecutive code bits from the receiver consist of a pattern that is neither /I/I/ nor /J/K/symbols but contains at least 2 non contiguous 0's, then activity is detected but the start of packet is considered to be faulty and a False Carrier Indication (also referred to as bad SSD) is signaled to the controller interface. When False Carrier is detected, then CRS is asserted, RX_DV remains deasserted RXD[3::0]=1110 while RX_ER is asserted, and the bad SSD bit is set in the MI Status Output register. Once a False Carrier Event is detected, the idle pattern (two /I/I/ symbols) must be detected before any new SSD's can be sensed.

If the receiver is in the idle state and 10 consecutive code bits from the receiver consist of a pattern that is neither /I/I/ nor /J/K/symbols but does not contain at least 3 non contiguous 0's, the data is ignored and the receiver stays in the idle state.

3.2.10.2 10 Mbps

Since the idle period in 10 Mbps mode is defined to be the period when no data is present on the TP

inputs, then the start of packet for 10 Mbps mode is detected when valid data is detected by the TP squelch circuit. When start of packet is detected, CRS is asserted as described in the Controller Interface section. Refer to the TP squelch section for 10 Mbps mode for the algorithm for valid data detection,

3.2.11 End Of Packet

3.2.11.1 100 Mbps

End of packet for 100 Mbps mode is indicated by a End of Stream Delimiter (referred to as ESD). The ESD pattern consists of the two /T/R/ 4B5B symbols inserted after the end of the packet, as defined in IEEE 802.3 Clause 24 and shown in Figure 3-16.

The transmit ESD is generated by the 4B5B encoder and the /T/R/ symbols are inserted by the 4B5B encoder after the end of the transmit data packet, as shown in Figure 3-16.

The receive ESD pattern is detected by the 4B5B decoder by examining groups of 10 consecutive code bits (two 58 words) from the descrambler during valid packet reception to determine if there is an ESD.

If the 10 consecutive code bits from the receiver during valid packet reception consist of the /T/R/ symbols, the end of packet is detected, data reception is terminated, CRS and RX_DV are asserted, and /I/I/ symbols are substituted in place of the /T/R/ symbols.

If the 10 consecutive code bits from the receiver during valid packet reception do not consist of /T/R/ symbols but consist of /I/I/ symbols instead, then the packet is considered to have been terminated prematurely and abnormally. When this premature end of packet condition is detected, RX_ER is asserted for the nibble associated with the first /I/ symbol detected and then CRS and RX_DV are deasserted. Premature end of packet condition is also indicated by setting the bad ESD bit in the MI Status Output register.

3.2.11.2 10 Mbps

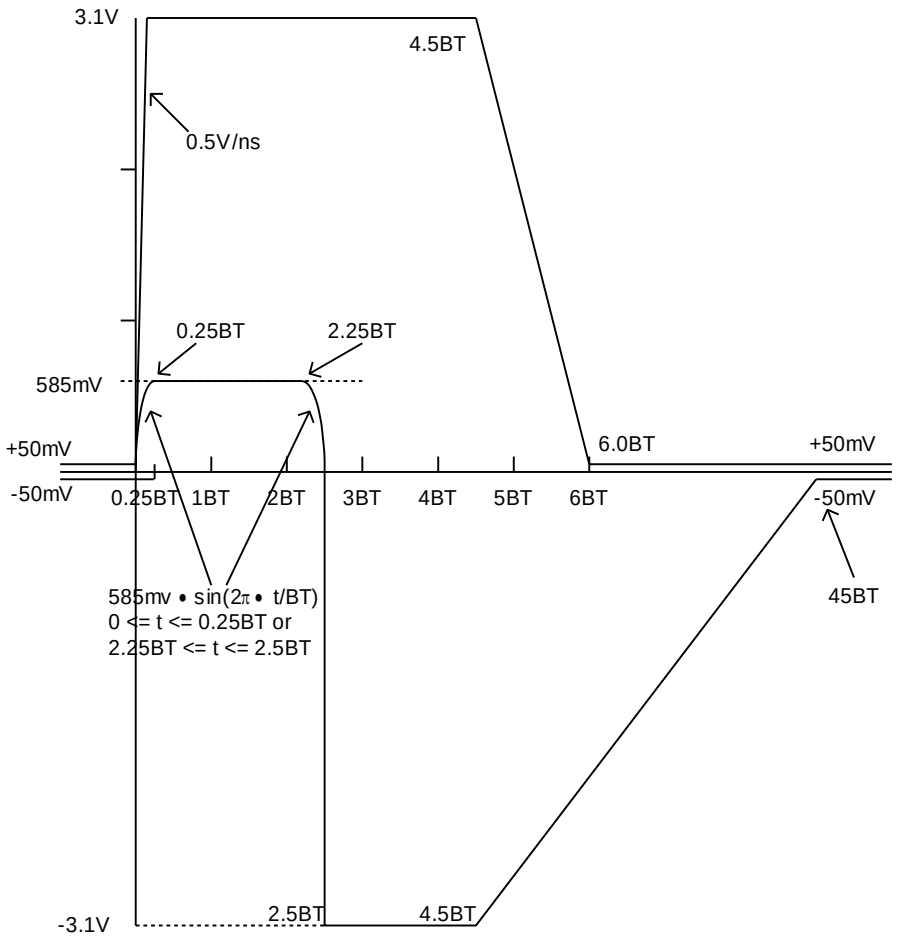


Figure 3-19 SOI Output Voltage Template - 10 Mbps

The end of packet for 10 Mbps mode is indicated with the SOI (Start of Idle) pulse. The SOI pulse is a positive pulse containing a Manchester code violation inserted at the end of every packet.

The transmit SOI pulse is generated by the TP transmitter and inserted at the end of the data packet after TX_EN is deasserted. The transmitted SOI output pulse at the TP output is shaped by the transmit waveshaper to meet the pulse template requirements specified in 1EEE 802.3 Clause 14 and shown in Figure 3-19.

The receive SOI pulse is detected by the TP receiver by sensing missing data transitions. Once the SOI pulse is detected, data reception is ended and CRS and RX_DV are deasserted.

3.2.12 Link Integrity & Auto-Negotiation

3.2.12.1 General

Link pulses are a means used by the twisted pair interface to indicate that the twisted pair link is intact. SiS900 can be configured to implement either the standard link integrity algorithms or the Auto-Negotiation algorithm.

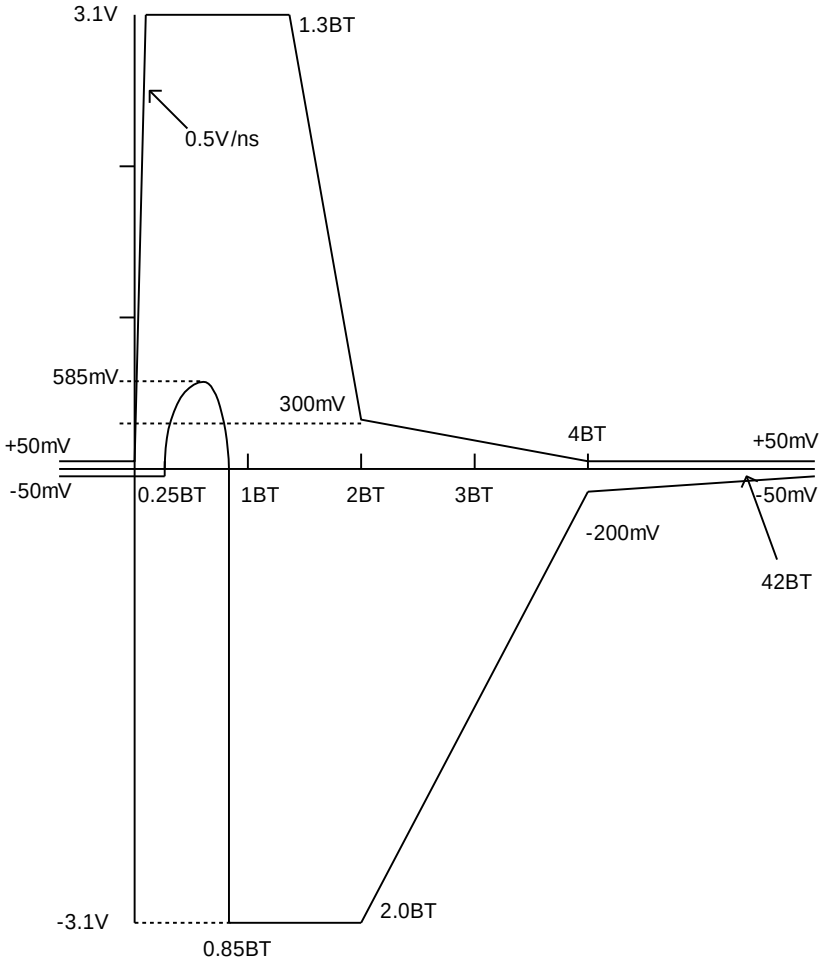


Figure 3-20 Link Pulse Output Voltage Template - NLP, FLP

The standard link integrity algorithm is used to indicate and establish an active link to and from a remote device. For 100 Mbps mode, the standard link integrity algorithm is outlined in various sections of the IEEE 802.3 specification with additional steps added as described in the receive TX LNK Link Integrity section. For 10 Mbps mode, the standard link integrity algorithm is the same as the 10Base-T link integrity algorithm as specified in IEEE 802.3 Clause 14.

The Auto-Negotiation algorithm is used to indicate and establish an active link to and from a remote device as well as automatically configure the device for either 100Base-TX Full or 100Base-TX Half duplex operation, or 10Base-TX Half duplex operation, or 10Base-T Full or 10Base-T Half Duplex operation. The Auto-Negotiation algorithm is the same as the Auto-Negotiation Signaling algorithm as specified in IEEE802.3 Clause 28.

SiS900 has three different transmitted link signals and four receive link integrity algorithms. Two of the transmitted link signals, NLP's and FLP's, are actually link pulses transmitted during the idle period as shown in Figure 3.2-8. The third transmitted link signal, TXLNK, is not a link pulse but the

transmission of symbols indicating idle that can be sensed and used to establish link integrity. The four receive link integrity algorithms are 10Base-T, NLP, 100Base-TX, and Auto-Negotiation. Each one of these is described in the following sections. The 10Base-T receive link integrity algorithm is used for link integrity only, while the Auto-Negotiation, NLP, and 100Base-TX algorithm are used for link integrity along with automatic configuration for 100/10 Mbps and Full/Half Duplex operation.

3.2.12.2 Transmit NLP

The transmit NLP (normal link pulse) is a single positive pulse spaced every 16+/- ms apart and is preshaped by the transmit waveform generator to meet the pulse template specified in IEEE 802.3 Clause 14 and shown in Figure 3-20. Refer to Figure 3-21 for difference between NLP and FLP.

3.2.12.3 Transmit FLP

The Transmit FLP (fast link pulse) is link pulse bursts spaced every 16+/-8 ms apart. The basic FLP transmitted link pulse is a single positive pulse that meets the same voltage template requirements specified for NLP's. The FLP burst consists of 17-33 link pulses spaced 62.5 us apart. Refer to Figure 3.2-8. The entire FLP burst is completed in 2 ms. 17 of the FLP's are clock FLP's and are always present. Another 0-16 of the FLP's are data FLP's that convey 16 data bits of the information. The data FLP's are spaced between the clock FLP's. Presence of a data FLP after a clock FLP is defined as a data bit value of 1; absence of a data FLP after a clock FLP is defined as a data bit value of 0. In this way, up to 16 bits of data can be signaled between two devices outside the normal packet structure.

3.2.12.4 Transmit TXLINK

The 100Base-TX does not have a transmit link integrity signal because data is always transmitted, even during the idle time between packets. As such, the receiver will use a complex data algorithm to establish link integrity, as described in the receive 100Base-TX Link Integrity section.

3.2.12.5 Receive 10Base-T Link Integrity Algorithm

The receive 10Base-T link pulse algorithm is the same as the one defined in IEEE 802.3 Clause 14. The 10Base-T algorithm detects transmitted NLP's. When the device powers up or resets, it is in the Link Fail State. In the Link Fail State, the transmit and receive data paths are disabled, CRS is disabled, and link pulses continue to be transmitted. For the device to exit the Link Fail State, 3 consecutive link pulses or one valid data packet needs to be detected by the receiver. While in the Link Pass State, if neither data nor link pulses are detected by the receiver for a period of 50-150 ms, the device enters the Link Fail State. Link pulses spaced less that 3-5 ms apart reset the link pulse counters in Link Fail State and are ignored as noise in Link Pass State.

3.2.12.6 Receive NLP Link Integrity Algorithm

The receive NLP link integrity algorithm is the same as the receive 10Base-T link integrity algorithm but with two modifications: (1) a halt state has been added that freezes the 10Base-T link pulse state machine when a halt command is issued and forces the device into the Link Fail State when the halt command is deasserted, and (2) only link pulses and not data can cause the device to exit from the Link Fail State.

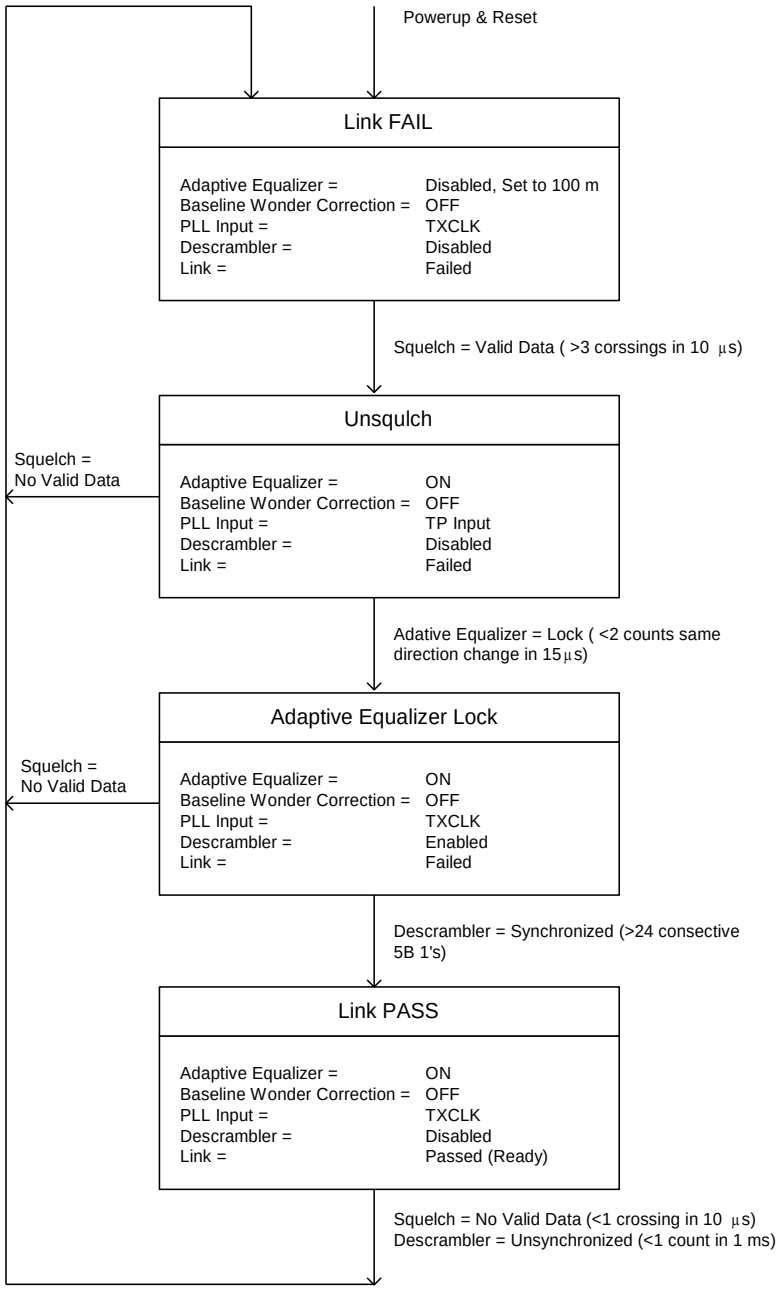


Figure 3-21 Receive 100Base-TX Link Integrity Algorithm

3.2.12.7 Receive 100Base-TX Link integrity Algorithm

The receive 100Base-TX link integrity algorithm uses the data quality indicators to determine link integrity. The exact link integrity algorithm for 100Base-TX is shown in the state machine in Figure 3-21.

3.2.12.8 Auto-Negotiation Data Field

Auto-Negotiation uses FLP bursts to combine link pulses with a 16 bit data word. The definition of the 16 bits transmit/receive FLP data word is shown in Table 3-8. The Transmitted data word (exclusive of bit D14) is determined from the contents of MI Register 4, the Auto-Negotiation Advertisement Register, as described in Section 4.4.5, and it is user programmable. The transmitted bit D14 is the acknowledge bit and is used for handshaking, and is internally set and cleared according to the Auto-Negotiation algorithm. The received Auto-Negotiation data word from the remote end is stored in MI Register 5, the Auto-Negotiation Remote Capability Register, as shown in Section 4.4.6, and it can be read out by the user. The Auto-Negotiation algorithm uses the advertised capability and remote capability data words to decide if the device should be placed in 10/100 Mbps and Full/Half Duplex modes. After the decision is made, the device is updated to the appropriate modes, the 10/100 Mbps and Full/Half Duplex mode decision are available as speed and duplex status bits in the MI Status Output register, and any PLED[3::0]# pins programmed to indicate 100/10 Mbps and Full/Half Duplex modes are asserted.

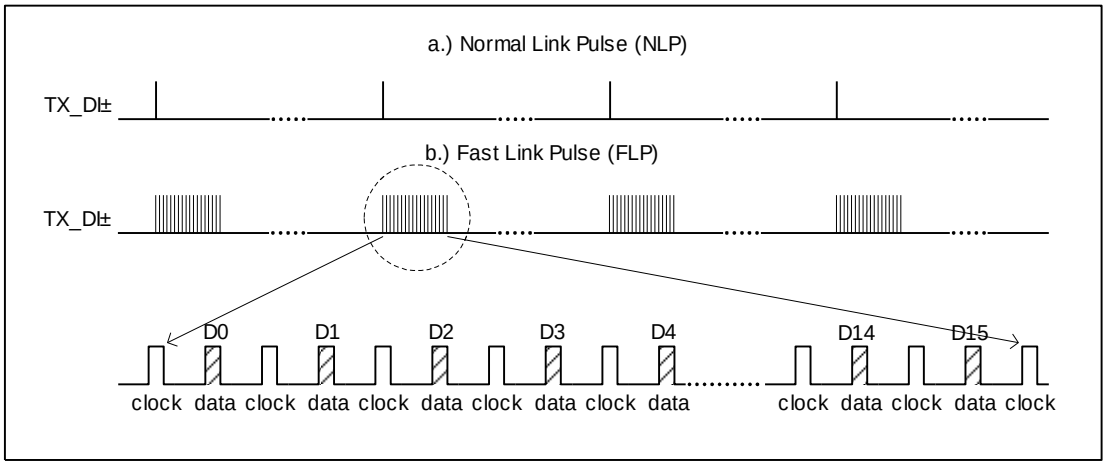


Figure 3-22 NLP vs. FLP Link Pulse

3.2.12.9 Receive Auto-Negotiation Algorithm

The receive Auto-Negotiation algorithm advertises the local capabilities to the remote end, looks to see what capabilities the remote end has broadcasted back, and then configures the device according to the decision algorithm in Table 3-19. The decision algorithm in Table 3-19 always chooses the mode that offers the highest performance that both the device and remote end device both support, called the highest common denominator mode, as specified in IEEE 802.3 Clause 28. The order of priority for the highest common denominator mode is as follows: (1) 100Base-TX Full Duplex, (2) 100Base-T4 Half Duplex, (3) 100Base-TX Half Duplex, (4) 10Base-T Full Duplex, (5) 10Base-T Half Duplex, and (6) None (disable transmit and receive data paths and renegotiate). In this way, the Auto-Negotiation algorithm combines receive NLP and 100Base-TX link algorithms along with data signaling capabilities.

When the device power up or is reset, or when Auto-Negotiation is reset or enabled, all transmission is halted including link pulses for 1200-1500 ms, the device is restarted in the Link Fail state, and Auto-Negotiation status bits are set for Auto-Negotiation started in the MI Status Output register. In the Link Fail State, the transmit and receive data paths are disabled, CRS is disable.

The device now advertises its capabilities to the far end. To do this, the transmitter sends out FLP bursts using the data word stored in the Auto-Negotiation Advertisement Register but with the acknowledgement bit D14 cleared.

Table 3-8 Auto-Negotiation Data Field Definition

BIT	SYMBOL	NAME	DEFINITION
D0	CSMA	CSMA 802.3 Capable	1 Capable of 802.3 Operation 0 Not Capable
D4 – D1			Reserved, Should Be 0's
D5	10HD	10Base-T Half Duplex Capable	1 Capable of 10Base-T Half Duplex 0 Not Capable
D6	10FD	10Base-T Full Duplex Capable	1 Capable of 10Base-T Full Duplex 0 Not Capable
D7	TXHD	100Base-TX Half Duplex Capable	1 Capable of 100Base-TX Half Duplex 0 Not Capable
D8	TXFD	100Base-TX Full Duplex Capable	1 Capable of 100Base-TX Full Duplex 0 Not Capable
D9	T4HD	100BaseT4 Half Duplex Capable	1 Capable of 100BaseT4 Half Duplex 0 Not Capable
D10	PAUSE	802.3x Pause Operation Capable	1 Capable of 802.3x Pause Operation 0 Not Capable
D12 –D11			RESERVED, Should Be 0's
D13	RF	Remote Fault Enable	1 Auto-Negotiation Remote Fault Detected 0 Normal
14	ACK	Acknowledge	1 Received Auto-Negotiation Word Recognized 0 Not Recognized
15	NP	Next Page Enable	1 Next Page Exists 0 No Next Page

Next, the receiver listens to the received link pulses from the remote end to determine if the remote terminal is sending NLP's, TX data, or FLP's. To do this, the NLP, TXLINK, and Auto-Negotiation algorithms are all activated, and the 10Base-T algorithm is halted.

If the receiver detects a NLP Link Pass only, then the device determines that the remote terminal is 10Base-T capable only, switches to the receive NLP link integrity algorithm, configures itself for 10 Mbps operation, and configures itself for Half Duplex.

If the receiver detects a TX Link Pass only, then the device determines that the remote terminal is 100Base-TX capable only, switches to the receive TXLINK link integrity algorithm, configures itself for 100 Mbps operation, and configures itself for Half Duplex operation.

If the receiver detects 3 consecutive and consistent valid FLP bursts ignoring the acknowledge bit D14, then the device determines that the remote terminal is Auto-Negotiation capable, sets the Auto-Negotiation status bit for Auto-Negotiation detect in the MI Status Output register, and starts the Auto-Negotiation acknowledgement process. A valid FLP burst is defined as one with at least 17 detectable clock pulses with each burst occurring in a 50-150 ms interval. Consistent FLP bursts are those with identical data words ignoring the acknowledge bit D14.

The acknowledgement process begins with the transmitter sending out the same FLP bursts but with the acknowledge bit, D14, set high.

Table 3-9 Auto-Negotiation Speed and Duplex Decision Algorithm

Xmt Advertised Capability	Rcv Remote Capability	Decision			
D[8,7,6,5,]	D[8,7,6,5]	TX	10BT	FDX	HDX
1xxx	1xxx	√		√	
01xx	x1xx	√			√
x1xx	01xx	√			√
001x	xx1x		√	√	
xx1x	001x		√	√	
0001	xxx1		√		√
xxx1	0001		√		√
Any Other Combination		Disable XMT & RCV Data Paths, Renegotiate			

If the receiver detects the same 3 consecutive and consistent FLP bursts again with the receive acknowledge bit D14 set, then the device transmits an additional 8 FLP bursts to the remote end and activates and switches over to either the NLP or TXLINK link integrity algorithm, depending on what speed is selected. The device now has 750-1000 ms to exit the Link Fail State. If the Link Fail state is not exited in 750-1000ms, the entire process is restarted. If the device does exit the Link Fail State in less than 750-1000 ms, the acknowledgement process is completed. The acknowledgement process completion causes the device to update itself to 100/10 Mbps and Full/half Duplex modes depending on the received values of D8, D7, D6, D5, and Table 3-9: (1) update the duplex bit in the MI Status Output register, (2) update the 100/10 speed detect bit in the MI Status Output register, (3) update the Auto-Negotiation acknowledgement bit in the MI Status register, (4) update the Auto-Negotiation status bits to indicate Auto-Negotiation done in the MI Status Output register, and (5) update the remote fault detect bit in the MI Status register.

If the receiver does not detect 3 consecutive and consistent FLP bursts with the acknowledge bit D14 set within 1200-1500 ms, the Auto-Negotiation Status bits are set to the Auto-Negotiation Stuck state in the MI Status Output register, but the device stays in the acknowledgement process state and continues to transmit FLP bursts with the acknowledgement bit D14 set and try to complete the acknowledgement process.

If the device enters the Link Fail State from the Link Pass state, the entire process is restarted. The Link Fail state is entered if data or NLP's are not received according to the NLP and TXLINK link integrity algorithms defined in IEEE 802.3 described in previous sections. When the Link Fail state is detected on the receiver, all transmissions are inhibited including link pulses for a period of 1200-1500 ms in order to cause the remote terminal to go into Link Fail and start re-negotiation.

If the device stops detecting FLP bursts in a 50-150 ms interval while in the Auto-Negotiation negotiation process is in progress, the device stays in the Link Fail state, all transmissions including link pulses are inhibited for a 1200-1500 ms interval, and the entire process is restarted.

3.2.12.10 Auto-Negotiation Outcome Indication

The outcome or result of the Auto-Negotiation process is stored in the speed detect and duplex detect bits in the MI Status Output register.

3.2.12.11 Auto-Negotiation Status

Reading the Auto-Negotiation status bits in both the MI Status and Status Output registers can monitor the status of the Auto-Negotiation process. The MI Status register contains a single Auto-Negotiation

acknowledgement bit that indicates when an Auto-Negotiation has been initiated and successfully completed. The MI Status Output register contains two Auto-Negotiation status bits which indicate one of four possible conditions as described in Table 3-10.

Table 3-10 Auto-Negotiation Status Bit Description

AUTO-NEGOTIATION STATUS BIT (18.5-18.4)	DEFINITION	DESCRIPTION
11	Auto-Negotiation Started	Auto-Negotiation sequence has been initiated but has not been completed.
10	Auto-Negotiation Stuck	Auto-Negotiation process has been ongoing for over 1200-1500 ms and has not yet completed.
01	Auto-Negotiation Done	Auto-Negotiation sequence has been initiated and successfully complete..
00	Auto-Negotiation Not Detected	Auto-Negotiation ability was not detected from the remote device.

3.2.12.12 Auto-Negotiation Enable

The Auto-Negotiation algorithm can be enabled (or restarted) by setting the Auto-Negotiation enable bit in the MI Control register. When the Auto-Negotiation algorithm is enabled, the device halts all transmissions including link pulses for 1200-1500 ms, enters the Link Fail State, and restarts the negotiation process. When the Auto-Negotiation algorithm is disabled, the selection of 100 Mbps or 10 Mbps modes is determined by the speed select bit in the MI Control register, and the selection of Half or Full Duplex is determined by the duplex select bit in the MI Control register.

3.2.12.13 Auto-Negotiation Reset

The Auto-Negotiation algorithm can be initiated at any time by setting the Auto-Negotiation reset bit in the MI Control register. When the Auto-Negotiation reset bit is set, the device halts all transmissions including link pulses for 1200-1500 ms, enters the Link Fail State, and restarts the negotiation process. The Auto-Negotiation reset bit clears itself automatically once the reset is completed.

3.2.12.14 Link Indication

Receive link pulse detect activity is indicated in three different ways: (1) the link status bit in the MI Status register, (2) the link fail detect bit in the MI Status Output register, and (3) PLED3# or PLED0# pins.

The link status bit in the MI Status register reflects the current link status. This bit is latched low when the link goes to the fail state and stays low until read out.

The link fail detect bit in the MI Status Output register also reflects the link status but it does not go to a logic “1” until the receive link has been continuously in the fail state for a specific interval of time, called the link fail timer interval. The link fail timer interval is programmable by appropriately setting the link fail timer select bits in the Mask register. The link fail detect bit latches itself every time it changes state and is updated after it is read out. The link fail detect bit can also be programmed to assert interrupt if its mask bit is cleared in the Mask register.

Link status can also be programmed to appear on the PLED3# or PLED0# pins by setting the programmable LED output select bits in the MI Configuration 2 register. When either the PLED3# or PLED0# pins are programmed to be a link pulse detect output, this pin is asserted low whenever the device is in the Link Pass State. The PLED3# output is open drain with resistor pull-up and can drive an LED from VCC; the PLED0# output has both pull-up and pull-down driver transistors plus a weak resistor pull-up, so it can drive an LED from either VCC or GND. Both PLED3# and PLED0# can also

drive another digital input. Refer to the LED Driver section for a description on how to program the PLED[3::0]# pins and their defaults.

3.2.12.15 Link Disable

Setting the link disable bit in the MI Configuration 1 register can disable the link integrity function. When the link integrity function is disabled, the device ignores the reception of link pulses, stays in the Link Pass state, configures itself for Half/Full Duplex based on the value of the duplex bit in the MI Control register, configures itself for 100/10 Mbps operation based on the value of the speed bit in the MI Control register, and continues to transmit NLP's or TX idle patterns, depending on whether the device is in 10 or 100 Mbps mode.

3.2.13 Jabber

3.2.13.1 100 Mbps

Jabber function is disabled in the 100 Mbps mode.

3.2.13.2 10 Mbps

Jabber condition occurs when the transmit packet exceeds a predetermined length. When jabber is detected, the TP transmit outputs are forced to the idle state, collision is asserted, and register bits in the MI Status and Status Output registers are set.

3.2.13.3 Jabber Disable

Setting the jabber disable bit in the MI Configuration 2 register can disable the jabber function.

3.2.14 Receive Polarity Correction

3.2.14.1 100 Mbps

No polarity detection or correction is needed in 100 Mbps mode.

3.2.14.2 10 Mbps

The polarity of the signal on the TP receive input is continuously monitored. If one SOI pulses indicate incorrect polarity on the TP receive input, the polarity is internally determined to be incorrect, and a reverse polarity bit is set in the MI Status Output register.

SiS900 will automatically correct for the reverse polarity condition provided that the auto-polarity feature is not disabled.

3.2.14.3 Auto-polarity Disable

Setting the auto-polarity disable bit in the MI Configuration 2 register can disable the auto-polarity feature.

3.2.15 Full Duplex Mode

3.2.15.1 100Mbps

Full Duplex mode allows transmission and reception to occur simultaneously. When Full Duplex mode is enabled, collision is disabled and internal TX_EN to CRS loopback is disabled.

The device can be either forced into Half or Full Duplex mode, or the device can detect either Half or Full Duplex capability from a remote device and automatically place itself in the correct mode.

The device can be forced into the Full or Half Duplex modes by setting the duplex bit in the MI Control register.

The device can automatically configure itself for Full or Half Duplex modes by using the Auto-Negotiation algorithm to advertise and detect Full and Half Duplex capabilities to and from a remote terminal. All of this is described in detail in the Link Integrity and Auto-Negotiation section.

3.2.15.2 10Mbps

Full Duplex in l0 Mbps mode is identical to the 100 Mbps mode.

3.2.15.3 Full Duplex Indication

Full Duplex detection can be monitored through the duplex bit in the MI Status output register, or it can be programmed to appear the PLED1# pin by appropriately setting the programmable LED output select bits in the MI Configuration 2 register as described in Table 3-11. When the PLED1# pin is programmed to be a Full Duplex detect output, this pin is asserted low when the device is configured for Full Duplex operation. The PLED1# output has both pull-up and pull-down driver transistors and a weak pull-up resistor, so it can drive an LED from either VCC or GND and can also drive a digital input.

3.2.16 100/10 Mbps Selection

3.2.16.1 General

The device can be forced into either the 100 or 10 Mbps mode, or the device also can detect 100 or 10 Mbps capability from a remote device and automatically place itself in the correct mode.

The device can be forced into either the 100 or 10 Mbps mode by setting the speed select bit in the MI Control register.

The device can automatically configure itself for 100 or 10 Mbps mode by using the Auto-Negotiation algorithm to advertise and detect 100 and 10 Mbps capabilities to and from a remote terminal. All of this is described in detail in the Link Integrity & Auto-Negotiation section.

3.2.16.2 10/100 Mbps Indication

The device speed (100/10 Mbps) can be determined through the speed bit in the MI Status Output register, or it can also be programmed to appear on the PLED0# pin by setting the programmable LED output select bits in the MI Configuration 2 register. When the PLED0# pin is programmed to be speed detect output, this pin is asserted low when the device is configured for 100 Mbps operation. The PLED0# output has both pull-up and pull-down driver transistors and a weak pull-up resistor, so it can drive an LED from either VCC or GND and can also drive a digital input.

3.2.17 PHY Loopback

3.2.17.1 Internal CRS Loopback

TX_EN is internally looped back onto CRS during every transmit packet. This internal CRS loopback is disabled during collision, in Full Duplex mode, in Link Fail State, when the transmit disable bit is set in the MI Configuration 1 register. In 10 Mbps mode, internal CRS loopback is also disabled when jabber is detected.

The internal CRS loopback can be disabled by setting the TX_EN to CRS loopback disable bit in the MI Configuration 1 register. When this bit is set, TX_EN is no longer looped back to CRS.

3.2.17.2 Diagnostic Loopback

A diagnostic loopback mode can also be selected by setting the loopback bit in the MI Control register. When diagnostic loopback is enabled, TXD[3::0] data is looped back onto RXD[3::0], TX_EN is looped back onto CRS, RX_DV operates normally, the TP receive and transmit paths are disabled, the transmit link pulses are halted, and the Half/Full Duplex modes do not change. Diagnostic loopback mode can not be enabled when the FBI interface is selected.

3.2.18 PHY Reset

SiS900 PHY is reset when either (1) VCC is applied to the device or (2) the reset bit is set in the MI Control register. When reset is initiated, an internal power-on reset pulse is generated which resets all internal PHY circuits, forces the MI Registers bits to their default values. After the power-on reset pulse has finished, the reset bit in the MI Control register is cleared and the device is ready for normal operation. The device is guaranteed to be ready for normal operation 500 ms after the reset was initiated.

3.2.19 Power Down

SiS900 can enter powered down mode by setting the power down bit in the MI Control register. In power down mode, the TP outputs are in high impedance state, all functions are disabled except the MI Registers, and the power consumption is reduced to a minimum. The device is guaranteed to be ready for normal operation 500 ms after power down is deasserted.

3.2.20 Oscillator

SiS900 requires a 25 Mhz reference frequency for internal signal generation. This 25 Mhz reference frequency is generated by either connecting an external/25 MHz crystal between OSCIN and GND or by applying an external 25Mhz clock to OSCIN.

3.2.21 LED Drivers

There are four LED outputs PLED[3::0]# provide by SiS900. The PLED[3::2]# outputs are open drain with a resistor pull-up and can drive LED's tied to VCC. PLED[1::0]# outputs have either pull-up or pull-down with a resistor, so PLED[1::0]# can drive LED's tied to either VCC or GND.

The PLED[3::0]# outputs can be programmed through the MI Configuration 2 register to do 4 different functions: (1) Normal Function (2) On, (3) Off, and (4) Blink.. When PLED[3::0]# are programmed for their Normal Functions, these outputs indicate specific events. There are four sets of specific events that these outputs can indicate, and they are described in Tables 3-11 and 3-12. The selection of which set of events that these outputs indicate is determined by appropriately setting the LED Normal Function select bits in the MI Configuration 2 register. The default Normal Functions for PLED[3::0]# are Link 100, Activity, Full Duplex, and Link 10, respectively.

When PLED[3::0]# is programmed to be off, the LED output driver go low, thus timing on the LED under user control. When PLED[3::0]# is programmed to be On, the LED output driver will turn off, thus turning off the LED under user control. When PLED[3::0]# is programmed to Blink, the LED output driver will continuously blink at a rate of 100 ms on, 100 ms off.

Table 3-11 LED Normal Function Definition

BITS 17.7-6	PLED3#	PLED2#	PLED1#	PLED0#
11	LINK	COL	FDX	10/100
10	LINK	ACT	FDX	10/100
01	LINK + ACT	COL	FDX	10/100
00 (Default)	LINK 100	ACT	FDX	LINK 10

Device powers up with default set to 00.

Table 3-12 LED Event Definition

SYMBOL	DEFINITION
ACT	Activity Occurred, Stretch Pulse to 100 ms
COL	Collision Occurred Stretch Pulse to 100 ms
LINK 100	100 Mb Link Detected
LINK 10	10 Mb Link Detected
LINK	100 or 10 Mb Link Detected
LINK + ACT	100 or 10 Mb Link Detected or Activity Occurred, Stretch Pulse To 100 mS (Link Detect Causes LED to be On, Activity Causes LED to Blink)
FDX	Full Duplex Mode Enabled
10/100	10 Mb Mode Enabled (High), or 100 Mb Mode Enabled (Low)

4. REGISTERS DESCRIPTION

4.1 Register Overview

SiS900 is configured and controlled through registers. There are three categories of control/status registers implemented inside SiS900, which includes PCI Configuration Registers, MAC Operational Registers and MII PHY Registers. The PCI Configuration registers are mapped into PCI configuration space and accessed using PCI configuration bus cycles. The MAC Operational registers can be mapped into either PCI memory or PCI IO space. MII PHY Registers are accessed through MAC Operational Register ENPHY (ENhanced PHY access register, offset 1Ch). SiS900 requires an allocation of 256 bytes of operational register space, and 72 bytes of PCI configuration register space. The detailed definitions for each bit allocated in each registers will be described in section 4.2, 4.3 and 4.4 respectively.

Acronyms mentioned in the PCI configuration registers and MAC Operational registers are defined as follows:

RO Read Only

R/W Read Write

Acronyms mentioned in the MII PHY registers that are defined as follows:

SYM.	NAME	DEFINITION	
		WRITE CYCLE	READ CYCLE
W	Write	Input	No Operation
R	Read	No Operation	Output
R/W	Read/Write	Input	Output
R/WSC	Read/Write Self Cleaning	Input	Output Clears itself After Operation Complete
R/LL	Read/Latching Low	No Operation	Output When Bit Goes Low, Bit Latched. When Bit is Read, Bit Updated.
R/LH	Read/Latching High	No Operation	Output When Bit Goes High, Bit Latched. When Bit is Read, Bit Updated.
R/LT	Read/Latching on Transition	No Operation	Output When Bit Transitions, Bit Latched And Interrupt Set When Bit is Read, Interrupt Clear And Bit Updated.

4.2 PCI Configuration Registers

SiS900 implements a PCI version 2.1 configuration register space. This allows PCI BIOS to "soft" configure SiS900. Software Reset has no effect on configuration registers. Hardware Reset returns all configuration registers to their hardware reset state. For all reserved registers, a write are ignored, and a read return 0.

Table 4-1 Configuration Register Map

OFFSET	TAG	DESCRIPTION	ACCESS	SECTION
00h	CFGID	Configuration Identification Register	RO	4.2.1
04h	CFGCS	Configuration Command and Status Register	R/W	4.2.2
08h	CFGRID	Configuration Revision ID Register	RO	4.2.3
0Ch	CFGLAT	Configuration Latency Timer Register	R/W	4.2.4
10h	CFGIOA	Configuration IO Base Address Register	R/W	4.2.5
14h	CFGMA	Configuration Memory Address Register	R/W	4.2.6
18h-28h		RESERVED (reads return zero).		
2Ch	CFGSID	Configuration Subsystem Identification Register	RO	4.2.7
30h	CFGEROMA	Configuration Expansion ROM Base Address Register	R/W	4.2.8
34h	CFGCAP	Configuration Capabilities Pointer Register	RO	4.2.9
38h		RESERVED (reads return zero).		
3Ch	CFGINT	Configuration Interrupt Select Register	R/W	4.2.10
40h	CFGPMC	Configuration Power Management Capabilities Register	RO	4.2.11
44h	CFGPMCSR	Configuration Power Management Control and Status Register	R/W	4.2.12
48-FFh		RESERVED (reads return zero).		

4.2.1 Configuration Identification Register

This register identifies SiS900 to PCI system software.

Tag: CFGID Size: 32 bits Hard Reset: unchanged
Offset: 00h Access: Read Only Soft Reset: unchanged

BIT	TAG	DESCRIPTION	R/W	USAGE
31-16	DEVID	Device ID	RO	This field is read-only and is set to the device ID 0900h assigned by SiS if auto load is not enabled. If auto load is enabled, it is set to the device ID stored in Serial EEPROM.
15-0	VENID	Vendor ID	RO	This field is read-only and is set to a value of 1039h that is SiS's PCI Vendor ID if auto load is not enabled. If auto load is enabled, it is set to the vendor ID stored in EEPROM.

4.2.2 Configuration Command and Status Register

The CFGCS register has two parts. The upper 16-bits (31-16) is devoted to device status. The lower 16-bits (15-0) is devoted to command and are used to configure and control the device.

Tag: CFGCS Size: 32 bits Hard Reset: 02900000h
Offset: 04h Access: Read Write Soft Reset: unchanged

BIT	TAG	DESCRIPTION	R/W	USAGE
31	DPERR	Detected Parity Error	R/W	SiS900 sets this bit whenever a parity error is detected, even if the parity error handling is disabled (controlled by command register bit 6). SW writes '1' to this bit will clear this bit. SW writes '0' to this bit leaves this bit unchanged.
30	SSERR	Signaled SERR	R/W	This bit is set whenever SiS900 asserts SERR#. SW writes '1' to this bit will clear this bit. SW writes '0' to this bit leaves this bit unchanged.
29	RMABT	Received Master Abort	R/W	SiS900 sets this bit whenever its master transaction is terminated with Master-Abort. SW writes '0' to this bit leaves this bit unchanged.
28	RTABT	Received Target Abort	R/W	SiS900 sets this bit whenever its master transaction is terminated with Target-Abort. SW writes '0' to this bit leaves this bit unchanged.
27	STABT	Sent Target Abort	R/W	SiS900 sets this bit whenever it terminates a target transaction with Target-Abort. SW writes '0' to this bit leaves this bit unchanged.
26-25	DSTIM	DEVSEL Timing	RO	This field will always be set to 01 indicating that SiS900 supports "medium" DEVSEL timing.
24	DPD	Data Parity Detected	R/W	This bit is set when three conditions are met: (1) the bus agent asserted PERR# itself or observed PERR# asserted; (2) SiS900 acted as the bus master for the operation in which the error occurred; and (3) the Parity Error Response bit in command register is set. SW writes '0' to this bit leaves this bit unchanged.

23	FBB	Fast Back-to-Back Capable	RO	SiS900 will set this bit to 1.
22	UDF	User Definable Features Supported	RO	SiS900 do not support User Definable Features, and therefore reads will return a 0.
21	66M	66MHz Capable	RO	SiS900 is not 66MHz capable. Reads will return a 0.
20	CAP	Capabilities	RO	SiS900 will set this bit to 1 indicating implementation of extended capabilities (PCI power management).
19-16				RESERVED (reads return 0).
15-10				RESERVED (reads return 0).
9	FBBEN	Fast Back-to-Back Enable	R/W	Set to 1 by the PCI BIOS to enable SiS900 to do Fast Back-to-Back transfers (FBB transfers as a master is not implemented in the current revision).
8	SERREN	SERR# Enable	R/W	When set, SiS900 will generate SERR# when an address parity error is detected.
7	STEP	Address Data Stepping	RO	This bit is hardwired to 0 for SiS900 never do stepping.
6	PERRSP	Parity Error Response	R/W	When set, SiS900 will assert PERR# on the detection of a data parity error when acting as the target, and will sample PERR# when acting as the initiator. When reset, data parity errors are ignored. The action taken is specified by CFG: PESEL.
5	SNOOP	VGA Palette Snoop	RO	SiS900 does not implement this bit. Reads will return a 0.
4	MWINV	Memory Write and Invalidate Enable	RO	Set to 0 indicating that SiS900 will not generate the Memory Write and Invalidate command.
3	SPECYC	Special Cycles	RO	Set to 0 indicating that SiS900 will ignore all Special Cycle operations.
2	BMEN	Bus Master Enable	R/W	When set, SiS900 is allowed to act as a PCI bus master. When reset, SiS900 is prohibited from acting as a PCI bus master.
1	MSEN	Memory Space Access	R/W	When set, SiS900 responds to memory space accesses. When reset, SiS900 ignores memory space accesses.
0	IOSEN	IO Space Access	R/W	When set, SiS900 responds to IO space accesses. When reset, SiS900 ignores IO space accesses.

4.2.3 Configuration Revision ID Register

This register stores silicon revision number, revision number of software interface specification and lets the configuration software know that it is an Ethernet controller in the class of network controllers.

Tag:	CFGRID	Size:	32 bits	Hard Reset:	02000000h
Offset:	08h	Access:	Read Only	Soft Reset:	unchanged

BIT	TAG	DESCRIPTION	R/W	USAGE

31-24	BASECL	Base Class	RO	Returns 02 which specifies a network controller
23-16	SUBCL	Sub Class	RO	Returns 00, which specifies an Ethernet controller.
15-8	PROGIF	Programming IF	RO	Returns 00, which specifies the first release of SiS900 Software Interface Specification
7-0	REVID	Silicon Revision	RO	Returns 00, which specifies the silicon revision.

4.2.4 Configuration Latency Timer Register

This register gives status and controls such miscellaneous functions as BIST, Latency timer and Cache line size.

Tag: CFGLAT Size: 32 bits Hard Reset: 00000000h
Offset: 0Ch Access: Read Write Soft Reset: unchanged

BIT	TAG	DESCRIPTION	R/W	USAGE
31-24	BIST	Built-in Self Test	RO	SiS900 do not support BIST. Read will return 0, write is ignored.
23-16	HEAD	Header Type	RO	00h
15-8	LAT	Latency Timer	R/W	Set by software to the number of PCI clocks that SiS900 may hold the PCI bus.
7-0	CLS	Cache Line Size	RO	Ignored by SiS900.

4.2.5 Configuration IO Base Address Register

This register specifies the Base I/O address that is required to build an address map during configuration. It also specifies the number of bytes required as well as an indication that it can be mapped into I/O space.

Tag: CFGIOA Size: 32 bits Hard Reset: 00000001h
Offset: 10h Access: Read Write Soft Reset: unchanged

BIT	TAG	DESCRIPTION	R/W	USAGE
31-8	IOBASE	Base IO Address	R/W	This is set by software to the base IO address for the Operational Register Map.
7-2	IOSIZE	Size indication	RO	Read back as 0. This allows the PCI bridge to determine that SiS900 requires 256 bytes of IO space.
1				RESERVED (reads return 0)
0	IOIND	IO Space Indicator	RO	Set to 1 by SiS900 to indicate that SiS900 is capable of being mapped into IO space.

4.2.6 Configuration Memory Address Register

This register specifies the Base Memory address that is required to build an address map during configuration. It also specifies the number of bytes required as well as an indication that it can be mapped into memory space.

Tag: CFGMA Size: 32 bits Hard Reset: 00000000h
Offset: 14h Access: Read Write Soft Reset: unchanged

BIT	TAG	DESCRIPTION	R/W	USAGE

31-12	MEMBASE	Memory Base Address	R/W	This is set by software to the base address for the Operational Register Map.
11-4	MEMSIZE	Memory Size	RO	These bits return 0, which indicates that SiS900 requires 4096 bytes of Memory Space (the minimum recommended allocation)
3	MEMPF	Prefetchable	RO	Set to 0 by SiS900 to indicate that SiS900 does not support this feature.
2-1	MEMLOC	Location Selection	RO	Set to 00 by SiS900. This indicates that the base register is 32-bits wide and can be placed anywhere in the 32-bit memory space.
0	MEMIND	Memory Space Indicator	RO	Set to 0 by SiS900 to indicate that SiS900 is capable of being mapped into memory space.

4.2.7 Configuration Subsystem Identification Register

The CFGSID allows system software to distinguish between different subsystems based on the same PCI silicon.

Tag: CFGSID Size: 32 bits Hard Reset: unchanged
Offset: 2Ch Access: Read Only Soft Reset: unchanged

BIT	TAG	DESCRIPTION	R/W	USAGE
31-16	SDEVID	Subsystem Device ID	RO	This field is set to the device ID 0900h assigned by SiS if auto load is not enabled. If auto load is enabled, it is set to the subsystem ID stored in EEPROM.
15-0	SVENID	Subsystem Vendor ID	RO	This field is set to a value of 1039h, which is SiS's PCI Vendor ID if auto load is not enabled. If auto load is enabled, it is set to the subvendor ID stored in EEPROM.

4.2.8 Configuration Expansion ROM Base Address Register

This register specifies the Base Expansion ROM address that is required to build an address map during configuration. It also specifies the number of bytes required as well as an indication that the device accepts accesses to its expansion ROM.

Tag: CFGEROMA Size: 32 bits Hard Reset: 00000000h
Offset: 30h Access: Read Write Soft Reset: unchanged

BIT	TAG	DESCRIPTION	R/W	USAGE
31-17	EROMBASE	Expansion ROM Base Address	R/W	This is set by software to the base address for the Expansion ROM.
16-1				RESERVED (reads return 0)
0	EROMEN	Expansion ROM address decode enable	R/W	This SiS900 will respond to access its expansion ROM when this bit is set and the Memory Space Access bit is set.

4.2.9 Configuration Capabilities Pointer Register

Tag: CFGCAP Size: 32 bits Hard Reset: 00000040h

Offset: 34h Access: Read Only Soft Reset: unchanged

BIT	TAG	DESCRIPTION	R/W	USAGE
31-8				RESERVED (reads return 0)
7-0	CAPTR	Capabilities Pointer	RO	It provides an offset into PCI configuration space for the location of the first item in the capabilities linked list. Hardwired to 40'h in SiS900 to point to CFGPMC.

4.2.10 Configuration Interrupt Select Register

This register stores the interrupt line number as identified by the POST software that is connected to the interrupt controller as well as SiS900 desired settings for maximum latency and minimum grant.

Tag: CFGINT Size: 32 bits Hard Reset: 0b340100h
Offset: 3Ch Access: Read Write Soft Reset: unchanged

BIT	TAG	DESCRIPTION	R/W	USAGE
31-24	MXLAT	Maximum Latency	RO	SiS900 desired setting for Max Latency. SiS900 will initialize this field to 0B (2.75 μsec).
23-16	MNGNT	Minimum Grant	RO	SiS900 desired setting for Minimum Grant. SiS900 will initialize this field to 34 (13 μsec)
15-8	IPIN	Interrupt Pin	RO	Always return 0000 0001 (INTA)
7-0	ILINE	Interrupt Line	R/W	Set to which line on the interrupt controller that SiS900's interrupt pin is connected to.

4.2.11 Configuration Power Management Capabilities Register

SiS900 supports both PCI Bus Power Management Interface specifications. revision 1.0 and revision 1.0a. If auto load is enabled, the CFGPMC register is 1.0a version, otherwise it is 1.0 version.

1.0 version:

Tag: CFGPMC Size: 32 bits Hard Reset: unchanged
Offset: 40h Access: Read Only Soft Reset: unchanged

BIT	TAG	DESCRIPTION	R/W	USAGE
31-27	PMESP	PME Support	RO	Indicates PME# may be asserted from which power state. If Auxiliary Power Source is present, this 5-bit field is 11111b indicating PME# can be asserted from D0, D1, D2, D3hot and D3cold. If Auxiliary Power Source is absent, this 5-bit field is 01111b indicating PME# can be asserted from D0, D1, D2 and D3hot but cannot be asserted from D3cold.
26	D2SP	D2 Support	RO	Set to 1 by SiS900 to indicate that SiS900 supports D2 Power Management State.
25	D1SP	D1 Support	RO	Set to 1 by SiS900 to indicate that SiS900 supports D1 Power Management State.
24-22				RESERVED (reads return 0).
21	DSI	Device Specific Initialization	RO	Set to 0 by SiS900 to indicate that SiS900 does not require a device specific initialization sequence

				following transition to the D0 uninitialized state.
20				RESERVED (reads return 0)
19	PMECLK	PME Clock	RO	Set to 0 by SiS900 to indicate that no PCI clock is required for SiS900 to generate PME#.
18-16	PMVER	PCI PM Spec. Version	RO	Set to 001b indicates that SiS900 complies with Revision 1.0 of the PCI Power Management Interface Specification.
15-8	NIPTR	Next Item Pointer	RO	Set to 00h by SiS900 to indicate that no additional items in the Capabilities List.
7-0	CAPID	Capability ID	RO	Set to 01h by SiS900 to indicate that the linked list item as being the PCI Power Management registers.

1.0a version:

Tag: CFGPMC Size: 32 bits Hard Reset: unchanged

Offset: 40h Access: Read Only Soft Reset: unchanged

BIT	TAG	DESCRIPTION	R/W	USAGE
31-27	PMESP	PME Support	RO	Indicates PME# may be asserted from which power state. If Auxiliary Power Source is present, this 5-bit field is 11111b indicating PME# can be asserted from D0, D1, D2, D3hot and D3cold. If Auxiliary Power Source is absent, this 5-bit field is 01111b indicating PME# can be asserted from D0, D1, D2 and D3hot but cannot be asserted from D3cold.
26	D2SP	D2 Support	RO	Set to 1 by SiS900 to indicate that SiS900 supports D2 Power Management State.
25	D1SP	D1 Support	RO	Set to 1 by SiS900 to indicate that SiS900 supports D1 Power Management State.
24-22	IAUX	Auxiliary Current	RO	This field reports the 3.3Vaux auxiliary current requirements for SiS900.
21	DSI	Device Specific Initialization	RO	Set to 0 by SiS900 to indicate that SiS900 does not require a device specific initialization sequence following transition to the D0 uninitialized state.
20				RESERVED (reads return 0)
19	PMECLK	PME Clock	RO	Set to 0 by SiS900 to indicate that no PCI clock is required for SiS900 to generate PME#.
18-16	PMVER	PCI PM Spec. Version	RO	Set to 010b indicates that SiS900 complies with Revision 1.0a of the PCI Power Management Interface Specification.
15-8	NIPTR	Next Item Pointer	RO	Set to 00h by SiS900 to indicate that no additional items in the Capabilities List.
7-0	CAPID	Capability ID	RO	Set to 01h by SiS900 to indicate that the linked list item as being the PCI Power Management registers.

4.2.12 Configuration Power Management Control/Status Register

This register is used to manage SiS900's power management state as well as to enable/monitor PME.

Tag: CFGPMCSR Size: 32 bits Hard Reset: (see below)
Offset: 44h Access: Read Write Soft Reset: unchanged

BIT	TAG	DESCRIPTION	R/W	USAGE
31-24	DATA	State Dependent Data	RO	Not implemented in SiS900 (reads return 0)
23-16	PMCSR_BSE	PMCSR PCI to PCI Bridge Support Extensions	RO	Not implemented in SiS900 (reads return 0)
15	PMESTS	PME Status	R/W	This bit is set when SiS900 would normally assert the PME# signal independent of the state of the PME_EN bit. Writing a '1' to this bit will clear it and cause SiS900 to stop asserting a PME# (if enabled). Writing a '0' has no effect. If Auxiliary Power Source is present, i.e. PME# can be asserted from D3cold, then this bit must be explicitly cleared by the operating system each time the operating system is initially loaded. Unchanged by hardware reset.
14-13	DATASCA	Data Scale	RO	Not implemented in SiS900 (reads return 0)
12-9	DATASEL	Data Select	RO	Not implemented in SiS900 (reads return 0)
8	PME_EN	PME Enable	R/W	Writing a '1' enables SiS900 to assert PME#. Writing a '0', PME# assertion is disabled. If Auxiliary Power Source is present, i.e. PME# can be asserted from D3cold, then this bit must be explicitly cleared by the operating system each time the operating system is initially loaded. Unchanged by hardware reset.
7-2				RESERVED (reads return 0)
1-0	PWRSTA	Power State	R/W	This 2-bit field is used both to determine the current power state of SiS900 and to set SiS900 into a new power state. The hardware reset value is 00b. The definition of the field values is given below. 00b D0 01b D1 10b D2 11b D3hot

4.3 MAC Operational Registers

SiS900 provides the following set of operational registers mapped into PCI memory space or I/O space. Writes to reserved register locations may result in unexpected behavior. Reads to reserved register locations will return unspecified value.

Table 4-2 Operational Register Map

OFFSET	TAG	DESCRIPTION	ACCESS	SECTION
00h	CR	Command Register	R/W	4.3.1
04h	CFG	Configuration Register	R/W	4.3.2
08h	EROMAR	EEPROM Access Register	R/W	4.3.3
0Ch	PTSCR	PCI Test Control Register	R/W	4.3.4
10h	ISR	Interrupt Status Register	R/W	4.3.5
14h	IMR	Interrupt Mask Register	R/W	4.3.6
18h	IER	Interrupt Enable Register	R/W	4.3.7
1Ch	ENPHY	Enhanced PHY Access Register	R/W	4.3.8
20h	TXDP	Transmit Descriptor Pointer Register	R/W	4.3.9
24h	TXCFG	Transmit Configuration Register	R/W	4.3.10
28-2Ch		RESERVED		
30h	RXDP	Receive Descriptor Pointer Register	R/W	4.3.11
34h	RXCFG	Receive Configuration Register	R/W	4.3.12
38h	FLOWCTL	Flow Control Register	R/W	4.3.13
3C-44h		RESERVED		
48h	RFCR	Receive Filter Control Register	R/W	4.3.14
4Ch	RFDR	Receive Filter Data Register	R/W	4.3.15
50-ACh		RESERVED		
B0h	PMCTL	Power Management Control Register	R/W	4.3.16
B4h	PMEVT	Power Management Wake-up Event Register	R/W	4.3.17
B8h		RESERVED		
BCh	WAKECRC	Wake-up Sample Frame CRC Register	R/W	4.3.18
C0-ECh	WAKEMASK	Wake-up Sample Frame Mask Registers	R/W	4.3.19
F0-FCh		RESERVED		

4.3.1 Command Register

This register is used for issuing commands to SiS900. These commands are issued by setting the corresponding bits for the function. Global software reset along with individual reset and enable/disable switches for transmitter and receiver are provided here.

Tag:	CR	Size:	32 bits	Hard Reset:	00000000h
Offset:	0000h	Access:	Read Write	Soft Reset:	00000000h

BIT	TAG	DESCRIPTION	R/W	USAGE
31-9				RESERVED
8	RST	Reset	R/W	Set to 1 to force SiS900 to a soft reset state, which disables the transmitter and receiver, reinitializes the FIFOs, and resets all affected registers to their soft reset state. This operation implies both a TXR and a RXR. This bit will read back a 1 during the reset operation, and be cleared to 0 by the hardware when the reset operation is complete.
7	SWI	Software Interrupt	R/W	Setting this bit to a 1 forces SiS900 to generate a hardware interrupt. This interrupt is maskable via the IMR.
6				RESERVED
5	RXR	Receiver Reset	R/W	When set to a 1, this bit causes the current packet reception to be aborted, the receiver data and status FIFOs to be flushed, and the receiver state machine to enter the idle state (RXE goes to 0). This is a write-only bit and is always read back as 0.
4	TXR	Transmit Reset	R/W	When set to a 1, this bit causes the current transmission to be aborted, the transmitter data and status FIFOs to be flushed, and the transmitter state machine to enter the idle state (TXE goes to 0). This is a write-only bit and is always read back as 0.
3	RXD	Receiver Disable	R/W	Disable the receiver's state machine after any current packets in progress. When this operation has been completed the RXE bit will be cleared to 0. This is a write-only bit and is always read back as 0. If the programmer is silly enough to set both RXD and RXE in the same write, the RXE will be ignored, and RXD will have precedence.
2	RXE	Receiver Enable	R/W	When set to a 1, and the receiver's state machine is idle, then the receiver's machine becomes active. This bit will read back as a 1 whenever the receive state machine is active. After initial power-up, software must insure that the receiver has completely reset before setting this bit (see ISR:RXRCMP)
1	TXD	Transmit Disable	R/W	When set to a 1, halts the transmitter after the completion of the current packet. This is a write-only bit and is always read back as 0. If the

				programmer is silly enough to set both TXD and TXE in the same write, the TXE will be ignored, and TXD will have precedence.
0	TXE	Transmit Enable	R/W	When set to a 1, and the transmit state machine is idle, then the transmit state machine becomes active. This bit will read back as a 1 whenever the transmit state machine is active. After initial power-up, software must insure that the transmitter has completely reset before setting this bit (see ISR:TXRCMP)

4.3.2 Configuration Register

Tag: CFG Size: 32 bits Hard Reset: 00000000h
Offset: 0004h Access: Read Write Soft Reset: 00000000h

BIT	TAG	DESCRIPTION	R/W	USAGE
31-8				RESERVED
7	REQALG	PCI Bus Request Algorithm	R/W	Selects mode for making requests for the PCI bus. When set to 0 (default), SiS900 will use an aggressive Request scheme. When set to a 1, SiS900 will use a more conservative scheme.
6	SB	Single Backoff	R/W	Setting this bit to 1 forces the transmitter backoff state machine to always backoff for a single 802.3 slot time instead of following the 802.3 random backoff algorithm. 0 (default) allows normal transmitter backoff operation.
5	POW	Program Out of Window Timer	R/W	This bit controls when the Out of Window collision timer begins counting its 512-bit slot time. A 0 causes the timer to start after the SFD is received. A 1 causes the timer to start after the first bit of the preamble is received.
4	EXD	Excessive Deferral Timer disable	R/W	Setting this bit to 1 will inhibit transmit errors due to excessive deferral. This will inhibit the setting of the ED status.
3	PESEL	Parity Error Detection Action	R/W	This bit control the assertion of SERR when a data parity error is detected while SiS900 is acting as the bus master. When set, parity errors will not result in the assertion of SERR. When reset, parity errors will result in the assertion of SERR, indicating a system error.
2-1				RESERVED
0	BEM	Big Endian Mode	R/W	When set, SiS900 will perform bus-mastered data transfers in “big endian” mode. Note that access to register space is unaffected by the setting of this bit.

4.3.3 Serial EEPROM Access Register

The Serial EEPROM Access Register provides an interface for software access to the serial EEPROM.

Tag: EROMAR Size: 32 bits Hard Reset: 00000000h
Offset: 0008h Access: Read Write Soft Reset: 00000000h

BIT	TAG	DESCRIPTION	R/W	USAGE
31-4				RESERVED
3	EECS	EEPROM Chip Select	R/W	Controls the value of the EECS pin. When set, the EECS pin is 1; when clear the EECS pin is 0.
2	EESK	EEPROM Serial Clock	R/W	Controls the value of the EESK pin. When set, the EESK pin is 1; when clear the EESK pin is 0.
1	EEDO	EEPROM Data Out	RO	Returns the current state of the EEDO/PA2 pin when EECS is 1. When EECS is 0, this bit returns 0.
0	EEDI	EEPROM Data In	R/W	Controls the value of the EEDI pin.

4.3.4 PCI Test Control Register

Tag: PTSCR Size: 32 bits Hard Reset: 34000000h
Offset: 000Ch Access: Read Write Soft Reset: 34000000h

BIT	TAG	DESCRIPTION	R/W	USAGE
31				RESERVED
30	DISCARD_ TEST	Discard Timer Test Mode	R/W	Setting this bit to 1, the discard timer for delay transaction will have an initial value of 3ff0h. Setting this bit to 0, the initial value of the discard timer will be 0 and the counter expires when up-count to 3fffh. Default value is set to 0.
29-28				RESERVED
27-24	EROM_ TACC	Boot ROM Access Time	R/W	This field adjusts the boot ROM access time. The default value is 0100b that equal to 4 PCI clocks.
23-21				RESERVED
20-12	TRRAMADR	TX/RX RAM address	R/W	Used as the address for the Transmit/Receive data FIFO when accessed through TXCFG/RXCFG during RAM test mode.
11-10				RESERVED
9	BMTEN	Bus Master Test Enable	R/W	When enabled (set to 1), the bus master test mode allows the TX buffer manager to be used as a bus master read cycle generator, and the RX buffer manager to be used as a bus master write cycle generator. While in this test mode, normal buffer manager operation is inhibited. The BMTEN bit should only be set to 1 after the TX and RX have been reset and disabled. After setting BMTEN to 0, the TX and RX must be reset and reconfigured to allow normal operation to resume.
8				RESERVED
7	RRTMEN	Receive RAM Test Mode Enable	R/W	Set this bit to 1 to enable Receive RAM Test mode, which will allow read/write access to the RX data FIFO. The address is specified in bit20-12 RAM address field. The data is written to or read from the RXCFG register.
6	TRTMEN	Transmit RAM Test Mode Enable	R/W	Set this bit to 1 to enable Transmit RAM Test mode, which will allow read/write access to the

				TX data FIFO. The address is specified in bit20-12 RAM address field. The data is written to or read from the TXCFG register.
5	SRTMEN	Status RAM Test Mode Enable	R/W	Set this bit to 1 to enable Status RAM Test mode, which will allow read/write access to the RX status FIFO. The address is specified in bit4-0 Status RAM address field. The data is written to or read from the RXCFG register.
4-0	SRAMADR	Status RAM address	R/W	Used as the address for the receiver status FIFO when accessed through RXCFG during RAM test mode.

Bus Master Read Cycle Test Mode Generation

When the BMTEN bit is set to 1, the TX buffer manager will generate bus master read cycles on command. Several of the TX operational register bit fields are redefined to facilitate control of this mode.

TXDP	Read cycle starting address (dword aligned only).
TXCFG:DRTH	Length of read cycle in bytes (1-335 bytes). The actual length value is derived as follows: length[8:0] = {DRTH[5], 0, DRTH[4], 0, 0, DRTH[3:0]}. **NOTE**: TXCFG:MXDMA is still utilized while in this test mode to control the maximum DMA size. It is recommended that TXCFG:MXDMA be set to 0 so that the byte count in TXCFG:DRTH will control the DMA length.
CR:TXE	Write a "1" to this bit will invoke the read cycle.

The sequence required to generate bus master read cycle is as follows:

1. Write a 1 to CR:TXR (not necessary if this mode is invoked immediately after reset)
2. Write a 1 to PTSCR:BMTEN
3. Write a Dword aligned starting address to the TXDP reg
4. Write a byte length to the TXCFG:DRTH
5. Write a 1 to the CR:TXE

All data read during this bus master cycle is discarded (bit bucket). Read cycles can be initiated repetitively without resetting TX between cycles. TXDP, and TXCFG data are retained between cycles.

Bus Master Write Cycle Test Mode Generation

When the BMTEN bit is set to 1, the RX buffer manager will generate bus master write cycles on command. Several of the RX operational register bit fields are redefined to facilitate control of this mode.

RXDP	Write cycle starting address (Dword aligned only).
RXCFG:DRTH	Length of write cycle in bytes (1-335 bytes). The actual length value is derived as follows: length[8:0] = {DRTH[5], 0, DRTH[4], 0, 0, DRTH[3:0]}. NOTE: RXCFG:MXDMA is still utilized while in this test mode to control the maximum DMA size. It is recommended that RXCFG:MXDMA be set to 0 so that the byte count in the RXCFG:DRTH bits will control the DMA length.
RXstatus[22:0]	Write cycle data (this data byte value is used for all byte lanes – see below for data pattern)

CR:RXE Writing a "1" to this bit will invoke the write cycle

Data from the Receive status FIFO is used to provide the bus data for the write cycles. A location in the RX status FIFO must be written and read using RAM test mode to initialize the desired data pattern. The status data mapping used for each byte lane (little endian) during the generated write cycles is as follows:

byte 0 : status[7:0]

byte 1 : status[15:8]

byte 2 : {status[0], status[22:16]}

byte 3 : status[8:1]

The sequence required to generate bus master write cycle is as follows:

1. Write a 1 to CR:RXR (not necessary if this mode is invoked immediately after reset)
2. Write a 1 to PTSCR:SRTMEN and 00000 to PTSCR:SRAMADR[4:0]
3. Write desired data pattern to RXCFG (Note: Only bits 22-0 are used)
4. Read RXCFG
5. Write a 1 to PTSCR:BMTEN
6. Write a dword aligned starting address to the RXDP register
7. Write a byte length to the RXCFG:DRTH
8. Write a 1 to the CR:RXE

Write cycles can be initiated repetitively without resetting RX between cycles. RXDP, RX status, and RXCFG data are retained between cycles.

The sequence from step 1 to step 4 also describes the status RAM test mode procedure, as a example with address 00000. Similarly, Transmit and Receive RAM test mode can be achieved as follows:

1. Write a 1 to CR:TXR (not necessary if this mode is invoked immediately after reset)
2. Write a 1 to PTSCR:TRTMEN and the address to PTSCR:TRRAMADR[20:12]
3. Write desired data pattern to TXCFG
4. Read RXCFG

4.3.5 Interrupt Status Register

This register indicates the source of an interrupt when the INTA pin goes active. Enabling the corresponding bits in the Interrupt Mask Register (IMR) allows bits in this register to produce an interrupt. When an interrupt is active, one or more bits in this register are set to a "1". The Interrupt Status Register reflects all current pending interrupts, regardless of the state of the corresponding mask bit in the IMR. Reading the ISR clears all interrupts. Writing to the ISR has no effect.

Tag: ISR Size: 32 bits Hard Reset: 03008000h

Offset: 0010h Access: Read Only Soft Reset: 03008000h

BIT	TAG	DESCRIPTION	R/W	USAGE
31-29				RESERVED
28	WAKEEVT	Wake Up Event	RO	Indicates that there is wake-up event occurs. This bit is a wired version of PM Event registers bits, it's not a registered one. So this bit will not be cleared by read operation like others status bits do, it is read as '0' when all PM Event registers bits

				are cleared.
27	PAUSE_END	End of Transmission Pause	RO	Indicates pause command is completed when pause timer expires.
26	PAUSE_ST	Start of Transmission Pause	RO	Indicates data transmission is paused.
25	TXRCMP	Transmit Reset Complete	RO	Indicates that a requested transmit reset operation is complete.
24	RXRCMP	Receive Reset Complete	RO	Indicates that a requested receive reset operation is complete.
23	DPERR	Detected Parity Error	RO	This bit is set whenever CFGCS:DPERR is set, but cleared (like all other ISR bits) when the ISR register is read.
22	SSERR	Signaled System Error	RO	SiS900 signaled a system error on the PCI bus.
21	RMABT	Received Master Abort	RO	SiS900 received a master abort on the PCI bus.
20	RTABT	Received Target Abort	RO	SiS900 received a target abort on the PCI bus.
19-17				RESERVED
16	RXSOVR	RX Status FIFO Overrun	RO	Set when an overrun condition occurs on the RX Status FIFO.
15	HIBERR	High Bits Error Set	RO	A logical OR of bits 25-16
14-13				RESERVED
12	SWI	Software Interrupt	RO	Set whenever the SWI bit in the CR register is set.
11				RESERVED
10	TXURN	TX Underrun	RO	Set when a transmit data FIFO underrun condition occurs.
9	TXIDLE	TX Idle	RO	This event is signaled when the transmit state machine enters the idle state from a non-idle state. This will happen whenever the state machine encounters an "end-of-list" condition (NULL link field or a descriptor with OWN clear).
8	TXERR	TX Packet Error	RO	This event is signaled after the last transmit descriptor in a failed transmission attempt that has been updated with valid status.
7	TXDESC	TX Descriptor	RO	This event is signaled after a transmitter descriptor with the INTR bit set in the CMDSTS field that has been updated.
6	TXOK	TX Packet OK	RO	This event is signaled after the last transmit descriptor in a successful transmission attempt has been updated with valid status
5	RXORN	RX Overrun	RO	Set when a receive data FIFO overrun condition occurs.
4	RXIDLE	RX Idle	RO	This event is signaled when the receive state machine enters the idle state from a running state. This will happen whenever the state machine

				encounters an "end-of-list" condition (NULL link field or a descriptor with OWN set).
3	RXEARLY	RX Early Threshold	RO	Indicates that the initial RX Drain Threshold has been met by the incoming packet, and the transfer of the number of bytes specified by the DRTH field in the RXCFG register has been completed by the receive DMA engine. This interrupt condition will occur only once per packet.
2	RXERR	RX Packet Error	RO	This event is signaled after the last receive descriptor in a failed packet reception that has been updated with valid status.
1	RXDESC	RX Descriptor	RO	This event is signaled after a receiver descriptor with the INTR bit set in the CMDSTS field that has been updated.
0	RXOK	RX OK	RO	Set by the receive state machine following the update of the last receive descriptor in a good packet.

4.3.6 Interrupt Mask Register

This register masks the interrupts that can be generated from the ISR. Writing a “1” to the bit enables the corresponding interrupt. During hardware reset, all mask bits are cleared.

Tag: IMR Size: 32 bits Hard Reset: 00000000h
Offset: 0014h Access: Read Write Soft Reset: 00000000h

BIT	TAG	DESCRIPTION	R/W	USAGE
31-29				RESERVED
28	WAKEEVT	Wake Up Event	R/W	When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.
27	PAUSE_END	End of Transmission Pause	R/W	When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.
26	PAUSE_ST	Start of Transmission Pause	R/W	When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.
25	TXRCMP	Transmit Reset Complete	R/W	When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.
24	RXRCMP	Receive Reset Complete	R/W	When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.
23	DPERR	Detected Parity Error	R/W	When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.
22	SSERR	Signaled System Error	R/W	When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.
21	RMABT	Received Master Abort	R/W	When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.
20	RTABT	Received Target Abort	R/W	When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.
19-17				RESERVED
16	RXSOVR	RX Status FIFO	R/W	When this bit is 0, the corresponding bit in the ISR

		Overrun		will not cause an interrupt.
15	HIERR	High Bits Error	R/W	When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.
14-13				RESERVED
12	SWI	Software Interrupt	R/W	When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.
11				RESERVED
10	TXURN	TX Underrun	R/W	When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.
9	TXIDLE	TX Idle	R/W	When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.
8	TXERR	TX Packet Error	R/W	When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.
7	TXDESC	TX Descriptor	R/W	When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.
6	TXOK	TX Packet OK	R/W	When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.
5	RXORN	RX Overrun	R/W	When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.
4	RXIDLE	RX Idle	R/W	When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.
3	RXEARLY	RX Early Threshold	R/W	When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.
2	RXERR	RX Packet Error	R/W	When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.
1	RXDESC	RX Descriptor	R/W	When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.
0	RXOK	RX OK	R/W	When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.

The Interrupt Mask Register provides a mechanism for enabling individual interrupt sources in the Interrupt Status Register (ISR). Setting a mask bit allows the corresponding bit in the ISR to cause an interrupt. ISR bits are always set to 1, however, if the condition is present, regardless of the state of the corresponding mask bit.

4.3.7 Interrupt Enable Register

The Interrupt Enable Register controls the hardware INTR signal.

Tag:	IER	Size:	32 bits	Hard Reset:	00000000h
Offset:	0018h	Access:	Read Write	Soft Reset:	00000000h

BIT	TAG	DESCRIPTION	R/W	USAGE
31-1				RESERVED
0	IE	Interrupt Enable	R/W	When set to 1, the hardware INTR signal is enabled. When set to 0, the hardware INTR signal will be masked, and no interrupts will be generated. The setting of this bit has no effect on the ISR or IMR. This provides the ability to disable the hardware interrupt to the host with a

				single access (eliminating the need for a read-modify-write cycle).

4.3.8 Enhanced PHY Access Register

SiS900 provides ten internal MII PHY registers for internal PHY configuration settings and status readings. Driver can access the ten internal MII registers by defining the command, Register offset, desired data from the ENPHY resister listed below.

Tag: ENPHY Size: 32 bits Hard Reset: 00000000h
Offset: 001Ch Access: Read Write Soft Reset: 00000000h

BIT	TAG	DESCRIPTION	R/W	USAGE
31-16	PHYDATA	R/W PHY Data	R/W	When write, this field specifies the data written to PHY register. When read, this field contains the data returned by PHY.
15-11				RESERVED
10-6	REGADDR	Register Address of PHY	R/W	Indicates the offset of PHY register.
5	RWCMD	Access CMD to PHY	R/W	When '1', HW will issue a read operation to PHY registers, when '0', HW will issue a write operation. This field is valid only when bit 4 is '1'.
4	ACCESS	SW Access Request/HW Done	R/W	When SW wants to access PHY register, it sets this bit to request HW. For such operation, HW will perform the access operation in a proper time, when finished, it clears this bit. SW can't change the PHY access contents if the current access is not done.
3-0				RESERVED

4.3.9 Transmit Descriptor Pointer Register

This register points to the current Transmit Descriptor.

Tag: TXDP Size: 32 bits Hard Reset: 00000000h
Offset: 0020h Access: Read Write Soft Reset: 00000000h

BIT	TAG	DESCRIPTION	R/W	USAGE
31-2	TXDP	Transmit Descriptor Pointer	R/W	The current value of transmitter descriptor pointer. When the transmit state machine is idle, software must set TXDP to the address of a completed transmit descriptor. While the transmit state machine is active, TXDP will follow the state machine as it advances through a linked list of active descriptors. If the link field of the current transmit descriptor is NULL (signifying the end of the list), TXDP will not advance, but will remain on the current descriptor. Any subsequent writes to the TXE bit of the CR register will cause the transmit state machine to reread the link field of the current descriptor to check for new descriptors that may have been appended to the end of the list. Transmit descriptors must be aligned on an even 32-bit boundary in host memory (A1-A0 must be

				0).
1-0				RESERVED

4.3.10 Transmit Configuration Register

This register defines the Transmit Configuration for SiS900. It controls such functions as Loopback, Auto Transmit Padding, Fill & Drain Thresholds, and maximum DMA burst size.

Tag:	TXCFG	Size:	32 bits	Hard Reset:	00800102h
Offset:	0024h	Access:	Read Write	Soft Reset:	00800102h

BIT	TAG	DESCRIPTION	R/W	USAGE
31	CSI	Carrier Sense Ignore	R/W	Setting this bit to 1 causes the transmitter to ignore carrier sense activity, which inhibits reporting of CRS status to the transmitter status register. When this bit is 0 (default), the transmitter will monitor the CRS signal during transmission and reflect valid status in the transmitter status register. This bit must be set to enable full-duplex operation.
30	HBI	HeartBeat Ignore	R/W	Setting this bit to 1 causes the transmitter to ignore the heartbeat (CD) pulse that follows the packet transmission. When this bit is set to 0 (default), the transmitter will monitor the heartbeat pulse. This bit must be set to enable full-duplex operation
29	MLB	MAC Loopback	R/W	Setting this bit to a 1 places SiS900 into a controller loopback state which routes all transmit traffic to the receiver, and disables the transmit and receive interfaces of the MII. A 0 in this bit allows normal MAC operation. The transmitter and receiver must be disabled before enabling the loopback mode. (Packets received during MLB mode will reflect loopback status in the receive descriptor‘s CMDSTS.LBP field.)
28	ATP	Automatic Transmit Padding	R/W	Setting this bit to 1 causes the MAC to automatically pad small (runt) transmit packets to the Ethernet minimum size of 64 bytes. This allows driver software to transfer only actual packet data. Setting this bit to 0 disables the automatic padding function, forcing software to control runt padding.
27-25				RESERVED
24-23				Writes are ignored, reads return 01.
22-20	MXDMA	Max DMA Burst Size per TX DMA Burst	R/W	This field sets the maximum size of transmit DMA data bursts according to the following table: 000 128 x 32-bit words (512 bytes) 001 1 x 32-bit word (4 bytes) 010 2 x 32-bit words (8 bytes) 011 4 x 32-bit words (16 bytes) 100 8 x 32-bit words (32 bytes) 101 16 x 32-bit words (64 bytes) 110 32 x 32-bit words (128 bytes) 111 64 x 32-bit words (256 bytes)
19-14				RESERVED

13-8	FLTH	TX Fill Threshold	R/W	Specifies the fill threshold in units of 32 bytes. When the number of available bytes in the transmitter FIFO reaches this level, the transmit bus master state machine will be allowed to request the PCI bus for transmit packet fragment reads. A value of 0 in this field will produce unexpected results and must not be used.
7-6				RESERVED
5-0	DRTH	TX Drain Threshold	R/W	Specifies the drain threshold in units of 32 bytes. When the number of bytes in the FIFO reaches this level (or the FIFO contains at least one complete packet) the MAC transmit state machine will begin the transmission of a packet. NOTE: In order to prevent a deadlock condition from occurring, the transmit drain threshold should never be set higher than the (TXFIFOSize – TXCFG:FLTH). A value of 0 in this field will produce unexpected results and must not be used.

4.3.11 Receive Descriptor Pointer Register

This register points to the current Receive Descriptor.

Tag:	RXDP	Size:	32 bits	Hard Reset:	00000000h
Offset:	0030h	Access:	Read Write	Soft Reset:	00000000h

BIT	TAG	DESCRIPTION	R/W	USAGE
31-2	RXDP	Receive Descriptor Pointer	R/W	The current value of the receiver descriptor pointer. When the receive state machine is idle, software must set RXDP to the address of an available receive descriptor. While the receive state machine is active, RXDP will follow the state machine as it advances through a linked list of available descriptors. If the link field of the current receive descriptor is NULL (signifying the end of the list), RXDP will not advance, but will remain on the current descriptor. Any subsequent writes to the RXE bit of the CR register will cause the receive state machine to reread the link field of the current descriptor to check for new descriptors that may have been appended to the end of the list. Software should not write to this register unless the receive state machine is idle. Receive descriptors must be aligned on 32-bit boundaries (A1-A0 must be zero).
1-0				RESERVED

4.3.12 Receive Configuration Register

This register is used to set the receiver configuration for SiS900. Receive properties such as accepting error packets, runt packets, setting the receive drain threshold etc. are controlled here.

Tag:	RXCFG	Size:	32 bits	Hard Reset:	00000002h
Offset:	0034h	Access:	Read Write	Soft Reset:	00000002h

BIT	TAG	DESCRIPTION	R/W	USAGE
31	AEP	Accept Errors Packets	R/W	When set to 1, all packets with CRC, alignment, and/or collision errors will be accepted. When set to 0, all packets with CRC, alignment, and/or collision errors will be rejected if possible. Note that depending on the type of error, some packets may be received with errors, regardless of the setting of AEP. These errors will be indicated in the CMDSTS field of the last descriptor in the packet.
30	ARP	Accept Runt Packets	R/W	When set to 1, all packets under 64 bytes in length without errors are accepted. When this bit is 0, all packets less than 64 bytes in length will be rejected if possible.
29				RESERVED
28	ATX	Accept Transmit Packets	R/W	When set to 1, data received simultaneously to a local transmission (such as during a PMD loopback or full duplex operation) will be accepted as valid received data. Additionally, when set to 1, the receiver will ignore collision activity. When set to 0 (default), all data receive simultaneous to a local transmit will be rejected. This bit must be set to 1 for PMD loopback and full duplex operation.
27	AJAB	Accept Jabber Packets	R/W	When set to 1, all packets over 1518 bytes in length (to a maximum of 2046 bytes) will be accepted and placed in the receive data buffers (if buffers that large are specified in the receive descriptor list). When set to 0, packets larger than 1518 bytes (CRC inclusive) will be rejected if possible. A byte count of 2046 indicates that the packet may have been truncated.
26-23				RESERVED
22-20	MXDMA	Max DMA Burst Size per RX DMA Burst	R/W	This field sets the maximum size of receive DMA data bursts according to the following table: 000 128 x 32-bit words (512 bytes) 001 1 x 32-bit word (4 bytes) 010 2 x 32-bit words (8 bytes) 011 4 x 32-bit words (16 bytes) 100 8 x 32-bit words (32 bytes) 101 16 x 32-bit words (64 bytes) 110 32 x 32-bit words (128 bytes) 111 64 x 32-bit words (256 bytes)
19-6				RESERVED
5-1	DRTH	RX Drain Threshold	R/W	Specifies the drain threshold in units of 8 bytes. When the number of bytes in the receiver FIFO reaches this value (times 8), or the FIFO contains a complete packet, the receive bus master state machine will begin the transfer of data from the FIFO to host memory. Care must be taken when setting DRTH to a value lower than the number of bytes needed to determine if packet should be accepted or rejected. In this case, the packet might be rejected after the bus master operation to begin

				transferring the packet into memory has begun. When this occurs, neither the OK bit nor any error status bit in the descriptor's CMDSTS will be set. A value of 0 is illegal, and the results are undefined. This value is also used to compare with the accumulated packet length for early receive indication. When the accumulated packet length meets or exceeds the DRTH value, the RXEARLY interrupt condition is generated.
0				RESERVED

4.3.13 Flow Control Register

The FLOWCTL register is used to control and configure SiS900 Flow Control logic. The Flow Control Logic is used to detect PAUSE frame packets and control data frame transmission.

Tag: FLOWCTL Size: 32 bits Hard Reset: 00000000h
Offset: 0038h Access: Read Write Soft Reset: 00000000h

BIT	TAG	DESCRIPTION	R/W	USAGE
31-2				RESERVED
1	PAUSE	PAUSE Flag	R/W	When "1" indicates data frame transmission is paused. When "0" transmission is normal. This bit is reset by H/W reset, 900 soft reset, transmit reset, pause timer expires or S/W write 0 to this bit.
0	FLOWEN	Flow Control Enable	R/W	Set to 1, enable the PAUSE frame detection. Set to 0, disable the PAUSE frame detection. This bit is reset only by H/W reset.

4.3.14 Receive Filter Control Register

The RFCR register is used to control and configure SiS900 Receive Filter Control logic. The Receive Filter Control Logic is used to configure destination address filtering of incoming packets.

Tag: RFCR Size: 32 bits Hard Reset: Unchanged
Offset: 0048h Access: Read Write Soft Reset: 00000000h

BIT	TAG	DESCRIPTION	R/W	USAGE
31	RFEN	RX Filter Enable	R/W	When this bit is set to 1, the RX Filter is enabled to qualify incoming packets. When set to 0, receive packet filtering is disabled (i.e. all receive packets are rejected).
30	AAB	Accept All Broadcast	R/W	When set to 1, this bit causes all broadcast address packets to be accepted. When set to 0, no broadcast address packets will be accepted.
29	AAM	Accept All Multicast	R/W	When set to 1, this bit causes all multicast address packets to be accepted. When set to 0, multicast destination addresses must have the appropriate bit set in the multicast hash table mask in order for the packet to be accepted.
28	AAP	Accept All Physical	R/W	When set to 1, this bit causes all physical address packets to be accepted. When set to 0, the

				destination address must match the node address register in order for the packet to be accepted.
27-20				RESERVED
19-16	RFADDR	Receive Filter Address	R/W	Selects which internal receive filter register is accessible via RFDR: 0000 node address octets 1-0 0001 node address octets 3-2 0010 node address octets 5-4 0011 RESERVED 0100 multicast hash table bits 15-0 0101 multicast hash table bits 31-16 0110 multicast hash table bits 47-32 0111 multicast hash table bits 63-48 1000 multicast hash table bits 79-64 1001 multicast hash table bits 95-80 1010 multicast hash table bits 111-96 1011 multicast hash table bits 127-112 others RESERVED
15-0				RESERVED

4.3.15 Receive Filter Data Register

The RFDR register is used for reading from and writing to the internal receive filter registers (unique address register, and the hash table register).

Tag:	RFDR	Size:	32 bits	Hard Reset:	Unchanged
Offset:	004Ch	Access:	Read Write	Soft Reset:	00000000h

BIT	TAG	DESCRIPTION	R/W	USAGE
31-16				RESERVED
15-0	RFDATA	Receive Filter Data	R/W	Receiver Filter Data

The Receive Filter Logic uses the following algorithm when qualifying incoming packets for reception:

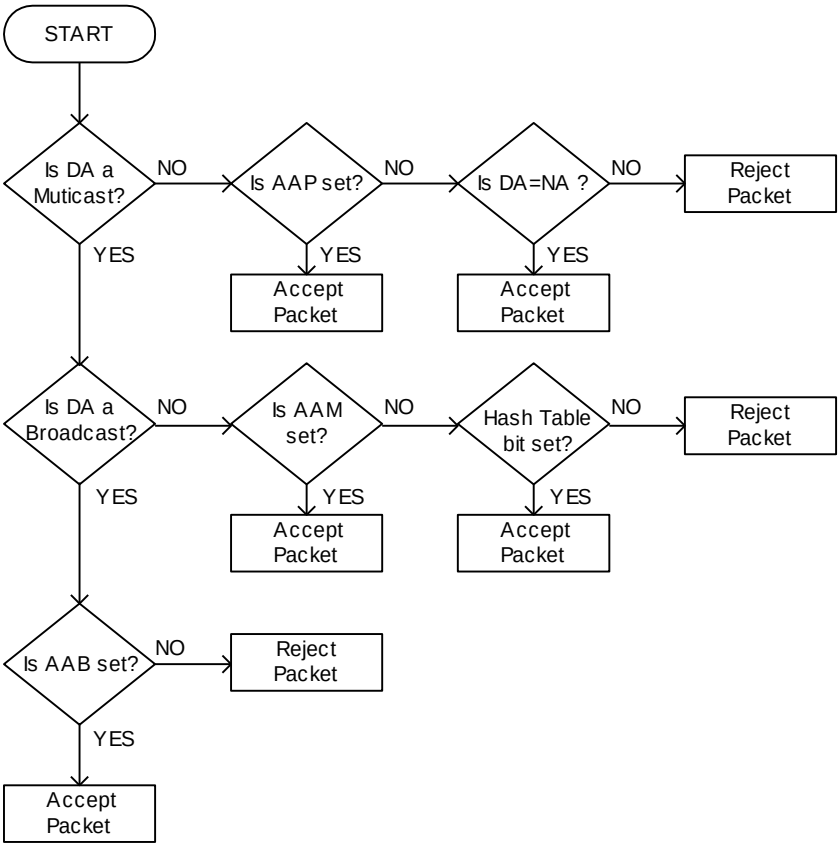
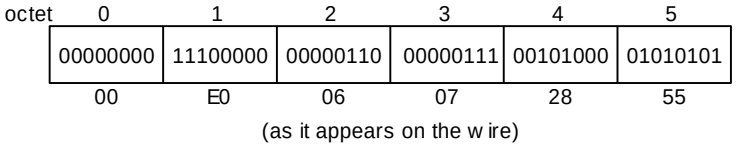


Figure 4-1 Receive Filter Algorithm

The *Node Address* register is a 48-bit register internal to the Receive Filter logic. When RFCR:AAP is clear, then the receive filter logic will only accept unicast packets which match the contents of the node address register. Octet 0 of the node address register corresponds to the first octet of the packet as it appears on the wire. Octet 5 of the node address register corresponds to the last octet of the destination address as it appears on the wire. For example, to configure a node address of 00-E0-06-07-28-55,

Software would need to execute the following series of register operations:




```
out32( RFCR, 0x00000000 );    /* disable receive filter, NA(0) */
out32( RFDR, 0x0000E000 );    /* load octets 0 and 1 */
out32( RFCR, 0x00010000 );    /* select NA[1] */
out32( RFDR, 0x00000706 );    /* load octets 2 and 3 */
out32( RFCR, 0x00020000 );    /* select NA[2] */
out32( RFDR, 0x00005528 );    /* load octets 4 and 5 */
out32( RFCR, 0xC0000000 );    /* enable receive filter, accept broadcasts */
```

The *Multicast Hash Table* register can be configured to perform imperfect filtering of multicast packets. If the receive packet's destination address is a multicast address (but not the broadcast address) and the RFCR:AAM is not set, then the receive filter logic will use the 7 most significant bits of the destination address's CRC as an index into the Multicast Hash Table register. If the corresponding bit is set, then the packet is accepted, otherwise the packet is rejected. Refer to Appendix B - Hash Table Index Computation.

4.3.16 Power Management Control Register

This register provides SW an interface to control which Power Management Event to assert PME# / INTA#. The contents of this register should be well-programmed before set the Ethernet Controller into power saving state, and will not be affected by PCI HW reset. It can be reset by software reset (OP register offset 00h bit8) except ISOSEL.

Tag:	PMCTL	Size:	32 bits	Hard Reset:	unchanged
Offset:	00B0h	Access:	Read Write	Soft Reset:	00000000h

BIT	TAG	DESCRIPTION	R/W	USAGE
31	GATECLK	Gate Dual Target Clock Enable	R/W	When '1', the clock of dual powered blocks will be gated when in (D3cold and (not PME_EN)). When '0', the clock of dual powered blocks will never be gated.
30	WAKEALL	Wake-up While Receive OK Packet	R/W	When '1', any packet that passed the RXFilter with no error will cause a wake-up event. This may include any broadcast, multicast, or direct addressed packet depending on how RXFilter is programmed.
29-27				RESERVED
26	FRM3ACS	3rd Wake-up Frame Access	R/W	When '1', access to WAKECRC is indirectly mapped to the 3rd wake-up frame CRC register. FRM3ACS, FRM2ACS, and FRM1ACS are supposed not to be set at the same time for read access.
25	FRM2ACS	2nd Wake-up Frame Access	R/W	When '1', access to WAKECRC is indirectly mapped to the 2nd wake-up frame CRC register. FRM3ACS, FRM2ACS, and FRM1ACS are supposed not to be set at the same time for read access.
24	FRM1ACS	1st Wake-up Frame Access	R/W	When '1', access to WAKECRC is indirectly mapped to the 1st wake-up frame CRC register. FRM3ACS, FRM2ACS, and FRM1ACS are supposed not to be set at the same time for read access.
23				RESERVED
22	FRM3EN	3rd Wake-up Frame Match Enable	R/W	When this bit is '1', and PME_EN is '1', the 3rd wake-up mechanism of receipt of a network wake-up frame is enabled.
21	FRM2EN	2nd Wake-up Frame Match Enable	R/W	When this bit is '1', and PME_EN is '1', the 2nd wake-up mechanism of receipt of a network wake-up frame is enabled.
20	FRM1EN	1st Wake-up Frame Match	R/W	When this bit is '1', and PME_EN is '1', the 1st wake-up mechanism of receipt of a network

		Enable		wake-up frame is enabled.
19-12				RESERVED
11	ALGORITHM	Magic Packet™ Match Algorithm	R/W	When '1', a strict magic packet match algorithm is used when detect magic packet. When '0', a loose magic packet match algorithm is used when detects magic packet.
10	MAGICPKT	Magic Packet™ Match Enable	R/W	When this bit is '1', and PME_EN is '1', the wake-up mechanism of receipt of a Magic Packet is enabled.
9-2				RESERVED
1	LINKON	Link On Monitor Enable	R/W	When this bit is '1', and PME_EN is '1', the wake-up mechanism of detection the link on state is enabled.
0	LINKLOSS	Link Loss Monitor Enable	R/W	When this bit is '1', and PME_EN is '1', the wake-up mechanism of detection the link loss state is enabled.

4.3.17 Power Management Wake-up Event Register

This register records which wake-up event wake up the system. This register is not affected by PCI HW reset. It can be reset only by software reset (OP register offset 00h bit8). SW writes 1 will clear the individual bits. SW writes 0 will leave the individual bits unchanged.

Tag: PMEVT Size: 32 bits Hard Reset: unchanged

Offset: 00B4h Access: Read Write Soft Reset: 00000000h

BIT	TAG	DESCRIPTION	R/W	USAGE
31				RESERVED
30	ALLFRMMAT	Receive OK Packet	R/W	H/W sets this bit whenever bit30 of PM Control Register is '1' and an incoming packet passes the RXFilter with no error. SW writes '1' to this bit will clear this bit. SW writes '0' to this bit leaves this bit unchanged.
29-23				RESERVED
22	FRM3MAT	Match 3rd Wake-up Sample Frame	R/W	H/W sets this bit whenever bit22 of PM Control Register is '1' and receipt of the pre-defined 3rd wake-up frame with no error. SW writes '1' to this bit will clear this bit. SW writes '0' to this bit leaves this bit unchanged.
21	FRM2MAT	Match 2nd Wake-up Sample Frame	R/W	H/W sets this bit whenever bit21 of PM Control Register is '1' and receipt of the pre-defined 2nd wake-up frame with no error. SW writes '1' to this bit will clear this bit. SW writes '0' to this bit leaves this bit unchanged.
20	FRM1MAT	Match 1st Wake-up Sample Frame	R/W	H/W sets this bit whenever bit20 of PM Control Register is '1' and receipt of the pre-defined 1st wake-up frame with no error. SW writes '1' to this bit will clear this bit. SW writes '0' to this bit leaves this bit unchanged.
19-11				RESERVED
10	MAGICMAT	Magic Packet™	R/W	H/W sets this bit whenever bit10 of PM Control

		Match		Register is '1' and receipt of a magic packet with no error. SW writes '1' to this bit will clear this bit. SW writes '0' to this bit leaves this bit unchanged.
9-2				RESERVED
1	ONEVT	Link On Event	R/W	H/W sets this bit whenever bit1 of PM Control Register is '1' and link status changes from loss to on. SW writes '1' to this bit will clear this bit. SW writes '0' to this bit leaves this bit unchanged.
0	LOSSEVT	Link Loss Event	R/W	H/W sets this bit whenever bit0 of PM Control Register is '1' and link status changes from on to loss. SW writes '1' to this bit will clear this bit. SW writes '0' to this bit leaves this bit unchanged.

4.3.18 Wake-up Sample Frame CRC Register

This register provides an access window to the CRC values of the mask bytes in wake-up sample frames. When FRM3ACS, FRM2ACS, or FRM1ACS is '1', the CRC value of the mask bytes in the corresponding wake-up sample frame can be accessed through this register. FRM3ACS, FRM2ACS, and FRM1ACS are supposed not to be set at the same time for read access. If the CRC value of those incoming bytes, whose byte mask is set to 1 in the sample frame, equals to the CRC value in the sample frame, then the incoming frame is considered a wake-up frame. This register is not affected by PCI HW reset. It can be reset only by software reset (OP register offset 00h bit8).

Tag: WAKECRC Size: 32 bits Hard Reset: unchanged

Offset: 00BCh Access: Read Write Soft Reset: 00000000h

BIT	TAG	DESCRIPTION	R/W	USAGE
31-0	WAKECRC	Wake-up Frame CRC Value	R/W	This field specifies the CRC value of the mask bytes in the corresponding wake-up sample frame specified by FRM3ACS, FRM2ACS, and FRM1ACS. H/W uses this 32-bit CRC value to match the 32-bit CRC value of incoming frame mask bytes. If matched, the incoming frame is a wake-up frame and PME# will be asserted if enabled.

4.3.19 Wake-up Sample Frame Byte Mask Register

These registers provide the mask bytes in wake-up sample frames. These registers are not affected by PCI HW reset. They can be reset by software reset (OP register offset 00h bit8).

OFFSET	SIZE	R/W	DESCRIPTION
C0h	32	R/W	The 1st 32 byte mask in the 1st Wake-up sample frame.
C4h	32	R/W	The 2nd 32 byte mask in the 1st Wake-up sample frame.
C8h	32	R/W	The 3rd 32 byte mask in the 1st Wake-up sample frame.
CCh	32	R/W	The 4th 32 byte mask in the 1st Wake-up sample frame.
D0h	32	R/W	The 1st 32 byte mask in the 2nd Wake-up sample frame.
D4h	32	R/W	The 2nd 32 byte mask in the 2nd Wake-up sample frame.

D8h	32	R/W	The 3rd 32 byte mask in the 2nd Wake-up sample frame.
DCh	32	R/W	The 4th 32 byte mask in the 2nd Wake-up sample frame.
E0h	32	R/W	The 1st 32 byte mask in the 3rd Wake-up sample frame.
E4h	32	R/W	The 2nd 32 byte mask in the 3rd Wake-up sample frame.
E8h	32	R/W	The 3rd 32 byte mask in the 3rd Wake-up sample frame.
ECh	32	R/W	The 4th 32 byte mask in the 3rd Wake-up sample frame.

4.4 MII PHY Registers

SiS900 has eleven internal MII PHY 16 bit registers. Ten registers are available for setting configuration inputs and reading status outputs and one register is reserved for factory use. The ten accessible registers consist of six registers that are defined by IEEE 802.3 specification (MI Register 0-5) and four registers that are unique to SiS900 (MI Register 16-19).

The accesses of the ten MI PHY Registers are through MAC Operational Register ENPHY (offset 1Ch). Users can define the command (RWCMD, ENPHY bit 5), the Register Offset (REGADDR, ENPHY bit 10-6), and the Data contents (PHYDATA, ENPHY bit 31-16). And then the driver issue the access command bit by writing '1' to register ENPHY bit 4, ACCESS, and wait for SiS900 complete the operation which should return '0' when completed.

Table 4-3 PHY Configuration Register Map

OFFSET	TAG	DESCRIPTION	ACCESS	SECTION
00h	CONTROL	MI Register 0 Control Register	RO	4.4.1
01h	STATUS	MI Register 1 Status Register	R/W	4.4.2
02h	PHYID1	MI Register 2 PHY ID#1	RO	4.4.3
03h	PHYID2	MI Register 3 PHY ID#2	R/W	4.4.4
04h	AUTOADV	MI Register 4 Auto Negotiation Advertisement	R/W	4.4.5
00h	AUTOREC	MI Register 5 Auto Negotiation Remote End Capability	R/W	4.4.6
10h	CONFIG1	MI Register 16 Configuration 1	R/W	4.4.7
11h	CONFIG2	MI Register 17 Configuration 2	R/W	4.4.8
12h	STSOUT	MI Register 18 Status Output	R/LT	4.4.9
13h	MASK	MI Register 19 Mask	R/W	4.4.10
14h	RESERVED	MI Register 20 Reserved	R/W	4.4.11

4.4.1 Control Register

Tag: CONTROL Size: 16 bits Hard Reset: 3000h
Offset: 00h Access: Read Write Soft Reset: 3000h

BIT	TAG	DESCRIPTION	R/W	USAGE
15	RST	Reset	R/WSC	1 Reset, Bit Self Cleaning After Reset Completed 0 Normal
14	LPBK	Loopback Enable	R/W	1 Loopback Mode Enabled 0 Normal
13	SPEED	Speed Select	R/W	1 100 Mbps Selected (100Base TX) 0 Normal
12	ANEG_EN	Auto-Negotiation Enable	R/W	1 Auto-Negotiation Enabled 0 Normal
11	PDN	Powerdown Enable	R/W	1 Powerdown 0 Normal
10	MII_DIS	MII Interface Disable	R/W	1 MII Interface Disabled 0 = Normal
9	ANEG_RST	Auto-Negotiation Reset	R/WSC	1 Reset Auto-Negotiation Process, Bit Self Clearing After Reset Completed 0 Normal
8	DPLX	Duplex Mode Select	R/W	1 Full Duplex 0 Half Duplex
7	COLTST	Collision Test Enable	R/W	1 Collision Test Enabled 0 Normal
6-0			R/W	RESERVED

4.4.2 Status Register

Tag: STATUS Size: 16 bits Hard Reset: 7809h
Offset: 01h Access: Read Only Soft Reset: 7809h

BIT	TAG	DESCRIPTION	R/W	USAGE
15	CAP_T4	100Base-T4 Capable	R	0 Not Capable of 100Base-T4 Operation
14	CAP_TXF	100Base-TX Full Duplex Capable	R	1 Capable of 100Base-TX Full Duplex
13	CAP_TXH	100Base-TX Half Duplex Capable	R	1 Capable of 100Base-TX Half Duplex
12	CAP_TF	10Base-T Full Duplex Capable	R	1 Capable of 10Base-T Full Duplex
11	CAP_TH	10Base-T Half Duplex Capable	R	1 Capable of 10Base-T Half Duplex
10-7			R	RESERVED
6	CAP_SUPR	MI Preamble Suppression Capable	R	0 Not Capable of Accepting MI Frames with MI Preamble Suppressed
5	ANEG_ACK	Auto-Negotiation	R	1 Auto-Negotiation Acknowledge Process

		Acknowledge		Complete 0 Normal
4	REM_FLT	Remote Fault Detect	R/LH	1 Remote Fault Detected. This bit is set when Either Interrupt Detect Bit 18.15 or Auto-Negotiation Remote Fault bit 5.13 is set. 0 No Remote Fault
3	CAP_ANEG	Auto-Negotiation Capable	R	1 Capable of Auto-Negotiation Operation
2	LINK	Link Status	R/LL	1 Link Detected (Some As Bit 18.8) 0 Link not detected
1	JAB	Jabber Detect	R/LH	1 Jabber Detected (Some As Bit 18.8) 0 Normal
0	EXREG	Extended Register Capable	R	1 Extended Register Exist

4.4.3 PHY ID #1 Register

Tag: PHYID1 Size: 16 bits Hard Reset: 001Dh
Offset: 02h Access: Read Only Soft Reset: 001Dh

BIT	TAG	DESCRIPTION	R/W	USAGE
15-0	OUI3 OUI4 OUI5 OUI6 OUI7 OUI8 OUI9 OUI10 OUI11 OUI12 OUI13 OUI14 OUI15 OUI16 OUI17 OUI18	Company ID, Bits 3-18	R	OUI = 00-E0-06

4.4.4 PHY ID #2 Register

Tag: PHYID2 Size: 16 bits Hard Reset: 8000h
Offset: 03h Access: Read Only Soft Reset: 8000h

BIT	TAG	DESCRIPTION	R/W	USAGE
15-10	OUI19 OUI20 OUI21 OUI22 OUI23 OUI24	Company ID, Bits 19-24	R	OUI = 00-E0-06
9-4	PART6 PART5 PART4 PART3	Manufacturer's Part Number	R	00_H

	PART2 PART1			
3-0	REV3 REV2 REV1 REV0	Manufacturer's Revision Number	R	00 H

4.4.5 Auto-Negotiation Advertisement Register

Tag: AUTOADV Size: 16 bits Hard Reset: 05E1h
Offset: 04h Access: Read Write Soft Reset: 05E1h

BIT	TAG	DESCRIPTION	R/W	USAGE
15	NP	Next Page Enable	R/W	1 Next Page Exists 0 No Next Page
14	ACK	Acknowledge	R	1 Received Auto-Negotiation Word Recognized 0 Not Recognized
13	RF	Remote Fault Enable	R/W	1 Auto-Negotiation Remote Fault Detected 0 No Remote Fault
12-11			R/W	RESERVED
10	PAUSE	Pause Operation for Full Duplex Link	R/W	1 Capable of Pause Operation for Full Duplex Link 0 Not Capable
9	T4	100Base-T4 Capable	R/W	1 Capable of 100Base-T4 0 Not Capable
8	TX_FDX	100Base-TX Full Duplex Capable	R/W	1 Capable of 100Base-TX Full Duplex 0 Not Capable
7	TX_HDX	100Base-TX Half Duplex Capable	R/W	1 Capable of 100Base-TX Half Duplex 0 Not Capable
6	10_FDX	10Base-T Full Duplex Capable	R/W	1 Capable of 10Base-T Full Duplex 0 Not Capable
5	10_HDX	10Base-T Half Duplex Capable	R/W	1 Capable of 10Base-T Half Duplex 0 Not Capable
4-1			R/W	RESERVED
0	CSMA	CSMA 802.3 Capable	R/W	1 Capable of 802.3 CSMA Operation 0 Not Capable

Note 1: Next Page currently not supported.

4.4.6 Auto-Negotiation Remote End Capability Register

Tag: AUTOREC Size: 16 bits Hard Reset: 0000h
Offset: 05h Access: Read Only Soft Reset: 0000h

BIT	TAG	DESCRIPTION	R/W	USAGE
15	NP	Next Page Enable	R	1 Next Page Exists 0 No Next Page
14	ACK	Acknowledge	R	1 Received Auto-Negotiation Word Recognized 0 Not Recognized
13	RF	Remote Fault	R	1 Auto-Negotiation Remote Fault Detected

		Enable		0 No Remote Fault
12-11			R	RESERVED
10	PAUSE	Pause Operation for Full Duplex Link	R	1 Capable of Pause Operation for Full Duplex Link 0 Not Capable
9	T4	100Base-T4 Capable	R	1 Capable of 100Base-T4 0 Not Capable
8	TX_FDX	100Base-TX Full Duplex Capable	R	1 Capable of 100Base-TX Full Duplex 0 Not Capable
7	TX_HDX	100Base-TX Half Duplex Capable	R	1 Capable of 100Base-TX Half Duplex 0 Not Capable
6	10_FDX	10Base-T Full Duplex Capable	R	1 Capable of 10Base-T Full Duplex 0 Not Capable
5	10_HDX	10Base-T Half Duplex Capable	R	1 Capable of 10Base-T Half Duplex 0 Not Capable
4-1			R	RESERVED
0	CSMA	CSMA 802.3 Capable	R	1 Capable of 802.3 CSMA Operation 0 Not Capable

4.4.7 Configuration 1 Register

Tag: CONFIG1 Size: 16 bits Hard Reset: 0022h

Offset: 10h Access: Read Write Soft Reset: 0022h

BIT	TAG	DESCRIPTION	R/W	USAGE
15	LNK_DIS	Link Disable	R/W	1 Received Link Detect Function Disabled (Force Link Pass) 0 Normal
14	XMT_DIS	TP Transmit Disable	R/W	1 TP Transmitter Disabled 0 Normal
13	XMT_PDN	TP Transmit Powerdown	R/W	1 TP Transmitter Powered Down 0 Normal
12	TXEN_CRS	TXEN to CRS Loopback Disable	R/W	1 TX_EN to CRS Loopback Disabled 0 Enabled
11-10				RESERVED
9	UNSCR_DIS	Unscrambled Idle Reception Disable	R/W	1 Disable Auto-Negotiation with devices that transmit unscrambled, idle on power up and various instances 0 Enables Auto-Negotiation with devices that transmit unscrambled, idle on power up and various instances
8	EQLZR	Receive Equalizer Select	R/W	1 Received Equalizer Disabled, Set to 0 Length 0 Receive Equalizer On (For 100Base-TX Mode Only)
7	CABLE	Cable Type Select	R/W	1 STP (150 Ohm) 0 UTP (100 Ohm)
6	RLVL0	Receive Input Level Adjust	R/W	1 Receive Squelch Levels Reduced By 4.5 dB 0 Normal
5-2	TLVL3	Transmit Output	R/W	See Table 3-7

	TLVL2 TLVL1 TLVL0	Level Adjust		
1-0	TRF1 TRF0	Transmitter Rise/Fall Time Adjust	R/W	11 -0.25 ns 10 +0.0 ns 01 +0.25 ns 00 +0.5 ns

4.4.8 Configuration 2 Register

Tag: CONFIG2 Size: 16 bits Hard Reset: FF00h
Offset: 11h Access: Read Write Soft Reset: FF00h

BIT	TAG	DESCRIPTION	R/W	USAGE
15-14	PLED3#_1 PLED3#_0	Programmable LED Output Select, Pin PLED3#	R/W	11 Normal (PLED3# is Determined By Bits 17.7-17.6 And Table 3-11. Default is LINK100) 10 LED Blink (PLED3# is toggling 100 mS Low, 100 ms High) 01 LED On (PLED3# is Low) 00 LED Off (PLED3# is High)
13-12	PLED2#_1 PLED2#_0	Programmable LED Output Select, Pin PLED2#	R/W	11 Normal (PLED2# is Determined By Bits 17.7-17.6 And Table 3-11. Default is Activity) 10 LED Blink (PLED2# is toggling 100 mS Low, 100 ms High) 01 LED On (PLED2# is Low) 00 LED Off (PLED2# is High)
11-10	PLED1#_1 PLED1#_0	Programmable LED Output Select, Pin PLED1#	R/W	11 Normal (PLED1# is Determined By Bits 17.7-17.6 And Table 3-11. Default is Full Duplex) 10 LED Blink (PLED1# is toggling 100 mS Low, 100 ms High) 01 LED On (PLED1# is Low) 00 LED Off (PLED1# is High)
9-8	PLED0#_1 PLED0#_0	Programmable LED Output Select, Pin PLED0#	R/W	11 Normal (PLED0# is Determined By Bits 17.7-17.6 And Table 3-11. Default is LINK10) 10 LED Blink (PLED0# is toggling 100 mS Low, 100 ms High) 01 LED On (PLED0# is Low) 00 LED Off (PLED0# is High)
7-6	LED_DEF1 LED_DEF0	LED Normal Function Select	R/W	See Table 3-11
5	APOL_DIS	Auto Polarity Disable	R/W	1 Auto Polarity Correction Function Disabled 0 Normal
4	JAB_DIS	Jabber Disable Select	R/W	1 Jabber Disabled 0 Enabled
3-0			R/W	RESERVED

4.4.9 Status Output Register

Tag: STSOUT Size: 16 bits Hard Reset: 0080h

Offset: 12h Access: Read Only Soft Reset: 0080h

BIT	TAG	DESCRIPTION	R/W	USAGE
15	INT	Interrupt Detect	R	1 Interrupt Bit(s) Have Changed Since Last Read Operation. 0 No Change
14	LNK_FAIL	Link Fail Detect	R/LT	1 Link Not Detected 0 Normal
13	LOSS_SYNC	Descrambler Loss of Synchronization Detect	R/LT	1 Descrambler Has Lost Synchronization 0 Normal
12	CWRD	Codeword Error	R/LT	1 Invalid 4B5B Code Detected On Receive Data 0 Normal
11	SSD	Start Of Stream Error	R/LT	1 No Start Of Stream Delimiter Detected on Received Data 0 Normal
10	ESD	End Of Stream Error	R/LT	1 No End Of Stream Delimiter Detected On Receive Data 0 Normal
9	RPOL	Reverse Polarity Detect	R/LT	1 Reserve Polarity Detected 0 Normal
8	JAB	Jabber Detect	R/LT	1 Jabber Detected 0 Normal
7	SPD_DET	100/10 Speed Detect	R/LT	1 Device in 100 Mbps Mode (100Base-TX) 0 Device in 10 Mbps Mode (10Base-T)
6	DPLX_DET	Duplex Detect	R/LT	1 Device In Full Duplex 0 Device In Half Duplex
5-4	ANEG_STS1 ANEG_STS0	Auto-Negotiation Status	R	11 Auto-Negotiation Detected & Started 10 Auto-Negotiation Detected & Stuck 01 Auto-Negotiation Detected & Done 00 Auto-Negotiation Not Detected
3-0			R	RESERVED

4.4.10 Mask Register

Tag: MASK Size: 16 bits Hard Reset: FFC0h

Offset: 13h Access: Read Write Soft Reset: FFC0h

BIT	TAG	DESCRIPTION	R/W	USAGE
15	MASK_INT	Interrupt Mask –Interrupt Detect	R/W	1 Mask Interrupt For INT in Register 18 0 No Mask
14	MASK_LNK_FAIL	Interrupt Mask – Link Fail Detect	R/W	1 Mask Interrupt For LNK_FAIL in Register 18 0 No Mask
13	MASK_LOSS_SYNC	Interrupt Mask –Descrambler Loss of Synchronization Detect	R/W	1 Mask Interrupt For LOSS_SYNC in Register 18 0 No Mask

12	MASK_CWRD	Interrupt Mask –Code Word Error	R/W	1 Mask Interrupt For CWRD in Register 18 0 No Mask
11	MASK_SSD	Interrupt Mask -Start Of Stream Error	R/W	1 Mask Interrupt For SSD in Register 18 0 No Mask
10	MASK_ESD	Interrupt Mask -End Of Stream Error	R/W	1 Mask Interrupt For ESD in Register 18 0 No Mask
9	MASK_RPOL	Interrupt Mask –Reverse Polarity Detect	R/W	1 Mask Interrupt For RPOL in Register 18 0 No Mask
8	MASK_JAB	Interrupt Mask –Jabber Detect	R/W	1 Mask Interrupt For JAB in Register 18 0 No Mask
7	MASK_SPD_DET	Interrupt Mask -100/10 Speed Detect	R/W	1 Mask Interrupt For SPD_DET in Register 18 0 No Mask
6	MASK_DPLX_DET	Interrupt Mask –Duplex Detect	R/W	1 Mask Interrupt For DPLX_DET in Register 18 0 No Mask
5-3			R/W	RESERVED.
2-0	LNK_TMR2 LNK_TMR1 LNK_TMR0	Link Fail Timer Select	R/W	111 RESERVED 110 Bit 18.14 Set to 1 if Link Fail for >32 Sec 101 Bit 18.14 Set to 1 if Link Fail for >16 Sec 100 Bit 18.14 Set to 1 if Link Fail for >8 Sec 011 Bit 18.14 Set to 1 if Link Fail for >4 Sec 010 Bit 18.14 Set to 1 if Link Fail for >2 Sec 001 Bit 18.14 Set to 1 if Link Fail for >1 Sec 000 Bit 18.14 Set to 1 if Link Fail for >0 Sec

4.4.11 Reservered Register

Tag: RESERVED Size: 16 bits Hard Reset: 0000h
Offset: 14h Access: Read Write Soft Reset: 0000h

BIT	TAG	DESCRIPTION	R/W	USAGE
15-0			R/W	Reserved for Factory Use. Must be 0 for Normal Operation

5 ELECTRICAL CHARACTERISTICS

5.1 Absolute Maximum Ratings

Supply Voltage (OVDD)	-0.3 V to +3.6 V
Supply Voltage (OVDD_AUX)	-0.3 V to +3.6 V
Supply Voltage (5VDD)	-0.5 V to +7.0 V
Supply Voltage (5VDD_AUX)	-0.5 V to +7.0 V
Supply Voltage (AVDD_AUX)	-0.3 V to +3.6 V
DC Input Voltage (VIN)	-0.5 V to 5VDD+0.5V
DC Output Voltage (VOUT)	-0.3 V to VDD+0.3V
Storage Temperature Range (T_{STG})	-40°C to 125°C
Ambient Temperature (TA)	0 to 70°C
Lead Temp. (TL) (Soldering, 10 sec)	250°C
ESD Rating ($R_{ZAP = 1.5k, CZAP = 120 pF}$)	2.0 KV
Input Latchup Current	+/- 25mA
Package Power Dissipation	3.0Watt@25^{0}C

5.2 Recommended Operating Conditions

Supply voltage (OVDD)		3.3 Volts ± 5%
Supply voltage (OVDD_AUX)		3.3 Volts ± 5%
Supply voltage (5VDD)		5 Volts ± 5%
Supply voltage (5VDD_AUX)		5 Volts ± 5%
Supply Current (I_{DD})	D0 State	
Supply Current (I_{DD_AUX})	D0 State	
Supply Current (I_{DD})	D1,D2,D3hot State	
Supply Current (I_{DD_AUX})	D1,D2,D3hot State	
Supply Current (I_{DD_AUX})	D3cold and PME Enable State	
Supply Current (I_{DD_AUX})	D3cold and PME Disable State	
Supply Current (I_{DD})	Low Power Mode	
Supply Current (I_{DD_AUX})	Low Power Mode	

5.3 DC Electrical characteristics

5.3.1 PCI Interface DC Specification

Unless otherwise noted, all test conditions ate as follows:

1. T_A = 0 to +70^{0}C
2. 5VDD = 5V +/- 5%
3. OVDD = 3.3V +/- 5%

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNITS	NOTE
V_{ih}	Input High Voltage		2.0	5VDD+0.5	V	
V_{il}	Input Low Voltage		-0.5	0.8	V	
I_{ih}	Input High Leakage Current	V_{in} = 2.7		10	µA	1
I_{il}	Input High Leakage Current	V_{in} = 0.5		-10	µA	1
V_{oh}	Output High Voltage	I_{out} = -2mA	2.4		V	
V_{ol}	Output Low Voltage	I_{out} = 3mA, 6mA		0.55	V	2
C_{in}	Input Pin Capacitance			10	pF	
C_{pclk}	PCLK Pin Capacitance		5	12	pF	
C_{IDSEL}	IDSEL Pin Capacitance			8	pF	
L_{pin}	Pin Inductance			20	nH	

NOTES:

1. Input leakage currents include hi-Z output leakage for all bi-directional buffers with tri-state outputs.
2. Signals without pull-up resistors must have 3mA low output current. Signals requiring pull-up must have 6mA; the latter include FRAME#, TRDY#, IRDY#, DEVSEL#, STOP#, SERR#, and PERR#.

5.3.2 Boot ROM/EEPROM Interface DC Specification

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNITS
V_{ih}	Input High Voltage		2.0	5VDD+0.5	V
V_{il}	Input Low Voltage		-0.5	0.8	V
I_{ih}	Input High Leakage Current	0<V_{in} < 5VDD		1	µA
I_{il}	Input High Leakage Current	0<V_{in} < 5VDD		-1	µA
V_{oh}	Output High Voltage		2.4		V
V_{ol}	Output Low Voltage			0.4	V
C_{in}	Input Pin Capacitance			10	pF

5.3.3 Analog Signals DC Specification

Unless otherwise noted, all test conditions ate as follows:

1. T_A = 0 to +70^{0}C
2. V_{CC} = 3.3V +/- 10%
3. 25Mhz +/- 0.01%
4. REXT = 10K +/- 1%, no load

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
V_{IL}	Input Low Voltage	OSCIN			1.5	Volt
V_{IH}	Input High Voltage	OSCIN	3.5			Volt
I_{IL}	Input Low Current	V_{IN}=GND. OSCIN			-150	µA
I_{IH}	Input High Current	V_{IN}=VCC. OSCIN			150	µA
V_{OL}	Output Low Voltage	I_{OL}= -4 mA TPO±			0.4	Volt
		I_{OL}= -20 mA, PLED[3:0]#			1	Volt
V_{OH}	Output High Voltage	I_{OH}= 4 mA TPO±	V_{CC}-1.0			Volt
		I_{OH}= 4 µA PLED[3:2]#	V_{CC}-1.0			Volt
		I_{OH}= 6 µA PLED[1:0]#	2.4			Volt
C_{IN}	Input Capacitance			5		pF
I_{CC}	V_{CC} Supply Current	Transmitting, 100Mbps			200	mA
		Transmitting, 10Mbps			250	mA
		Powerdown Mode			0.1	mA

5.4 Twist Pair Characteristics, Transmit

Unless otherwise noted, all test conditions ate as follows:

1. T_A = 0 to +70 ^{0}C
2. V_{CC} = 3.3V +/- 10%
3. 25Mhz +/- 0.01%
4. REXT = 10K +/- 1%, no load
5. TPO± loading shown in Figure 6-1 or equivalent.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
T_{OV}	TP Differential Output Voltage	100 Mbps, UTP Mode, 100 Ohm Load	0.950	1.000	1.050	V pk

		100 Mbps, SUTP Mode, 150 Ohm Load	1.165	1.225	1.285	V pk
		10 Mbps, UTP Mode, 100 Ohm Load	2.2	2.5	2.8	V pk
		10 Mbps, STP Mode, 150 Ohm Load	2.694	3.062	3.429	V pk
T_{OVS}	TP Differential Output Voltage Symmetry	100 Mbps, Ratio of Positive And Negative Amplitude Peak on TPO±	98		102	%
T_{ORF}	TP Differential Output Rise And Fall Time	100 Mbps	3.0		5.0	nS
T_{ORFS}	TP Differential Output Rise And Fall Time Symmetry	100 Mbps, Difference Between Rise And Fall Times on TPO± TRFADJ[1:0] = 10			+/- 0.5	nS
T_{ODC}	TP Differential Output Duty Cycle Distortion	100 Mbps, Output Data=0101_ NRZ Pattern Unscrambled, Measure At 50% Points			+/- 0.25	nS
T_{OJ}	TP Differential Output Jitter	100 Mbps, Output Data = Scrambled /H/			+/- 1.4	nS
T_{OO}	TP Differential Output Overshoot	100 Mbps			5.0	%
T_{OVT}	TP Differential Output Voltage Template	10 Mbps	See Figure 3-18			
T_{SOI}	TP Differential Output SOI Voltage Template	10 Mbps	See Figure 3-19			
T_{LPT}	TP Differential Output Link Pulse Voltage Template	10 Mbps, NLP and FLP	See Figure 3-20			
T_{OIV}	TP Differential Output Idle Voltage	10 Mbps, Measured on Secondary Side of Xfmr in Figure 7.3-1.			+/- 50	MV
T_{HD}	TP Harmonic Distortion	10Mbps, All 1's output			-27	DB
T_{OIA}	TP Output Current	100 Mbps, UTP with TLVL[3:0]=1000	38	40	42	MA pk
		100 Mbps, STP with TLVL[3:0]=1000	31.06	32.66	34.26	MA pk
		10 Mbps, UTP with TLVL[3:0]=1000	88	100	112	MA pk
		10 Mbps, STP with TLVL[3:0]=1000	71.86	81.64	91.44	MA pk
T_{OIR}	TP Output Current Adjustment Range	V_{CC} =3.3V, Adjustable with REXT, relative to T_{OIA} with REXT=10 K	0.80		1.12	
		V_{CC} =3.3V, Adjustable with TLVL[3:0], See Section 5.4, Relative to Value at TLVL[3:0] = 1000.	0.86		1.16	

T_{ORA}	TP Output Current TLVL Step Accuracy	Relative to Idea Values in Table 3.1-2. Table 3.1-2 Values Relative to Output with TLVL[3:0] = 1000.			+/- 50	%
T_{CMA}	TP Common Mode AC Output Voltage			10	20	MV_{PK}
T_{OR}	TP Output Resistance			10k		Ohm
T_{OC}	TP Output Capacitance			15		pF

5.5 Twist Pair Characteristics, Receive

Unless otherwise noted, all test conditions ate as follows:

1. T_A = 0 to +70 C
2. V_{CC} = 3.3V +/- 10%
3. 25Mhz +/- 0.01%
4. REXT = 10K +/- 1%, no load
5. 125/10Mhz Sequence Wave on TP inputs in 100/10 Mbps.

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
RST	TP Input Squelch Threshold	100 Mbps, RLVL=0	166		500	mV pk
		10 Mbps, RLVL=0	310		540	mV pk
		100 Mbps, RLVL=1	100		300	mV pk
		10 Mbps, RLVL=1	186		324	mV pk
RUT	TP Input Unsquelch Threshold	100 Mbps, RLVL=0	100		300	mV pk
		10 Mbps, RLVL=0	186		324	mV pk
		100 Mbps, RLVL=1	20		90	mV pk
		10 Mbps, RLVL=1	112		194	mV pk
RZT	TP Input Zero Cross Switching Threshold				+/- 20	mV pk
ROCV	TP Input Open Circuit Voltage	Voltage on Either TPI+ or TPI- with Respect to GND	V_{CC}-1.0	Vcc	V_{CC}+1.0	Volt
RCMR	TP Input Common Mode Voltage Range	Voltage on TPI± with Respect to GND	V_{CC}-1.0		V_{CC}+1.0	Volt
RDR	TP Input Differential Voltage Range		GND		V_{CC}	Volt
RCRR	TP Input Common Mode Rejection Ratio	0 – 10 Mhz			-20	DB
RIR	TP Input Resistance		5K			ohm
RIC	TP Input Capacitance			10		pF

5.6 AC Specifications

5.6.1 PCI Interface AC Specification

Unless otherwise noted, all test conditions ate as follows:

1. T_A = 0 to +70^{0}C
2. 5VDD = 5V +/- 5%
3. OVDD = 3.3V +/- 5%

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNITS	NOTES
$I_{oh\ (AC)}$	Switching	$0<V_{out}\_1.4$	-44		mA	1
	Current High	$1.4<V_{out}<2.4$	$-44+(V_{out}-1.4)/0.024$		mA	1
		$3.1<V_{out}<V_{dd}$		Eqt'n A		1,2
	(Test Point)	V_{out} = 3.1		-142	mA	2
$I_{oh\ (AC)}$	Switching	$V_{out}\_2.2$	95		mA	1
	Current Low	$2.2>V_{out}>0.55$	$V_{out}/0.023$		mA	1
		$0.71>V_{out}>0$		Eqt'n B		1,2
	(Test Point)	V_{out} = 0.71		206	mA	2
I_{cl}	Low Clamp Current	$-5<V_{in}\_-1$	$-25+(V_{in}+1)/0.015$		mA	
$Slew_r$	Output Rise Slew Rate	0.4V to 2.4V load	1	5	V/ns	3
$Slew_f$	Output Fall Slew Rate	2.4V to 0.4V load	1	5	V/ns	3

NOTES:

1. This specification does not apply to **PCLK** and **RST#** which are system outputs. "Switching Current High" specifications are not relevant to **SERR#**, **INTA#** and **PME#** which are open drain outputs.
2. Maximum current requirements must be met as drivers pull beyond the first step voltage. Equation A and B define the maximums are provided below. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.

   Equation A: $I_{oh} = 11.9*(V_{out}-5.25)*(V_{out}+2.45)$ for OVDD> V_{out} >3.1V

   Equation B: $I_{oh} = 78.5*(4.4-V_{out})$ for 0 V< V_{out} < 0.71V
3. This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition edge.

5.7 Timing Specification

5.7.1 Clock Specifications

5.7.1.1 PCI Clock

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES

t_{cyc}	PCLK Cycle TIme	30	∞	ns	1
t_{high}	PCLK High Time	11		ns	
t_{low}	PCLK Low Time	11		ns	
-	PCLK Slew Rate	1	4	V/ns	2

NOTES:

1. The SiS900 MAC works with PCLK frequency from DC to 33 MHz.
2. Rise and fall times are specified in terms of the edge rate measured in V/ns. This slew rate must be met across the minimum peak-to-peak portion of the above clock waveform.

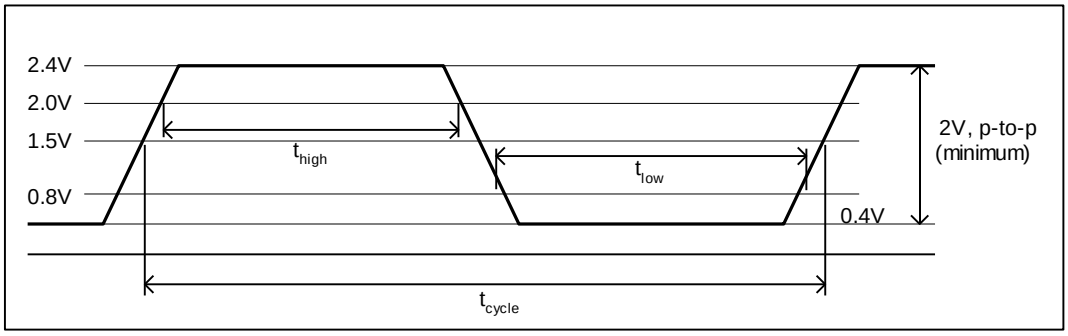


Figure 5-1 PCI Clock

5.7.1.2 25 Mhz Clock Timing Characteristics

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
T_1	OSCIN Cycle Time	Clock Applied to OSCIN	39.996	40	40.004	nS
T_2	OSCIN High Time	Clock Applied to OSCIN	16			nS
T_3	OSCIN Low Time	Clock Applied to OSCIN	16			nS

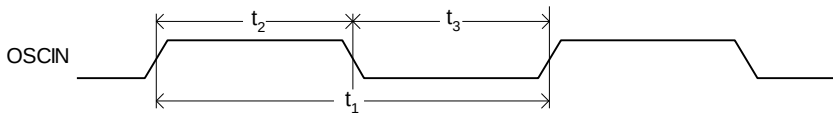


Figure 5-2 25Mhz Clock Timing

5.7.2 PCI Timings

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
t_{val}	PCLK to Signal Valid Delay - bused signals	2	11	ns	1,2
t_{val}(ptp)	PCLK to Signal Valid Delay - point to point	2	12	ns	1,2
t_{on}	Float to Active Delay	2		ns	
t_{off}	Active to Float Delay		28	ns	
t_{su}	Input Set up Time to PCLK - bused signals	7		ns	2
t_{su}(ptp)	Input Set up Time to PCLK - point to point	10,12		ns	2
t_h	Input Hold Time from PCLK	0		ns	

NOTES:

1. Minimum times are evaluated with 0pF equivalent load; maximum times are evaluated with 50pF equivalent load. Actual test capacitance may vary, but results should be correlated to these specifications.
2. **REQ#** and **GNT#** are point-to-point signals, and have different output valid delay and input setup times than do bused signals. **GNT#** has a setup of 10; **REQ#** has a setup of 12. All other signals are bused.
3. **RST#** is asserted and de-asserted asynchronously with respect to **PCLK**.
4. All output drivers must be asynchronously floated when **RST#** is active.

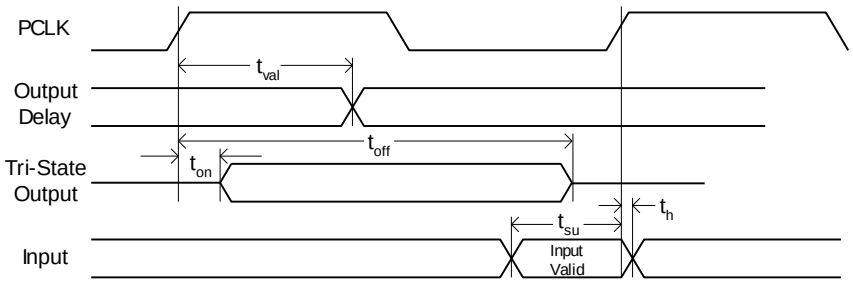


Figure 5-3 PCI Timings

5.7.3 Boot ROM Timings

■ Read Operation Timings

SYMBOL	PARAMETER	MIN	MAX	UNITS
tRC	Read Cycle Time	150		ns
tCE	PCE# Access Time		150	ns
tACC	Address Access Time		150	ns
tOE	POE# Access Time		55	ns
tCE-DF	Chip Disable to Output in High Z		55	ns
tOE-DF	Output Disable to Output in High Z		35	ns
tOH	Output Hold from Address,PCE# or POE# Change	0		ns
tREC	Write Recovery Time before Read	6		µs

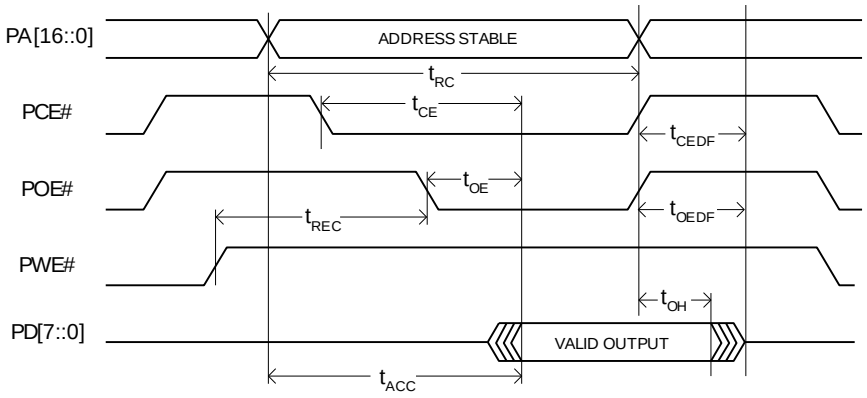


Figure 5-4 Boot ROM Read Operation Timings

■ Write Operation Timings

SYMBOL	PARAMETER	MIN	MAX	UNITS
tWC	Write Cycle Time	150		ns
tAS	Address Setup Time	0		ns
tAH	Address Hold Time	40		ns
tDS	Data Setup Time	40		ns
tDH	Data Hold Time	10		ns
tCES	Chip Enable Setup Time before Write	15		ns
tCEH	Chip Enable Hold Time	0		ns
tWP	Write Pulse Width	60		ns

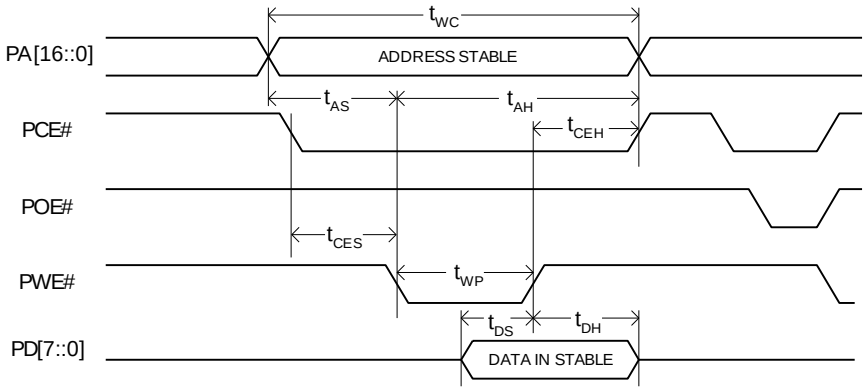


Figure 5-5 Flash Boot ROM Write Operation Timings

5.7.4 EEPROM Timings

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
tEESK	EESK Clock Frequency	0	0.5	MHz	
tEECSS	EECS Setup Time to EESK	50		ns	
tEECSH	EECS Hold Time from EESK	0		ns	
tEEDOH	EEDO Hold Time from EESK	70		ns	
tEEDOP	EEDO Output Delay to “1” or “0”		1000	ns	
tEEDIS	EEDI Setup Time to EESK	200		ns	
tEEDIH	EEDI Hold Time from EESK	20		ns	

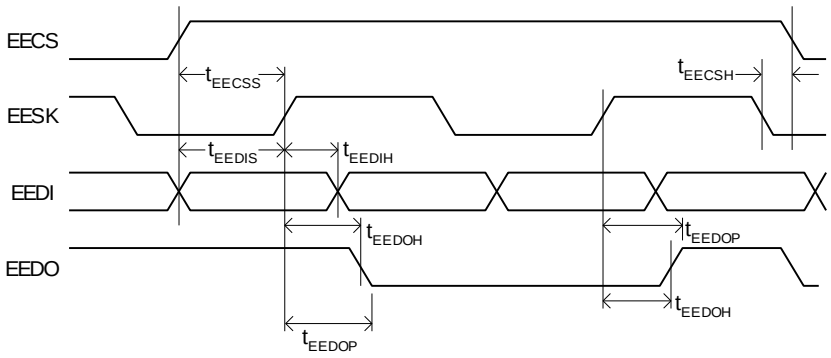


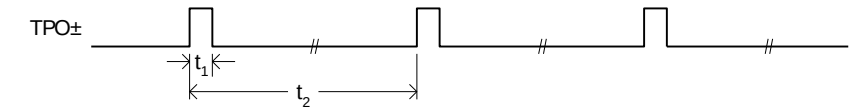
Figure 5-6 EEPROM Timings

5.7.5 Link Pulse Timing Characteristic

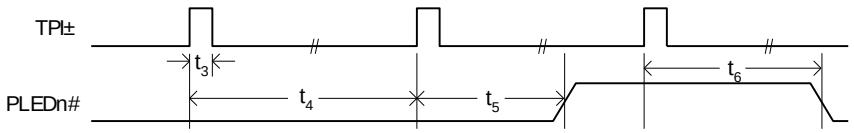
Refer to Figure 5-7 ~ 5-8 for Timing Diagram

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
t_1	NLP Transmit Link Pulse Width		See Figure 3-20			ns
t_2	NLP Transmit Link Pulse Period		8		24	ms
t_3	NLP Receive Link Pulse Width Required For Detection		50			ns
t_4	NLP Receive Link Pulse Minimum Period Required For Detection	link_test_min	6		7	ms
t_5	NLP Receive Link Pulse Maximum Period Required For Detection	link_test_max	50		150	ms
t_6	NLP Receive Link Pulse Required To Exit Link Fail State	lc_max	3	3	3	Link Pulses
t_7	FLP Transmit Link Pulse Width		100		150	ns
t_8	FLP Transmit Clock Pulse To Data Pulse Period	interval_timer	55.5	62.5	69.5	µs
t_9	FLP Transmit Clock Pulse To Clock Pulse Period		111	125	139	µs
t_{10}	FLP Transmit Link Pulse Burst Period	transmit_link_burst_timer	8		22	ms
t_{11}	FLP Receive Link Pulse Width Required For Detection		50			ns
t_{12}	FLP Receive Link Pulse Minimum Period Required For Clock Pulse Detection	flp_test_min_timer	5		25	µs
t_{13}	FLP Receive Link Pulse Maximum Period Required For Clock Pulse Detection	flp_test_max_timer	165		185	µs
t_{14}	FLP Receive Link Pulse Minimum Period Required For Data Pulse Detection	data_detect_min_timer	15		47	µs
t_{15}	FLP Receive Link Pulse Maximum Period Required For Data Pulse Detection	data_detect_max_timer	78		100	µS
t_{16}	FLP Receive Link Pulse Required To Detect Valid FLP Burst		17		17	Link Pulse
t_{17}	FLP Receive Link Pulse Burst Minimum Period Required For Detection	nlp_test_min_timer	5		7	ms

t_{18}	FLP Receive Link Pulse Burst Maximum Period Required For Detection	nlp_test_max_timer	50		150	ms
t_{19}	FLP Receive Link Pulse Burst Required To Detect AutoNegotiation Capability		3	3	3	Link Pulse
t_{20}	FLP Receive Acknowledge Fail Period		1200		1500	ms
t_{21}	FLP Transmit Renegotiate Link Fail Period	break_link_timer	1200		1500	ms
t_{22}	NLP Receive Link Pulse Maximum Period Required For Detection After FLP Negotiation Has Complete	link_fail_inhibit_timer	750		1000	ms

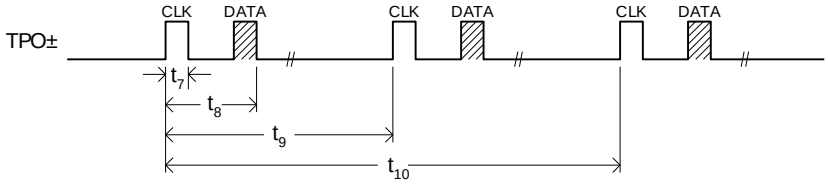


a.) Transmit NLP

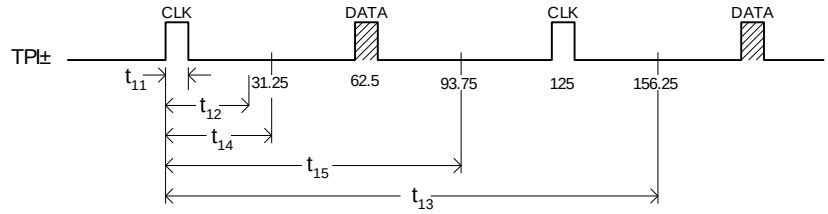


b.) Receive NLP

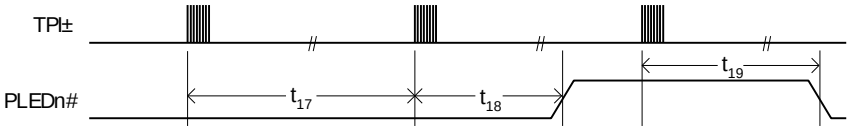
Figure 5-7 NLP Link Pulse Timing



a.) Transmit FLP and Transmit FLP Burst



b.) Receive FLP



c.) Receive FLP Burst

Figure 5-8 FLP Link Pulse Timing

5.7.6 LED Driver Timing Characteristics

Refer to Figure 5.5-9 for Timing Diagram

SYM	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
t_1	PLED[3:0]# On Time	PLED[3:0]# Programmed To Blink	80		105	ms
t_2	PLED[3:0]# Off Time	PLED[3:0]# Programmed To Blink	80		105	ms

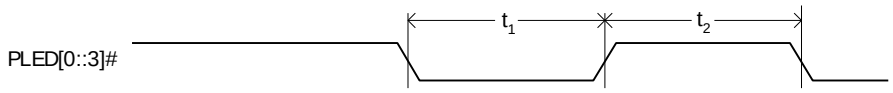
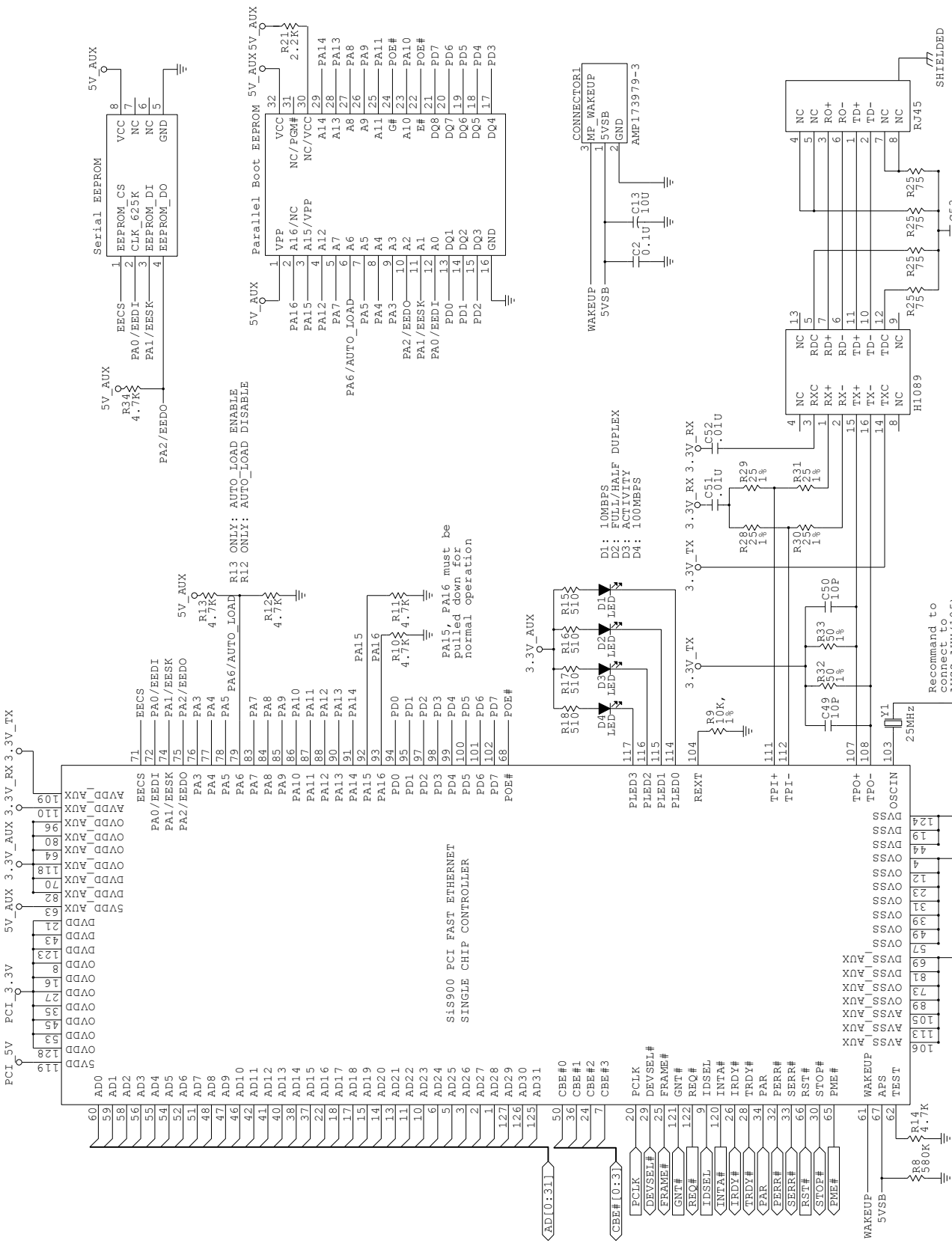


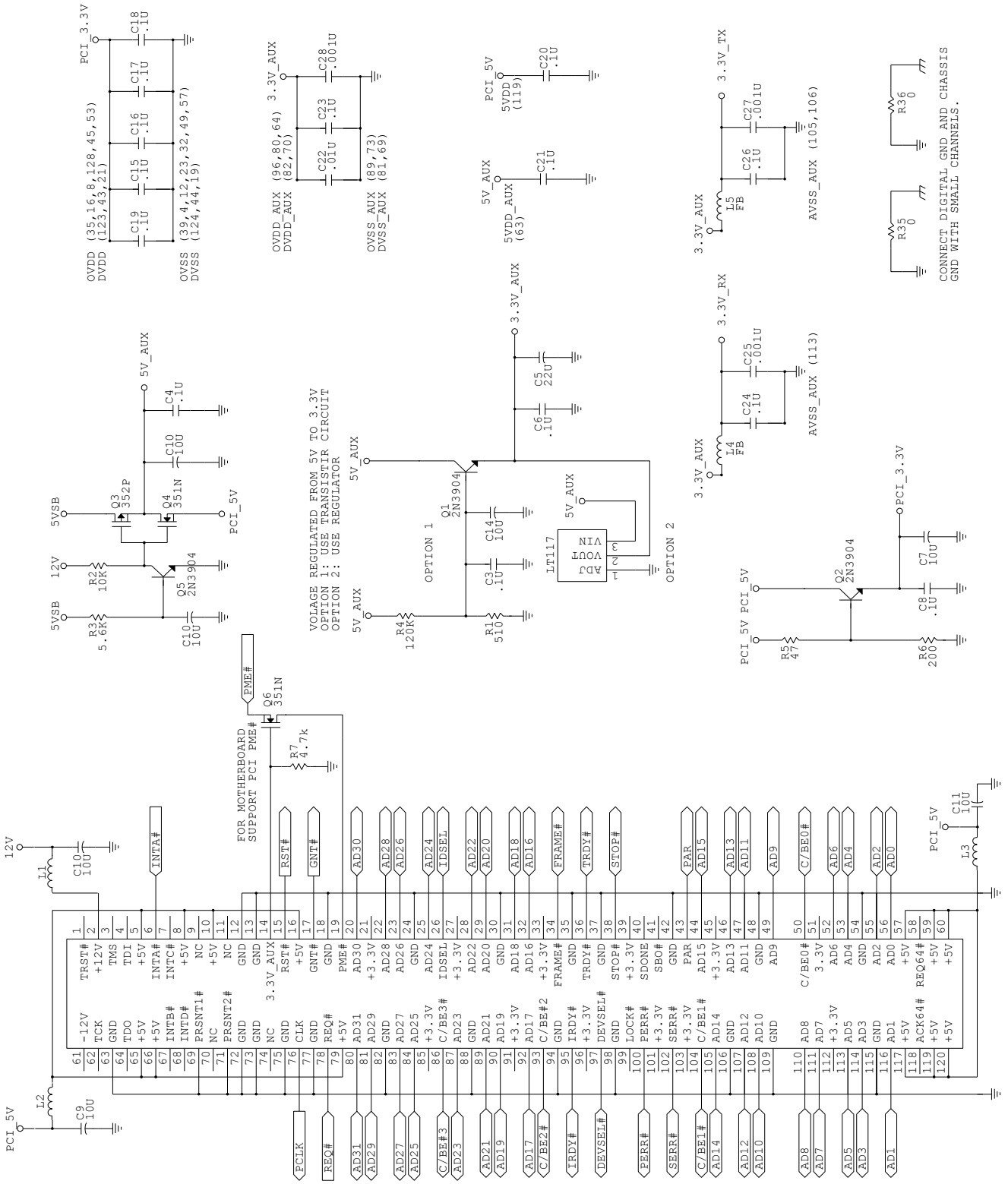
Figure 5-9 LED Driver Timing

6. APPLICATION INFORMATION

6.1 Examples Schematics

A typical example schematic of the SiS900 used in an adapter card application is shown in Figure 6-1.


SiS900 PCI FAST ETHERNET
SINGLE CHIP CONTROLLER
Serial EEPROM
Parallel Boot EEPROM
CONNECTOR1
MP_WAKEUP
AMP173979-3
H1089
RJ45
SHIELDED
Recommand to connect to AVSS_AUX(105)
D1: 10MBPS
D2: FULL/HALF DUPLEX
D3: ACTIVITY
D4: 100MBPS
PA15, PA16 must be pulled down for normal operation
R13 ONLY: AUTO_LOAD ENABLE
R12 ONLY: AUTO_LOAD DISABLE
PCI 5V
PCI 3.3V
5V_AUX
3.3V_AUX
3.3V_RX
3.3V_TX
AD[0:31]
CBE#[0:3]
PCLK
DEVSEL#
FRAME#
GNT#
REQ#
IDSEL
INTA#
IRDY#
TRDY#
PAR
PERR#
SERR#
RST#
STOP#
PME#
WAKEUP
APS
TEST
25MHz


OVDD (35,16,8,128,45,53)
DVDD (123,43,21)
OVSS (39,4,12,23,32,49,57)
DVSS (124,44,19)
OVDD_AUX (96,80,64)
DVDD_AUX (82,70)
OVSS_AUX (89,73)
DVSS_AUX (81,69)
5VDD (119)
5VDD_AUX (63)
AVSS_AUX (105,106)
AVSS_AUX (113)
CONNECT DIGITAL GND AND CHASSIS GND WITH SMALL CHANNELS.
VOLAGE REGULATED FROM 5V TO 3.3V
OPTION 1: USE TRANSISTIR CIRCUIT
OPTION 2: USE REGULATOR
OPTION 1
OPTION 2
LT1117
FOR MOTHERBOARD SUPPORT PCI PME#
PCI_3.3V
PCI_5V
5V_AUX
3.3V_AUX
3.3V_RX
3.3V_TX
5VSB
12V

6.2 Twist Pair Transmit Interface

The interface between the TP outputs on TPO± and the twisted pair cable is typically transformer coupled and terminated with the two resistors as shown in Figures 6-1.

The transformer for the transmitter is recommended to have a winding ration of 1:1 with a center tap on the primary winding tied to VDD, as shown in Figures 6-1. The specifications for such a transformer are shown in Table 6-1. Sources for the transformer are listed in Table 6-2.

The transmit output needs to be terminated with two external termination resistors in order to meet the output impedance and return loss requirements of IEEE 802.3. It is recommended that these two external resistors be connected from VDD to each of the TPO± outputs, and their value should be chosen to provide the correct termination impedance when looking back through the transformer from the twisted pair cable, as shown in Figures 6-1. The value of these two external termination resistors depends on the type of cable driven by the device. Refer to the Cable Selection section for more details on choosing the value of these resistors. This two external termination resistors should be placed symmetrically and close to SiS900 for reducing noise pick up into the transmit trace.

To minimize common mode output noise and to aid in meeting radiated emissions requirements, it may be necessary to add a common mode choke on the transmit outputs as well as add common mode bundle termination. The qualified transformers mentioned in Table 6-2 all contain common mode chokes along with the transformers on both the transmit and receive sides, as shown in Figures 6-1. Common mode bundle termination may be needed and can be achieved by tying the unused pairs in the RJ45 to chassis ground through 75 ohm resistors and a 0.01 uF capacitor, as shown in Figures 6-1.

To minimize noise pickup into the transmit path in a system or on a PCB, the loading on TPO± should be minimized and both outputs should always be loaded equally.

6.3 Twist Pair Receive Interface

Receive data is typically transformer coupled into the receive inputs on TPI± and terminated with external resistors as shown in Figures 6-1.

The transformer for the receiver is recommended to have a winding ration of 1:1, as shown in Figures 6-1. The specifications for such a transformer are shown in Table 6-1. Sources for the transformer are listed in Table 6-2.

The receive input needs to be terminated with the correct termination impedance meet the input impedance and return loss requirements of IEEE802.3. In addition, the receive TP inputs need to be attenuated. It is recommended that both the termination and attenuation be accomplished by placing four external resistors in series across the TPI± inputs as shown in Figures 6-1. The resistors should be 25% / 25% / 25% / 25% of the total series resistance, and the total series resistance should be equal to the characteristic impedance of the cable (100 Ohms for UTP, 150 Ohms for STP). It is also recommended that a 0.01μF capacitor be placed between the center of the series resistor string and VDD in order to provide an AC ground for attenuating common mode signal at the input. This capacitor is also shown in Figures 6-1. It is recommended that these series resistor string and grounding capacitor be placed near the transformer.

To minimize common mode input noise and to aid in meeting susceptibility requirements, it may be necessary to add a common mode choke on the receive input as well as add common mode bundle termination. The qualified transformers mentioned in Table 6-2 all contain common mode chokes along with the transformers on both the transmit and receive sides, as shown in Figures 6-1. Common mode bundle termination may be needed and can be achieved by tying the receive secondary center tap and the unused pairs in the RJ45 to chassis ground through 75 ohm resistors and a 0.01 μF capacitor, as shown in Figures 6-1.

In order to minimize noise pickup into the receive path in a system or on a PCB, loading on TPI± should be minimized and both inputs should be loaded equally.

Table 6-1 TP Transformer Specification

PARAMETER	SPECIFICATION	
	Transmit	Receive
Turns Ratio	1:1 CT	1:1
Inductance, (μH Min)	350	350
Leakage Inductance, (μH)	0.05-0.15	0.2
Capacitance (pF Max)	15	15
DC Resistance (Ohms Max)	0.4	0.4

Table 6 -2 TP Transformer Sources

Vendor	Part Number
Nano Pulse	NPI 7049-37, NPI 7050-37
Bel	S558-5999-J9
Pulse Engineering	H1089, H1102
Halo	TG22-3506ND, TG110-S050N2
YCL	20PMT04A, PH163112

6.4 Twist Pair Transmit Output Current Set

The TPO± output current level is set by an external resistor tied between REXT and ground. This output current is determined by the following equation where R is the value of REXT:

$I_{out} = (10K/R) * I_{ref}$
Where I_{ref} = 40 mA (100 Mbps, UTP)
= 32.6 mA (100 Mbps, STP)
= 100 mA (10 Mbps, UTP)
= 81.6 mA (10 Mbps, STP)

REXT should be typically set to 10K ohms and REXT should be a 1% resistor in order to meet IEEE 802.3 specified levels. Once REXT is set for the 100 Mbps and UTP modes as shown by the equation above, I_{ref} is then automatically changed inside the device when the alternate 10 Mbps mode and UTP/STP modes are selected.

Keep this external resistor close to the REXT and ground pins as possible in order to reduce noise pickup into the transmitter.

Since the TP output is a current source, capacitive and inductive loading can reduce the output voltage level from the ideal. Thus, in actual application, it might be necessary to adjust the value of the output current to compensate for external loading. One way to adjust the TP output level is to change the value of the external resistor tied to REXT. A better way to adjust the TP output level is to use the transmit level adjust register bits accessed through the MI serial port. These four bits can adjust the output level

by -14% to +16% in 2% steps as described in Table 3-7. For example, if the output loading is 30 pF, the value of the output level needs to be adjusted by approximately +10% to meet the IEEE levels.

6.5 Cable Selection

The SiS900 can drive two different cable types (1) 100 ohm unshielded twisted pair, Category 5, or (2) 150 ohm shielded twisted pair.

The SiS900 must be properly configured for the type of cable in order to meet the return loss specifications in IEEE 802.3. This configuration requires setting a bit in the serial port and setting the value of some external resistors, as described in Table 6-3. The Cable Type Select bit in Table 6-3 is a bit in the MI serial port Configuration 1 register that sets the output current level for the cable type. R_{TERM} in Table 6-3 is the value of the termination resistors needed to meet the level and return loss requirements. The value for R_{TERM} on the TPO± outputs is for the two termination resistors connected between VDD to TPO±; the value for R_{TERM} on the TPI± inputs is for the sum of the four series resistors across TPI± as shown in Figures 6-1. These resistors should be 1% tolerance. Also note that some output level adjustment may be necessary due to parasitic as described in the TP Output Current section.

Table 6-3 Cable Configuration

CABLE TYPE	CABLE TYPE SELECT BIT (16.7)	R_{TERM} (OHMS)	
		TPO±	TPI±
100 Ohm UTP	UTP	50	100
150 Ohm STP	STP	75	150

6.6 Transmitter Droop

The IEEE 802.3 specification has a transmit output droop requirement for 100Base-TX. Since the SiS900 TP output is a current source, it has no perceptible droop by itself. However, the open circuit inductance of the transformer added to the device transmitter output as shown in Figures 7.3-1 will cause droop to appear at the transmit interface to the TP wire. If the transformer connected to the SiS900 outputs meets the requirements in Table 6-2, the transmit interface to the TP cable will meet the IEEE 802.3 droop requirements.

6.7 Return Loss

Since the TP output on the SiS900 is a current source and since the TP input impedance to the SiS900 is a much higher than the characteristic impedance of the twisted pair cable, the SiS900 offers little or no degradation to the return loss. The return loss is primarily determined by the termination resistor values, the transformer characteristics, and any board parasitic. If the resistor values are chosen correctly and tolerances limited to 1%, then only the transformer and board parasitic contribute significantly to return loss degradation. As such, care should be taken in selecting transformer and in the layout of a PCB so as to meet all the return loss requirements of IEEE 802.3.

6.8 Long Cable

IEEE 802.3 specifies that 10Base-T and 100Base-TX operate over twisted pair cable lengths of between 0-100 meters. The squelch levels can be reduced by 4.5 dB if the receive level adjust bit is appropriately set in the MI serial port Configuration 1 register, which will allow the SiS900 to operate

with up to 150 meters of twisted pair cable. The equalizer is already designed to accommodate between 0-125 meters of cable.

6.9 Oscillator

The SiS900 requires a 25 Mhz reference frequency for internal signal generation. This 25 MHz reference frequency can be generated by either connecting an external 25 Mhz crystal between OSCIN and ground or by applying an external 25 Mhz clock to OSCIN.

If the crystal oscillator is used, it needs only a crystal, and no other external capacitors or other components are required. The crystal must have the characteristics shown in Table 6-4. The crystal must be placed as close as possible to OSCIN and ground pins so that parasitic on OSCIN are kept to a minimum.

Table 6-4 Crystal Specifications

PARAMETER	SPEC
Type	Parallel Resonant
Frequency	25 Mhz +/- 0.01%
Equivalent Series Resistance	25 ohms max
Load Capacitance	18 pF typ
Case Capacitance	7 pF max
Power Dissipation	1mW max

6.10 Power Supply Decoupling

There are five kinds of power/ground except 5VDD and 5VDD_AUX on the SiS900. They are DVDD/DVSS, DVDD_RTC/DVSS_AUX, OVDD/OVSS, OVDD_AUX/OVSS_AUX, AVDD_AUX/AVSS_AUX.

It is recommended that all DVDDs and OVDDs should be connected together as close as possible to SiS900 with a large power plane (3.3Vdc) and all DVDD_AUXs, OVDD_AUXs and AVDD_AUXs are connected together as close as possible to SiS900 with a large power plane (3.3Vdual). The variation of AVDD_AUXs should be kept minimized (within 50mV of each other), otherwise noise may result from.

All DVSSs, OVSSs, DVSS_AUXs, OVSS_AUXs and AVSS_AUXs should also be connected together as close as possible to SiS900 with a large ground plane. The variation of AVSS_AUXs should be kept minimized (within 50mV of each other), otherwise noise my result from.

A 0.01-0.1 μF decoupling capacitor should be connected between each VDD/VSS set as close as possible to the device pins. The value should be chosen on whether the noise from VDD/VSS is high or low frequency. A conservative approach is to use two decoupling capacitors on each VDD/VSS set, one 0.1 μF for low frequency noise and one 0.001μF for high frequency noise on the power supply.

The VDD connection to the transmit transformer center tap shown in Figures 6-1 has to be well decoupled in order to minimize common mode noise injection from the supply into the twisted pair cable. It is recommended that a 0.01 μF decoupling capacitor be placed between the center tap VDD to the SiS900 ground plane. This decoupling capacitor should be physically placed as close as possible to the transformer center tap, preferably within 0.5”.

The PCB layout and power supply decoupling discussed above should provide sufficient decoupling to achieve the following when measured at the device: (I) The resultant AC noise voltage measured across each VDD/VSS set should be less than 100 m Vpp, (2) All VDD's should be within 50 m Vpp of each other, and (3) All VSS 's should be within 50 m Vpp of each other.

6.11 PCB Layout Guideline

6.11.1 Placement

- The distance between SiS900 and transformer and the distance between RJ-45 and transformer should be as short as possible.
- The two termination resistors of TPO± should be placed near SiS900. The termination series resistor and grounding capacitor of TPI± should be placed near transformer.
- The OSC component should not be placed near important signal traces (such as TPO±, TPI± and analog power), transformer and board edge.

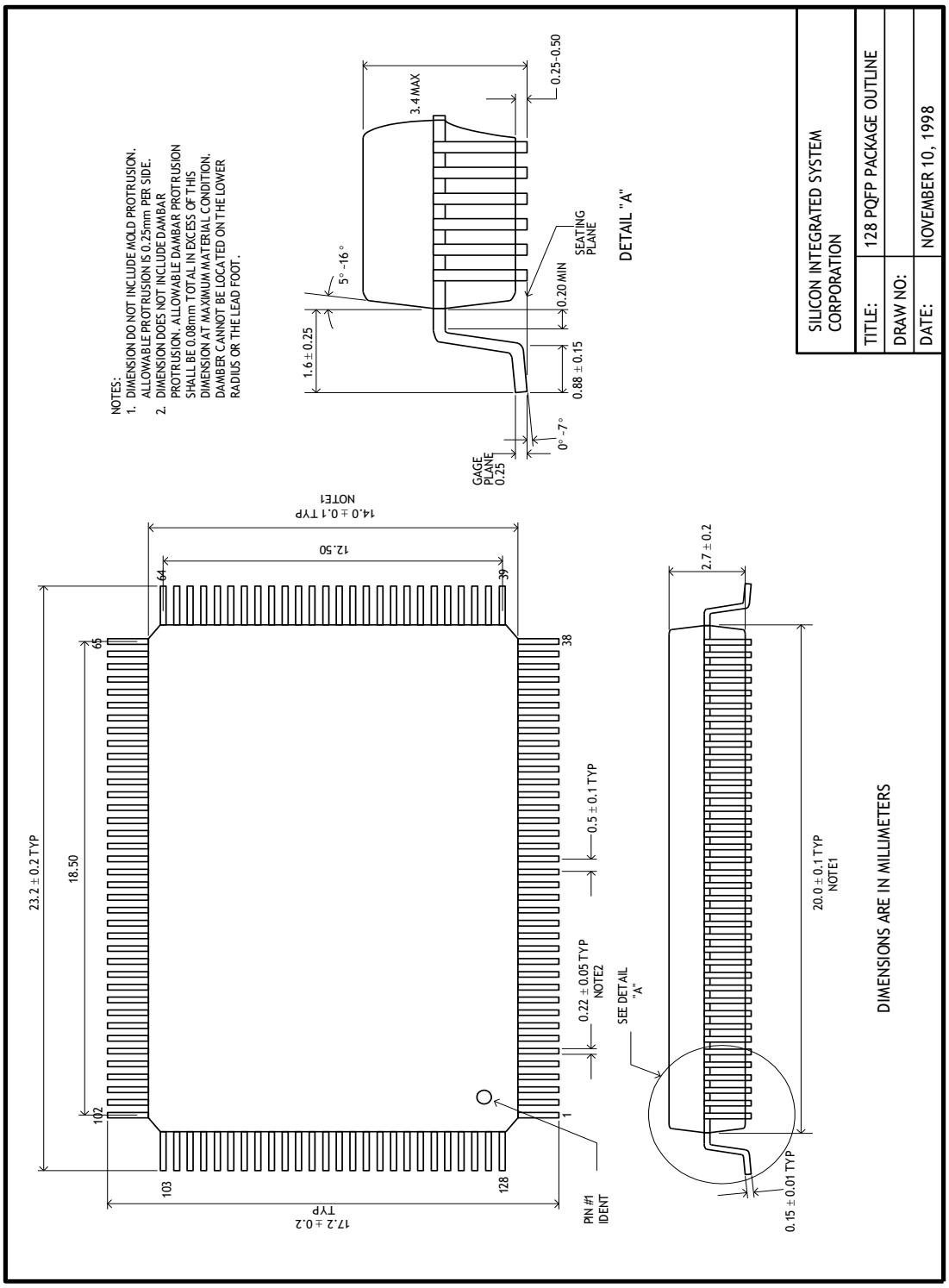
6.11.2 Trace Routing

- The traces between TPO±, TPI± of SiS900 and transformer and the traces between RJ-45 and transformer should be as short as possible.
- Keep TX+ trace close and symmetry to TX- trace, RX+ trace close and symmetry to RX- trace. (no more than 0.1")
- It is recommended TX± and RX± traces turn using arcs.
- It is best not using any vias for the traces of TX± and RX± and using few corners.
- The traces of TX± pair and RX± pair should be kept far away. It is best to place ground plane between these two pair of traces.
- The TX±, RX±, clock and power traces should be as short and wide as possible.

6.11.3 Power and Ground Plane

- The RJ-45 and output side of transformer should use a separated ground plane (chassis ground) which is isolated with the ground plane of the input side of transformer and SiS900. Another way is using no ground plane under the output side of transformer.
- The chassis side ground and the input side ground of transformer should be separated by at least 0.1".
- If possible, separate analog power/ground planes from noisy logic power/ground planes.

7. PHYSICAL DIMENSIONS



APPENDIX A - EEPROM MAP

The SiS900 supports the attachment of an external serial EEPROM. The serial EEPROM stores configuration data for the SiS900. The SiS900 performs an automatic read of 22 bytes of the EEPROM after the auxiliary power up reset de-asserts if the auto load function is enabled.

BYTE ADDR	TAG	DESCRIPTION
00-01h	signature	The signature field is a signature of 0900h, indicating there is a valid EEPROM. If the signature field is not 0900h, auto load function is disabled and the default values are used.
02h	mask	Bit0: 1: Enable "vendorID" and "deviceID" auto load function. 0: Disable "vendorID" and "deviceID" auto load function. Bit1: 1: Enable "sub_vendorID" and "subsystemID" auto load function. 0: Disable "sub_vendorID" and "subsystemID" auto load function. Bit2: 1: Enable "pmc" auto load function. 0: Disable "pmc"auto load function. Bit3: 1: Enable "Ethernet ID" auto load function and power up Magic Packet™wake up enable. 0: Disable "Ethernet ID" auto load function and power up Magic Packet™ wake up disable. Bit4-Bit7: reserved.
03h		RESEVERED
04-05h	vendorID	PCI vendor ID, PCI configuration space address 00-01h.
06-07h	deviceID	PCI device ID, PCI configuration space address 02-03h.
08-09h	sub_vendorID	PCI subsystem vendor ID, PCI configuration space address 2C-2Dh.
0A-0Bh	subsystemID	PCI subsystem ID, PCI configuration space address 2E-2Fh.
0C-0Dh	pmc	PCI power management capabilities, PCI power management register offset2.
0E-0Fh		Reserved.
10-11h	ethernetID	Ethernet ID word byte0 and byte1.
12-13h	ethernetID	Ethernet ID word byte2 and byte3.
14-15h	ethernetID	Ethernet ID word byte4 and byte5.
16-17h		EEPROM checksum