VIA PN800 detailed spec sheet

1.Defines Highly Integrated Solutions for Full Featured Value PC Mobile Designs

- High Performance UMA North Bridge: Integrated Pentium 4 North Bridge with 800 MHz FSB support and UniChrome Pro 3D / 2D Graphics & Video Controllers in a single chip

- Advanced 64-bit memory controller supporting DDR400 / 333 / 266 SDRAM

- Combines with VIA VT8235-CE / VT8237 South Bridge for integrated 10/100 LAN, Audio, ATA133 IDE, LPC, USB 2.0 and Serial ATA (VT8237)

- 1.5V Core and Pentium 4 AGTL+ I/O

- 37.5 x 37.5mm HSBGA (Ball Grid Array with Heat Spreader) package with 829 balls and 1mm ball pitch

- Pin compatible with PM800, PM880, PN880, PT800A and PT880 Pentium 4 North Bridges

2.High Performance CPU Interface

- Supports Intel 800 / 533 / 400 MHz FSB Pentium 4 and Pentium M processors

- Supports Intel Hyper-Threading Technology

- Supports DBI (Dynamic Bus Inversion) and Data, Address, Response Parity

- Twelve outstanding transactions (twelve level In-Order Queue (IOQ))

- AGP v3.0 compliant 8x / 4x transfer modes with Fast Write support

- 1.5V AGP I/O interface

- Pipelined split-transaction long-burst transfers up to 2.1 GB/sec

- Supports Side Band Addressing (SBA) mode

- Supports Flush / Fence commands

- Supports DBI (Dynamic Bus Inversion)

- Asynchronous AGP and CPU interface

- Thirty-two level request queue for read and write

- One-hundred-twenty-eight level (quadwords) of read data FIFO

- Sixty-four level (quadwords) of write data FIFO

- Graphics Address Relocation Table (GART)

- One level TLB structure

- Built-in Phase Lock Loop circuitry for optimal skew control within and between clocking regions

3.Full Featured Accelerated Graphics Port (AGP) Controller

- Sixteen entry fully associative page table

- LRU replacement scheme

- Supports DDR400 / 333 / 266 memory types with 2.5V SSTL-2 DRAM interface

- Supports mixed 64 / 128 / 256 / 512 / 1024Mb DDR SDRAMs in x8 and x16 configurations

- Supports CL 2 / 2.5 for DDR266 / 333 and CL 2.5 / 3 for DDR400

- Supports 4 unbuffered double-sided DIMMs and up to 8 GBytes of physical memory

- Two sets of memory data, address and control signals each of which drives up to 2 DIMMs

- Programmable timing / drive for memory address, data and control signals independently for each signal set

- DRAM interface pseudo-synchronous with host CPU for optimal memory performance

- Concurrent CPU, AGP / integrated graphics controller and V-Link access for minimum memory access latency

- Bank interleave and up to 16-bank page interleave (i.e., 16 pages open simultaneously) based on LRU to effectively reduce memory access latency

- Seamless DRAM command scheduling for maximum DRAM bus utilization (e.g., precharge other banks while accessing the current bank)

4.Advanced High-Performance DDR400 SDRAM Controller

- CPU Read-Around-Write capability for non-stalled operation

- Speculative DRAM read before snoop result to reduce PCI master memory read latency

- Supports Burst Read and Write operations with burst length of 4 or 8

- Twelve cache lines (96 quadwords) of integrated CPU-to-DRAM write buffers and twelve separate cache lines of CPU-to-DRAM read prefetch buffers

- Optional dynamic Clock Enable (CKE) control for DRAM power reduction during normal system state (S0)

- Supports self-refresh and CAS-before-RAS DRAM refresh with staggered RAS timing

- Supports 66 MHz, 4x and 8x transfer modes, Ultra V-Link Host interface with 1 GB/sec total bandwidth

- Full duplex transfers with separate command / strobe for 4x and 8x modes

- Request / Data split transaction

- Transaction assurance for V-Link Host-to-Client access eliminates V-Link Host-Client Retry cycles

- Intelligent V-Link transaction protocol to eliminate data wait-states and throttle transfer latency to avoid data overflow

5.High Bandwidth 1 GB / Sec 16-Bit “Ultra V-Link” Host Controller

- Highly efficient V-Link arbitration with minimum overhead

- ACPI 2.0 and PCI Bus Power Management 1.1 compliant

- Supports Suspend-to-DRAM (STR) and DRAM self-refresh

- Supports dynamic Clock Enable (CKE) control for DRAM power reduction during normal system state (S0)

- Supports SMI, SMM, and STPCLK mechanisms

- Supports Enhanced Intel Speedstep™ Technology

- Low-leakage I/O pads

6.Advanced System Power Management Support

- Optimized Unified Memory Architecture (UMA)

- Supports 16 / 32 / 64 MB Frame Buffer sizes

- 200 MHz Graphics Engine Clock

- Two independent 128-bit data paths between North Bridge and graphics core to improve video performance, one for frame buffer access and one for texture / command access

7.Integrated Graphics with 2D / 3D / Video Controllers

- PCI v2.2 compliant (for control and configuration)

- AGP v3.0 compliant (for control and data transfer)

- 128-bit 2D graphics engine

- Hardware 2D rotation

- Supports ROP3, 256 operations

- Supports 8bpp, 15/16bpp and 32bpp color depth modes

- BitBLT (Bit BLock Transfer) functions including alpha BLTs

- True-color hardware cursor (64x64x32bpp) with 256-level blending effect

- Color expansion, source Color Key and destination Color Key

- Bresenham line drawing / style line function

- Transparency mode

- Window clipping

- Text function

8.2D Acceleration

- 3D Graphics Processor

– 128-bit 3D graphics engine

– Dual pixel rendering pipes

– Dual texture units

– Floating-point setup engine

– Internal full 32-bit ARGB format for high rendering quality

– 8K Texture Cache

- Capability

– Supports ROP2

– Supports various texture formats including 16/32bpp ARGB, 8bpp Palletized (ARGB), YUV 422/420 and compressed texture (DXTC)

– Texture sizes up to 2048x2048

– Microsoft DirectX texture compression

– High quality texture filter for Nearest, Linear, Bi-linear, Tri-linear, and Anisotropic modes

– Flat and Gouraud shading

– Vertex Fog and Fog Table

– Z-Bias, LOD-Bias, Polygon offset, Edge Anti-aliasing and Alpha Blending

– Bump mapping and cubic mapping

9.3D Acceleration

– Hardware back-face culling

– Specular lighting

- Performance

– Two textures per pass

– Triangle rate up to 4.5 million triangles per second

– Pixel rate up to 200 million pixels per second for 2 textures each

– Texel bilinear fill rate up to 400 million texels per second

– High quality dithering

- High Quality Video Processor

– RGB555, RGB565, RGB8888 and YUV422 video playback formats

– High quality 5-tap horizontal and 5-tap vertical scaler (up or down) for both horizontal and vertical scaling

(linear interpolation for horizontal and vertical p-scaling and filtering for horizontal and vertical downscaling)

– Independent graphics and video gamma tables

– 2 sets of Color and Chroma Key support

– Color enhancement for contrast, hue, saturation and brightness

– YUV-to-RGB color space conversion

– Display rotation in clockwise and counter-clockwise directions

10.Video Acceleration

– Bob, Weave, Median-filter and Adaptive de-interlacing modes

– 3:2 / 2:2 pull-down detection

– De-blocking mode support

– Combining of many special effects such as filter, scaling up or down, sub-picture blending, de-interlacing and deblocking to one pass process

– Tear-free double / triple buffer flipping

– Input video vertical blanking or line interrupt

– Video gamma correction

- Video Overlay

– Simultaneous graphics and TV video playback overlay

– Supports video window overlays

– Supports both YUV and RGB format Chroma Key

– Supports 16 operations for Color and Chroma Key

– Hardware sub-picture blending

- MPEG Video Playback

– MPEG-2 hardware VLD (Various Length Decode), iDCT, and motion compensation for full speed DVD and MPEG-2 playback at full D1 resolution

– MPEG-4 ASP (Advanced Simple Profile) Level 5 with GMC (Global Motion Compensation) L0/L1 and ¼ pixel MC support for high video quality and performance

– High quality DVD and streaming video playback

– DVD playback auto-flipping

– DVD sub-picture playback overlay

- Video Capture Capability

– 8-bit capture port following ITU-R BT656, VIP 1.1 and VIP 2.0 standards supporting 16 / 32-bit RGB and YUV422 video capture formats

– Video capture and playback tear free auto flipping

– Multiplexed on Digital Video Port 0 (DVP0 selectable as Capture-In or TV-Out)

– External Hsync / Vsync support

- Built-in reference voltage generator and monitor sense circuits

- Automatic panel power sequencing and VESA DPMS (Display Power Management Signaling) CRT powerdown

- External I/O signal controls enabling of graphics accelerator into standby / suspend-off state

- Dynamic clock gating for inactive functions to achieve maximum power savings

- I2C Serial Bus and DDC / E-DDC Monitor Communications for Plug-and-Play configuration

11.Advanced Graphics Power Management Support

- CRT Display Interface

- Digital Video Port with Support for TV Out or Video Capture In

- Digital Video Port with Support for TV Out or External DVI Transmitter

- 24-Bit / Dual-12-Bit FPD Interface to External LVDS Transmitter

- Two Display Engines

– Provides two independent display engines, each of which can display completely different information at different resolutions, pixel depths, and refresh rates (supports different images on different displays simultaneously)

– CRT, FPD, DVI monitor and TV refresh rates are independently programmable for optimum image quality

– Improved display flexibility with simultaneous FPD / CRT, FPD / TV, FPD / DVI and other combined operations

- CRT Display

– CRT display interface with 24-bit true-color RAMDAC up to 350 MHz pixel rate with gamma correction capability

– Supports CRT resolutions up to 1920 x 1440

- TV-Out Interface

– 12-bit interface to external TV encoder for ATSC, NTSC or PAL TV display

– Selectable to use either Digital Video Port 0 (DVP0) or Digital Video Port 1 (GDVP1)

12.Extensive Display Support for External Video Output

– Supports 3.3V signaling on DVP0 and 1.5V signaling on GDVP1

- 12-Bit DVI Transmitter Interface

– Option of AGP-multiplexed digital video port 1 (GDVP1) when that port is not being used for TV out

– Supports external DVI transmitter for a driving a DVI monitor

– Double-data-rate data transfer with clock rates up to 165 MHz

– Built-in digital phase adjuster to fine-tune signal timing between clock and data bus

- 24-Bit Flat Panel Display (FPD) Interface

– Multiplexed with external AGP port pins

– Supports 18/24-bit FPD interface with external LVDS transmitter chip using single or double-data rate data transfer

– Supports panel resolutions up to 1600x1200

- Dual 12-Bit Flat Panel Display (FPD) Interface

– Alternate operating mode of FPD interface with external LVDS transmitters

– Single or separate sets of clock and sync signals

– Supports panel resolutions up to 1600x1200

- Microsoft DirectX 7.0, 8.0 and 9.0 compatible

- Microsoft DirectX Texture Compression (DXTC / S3TC)

13.Full Software Support

- Supports OpenGL

- Drivers for major operating systems and APIs: Windows 9x/ME, Windows 2000, Windows XP, Direct3DDirectDraw, DirectShow, and OpenGL ICD for Windows 9x/ME and XP

- Windows NT 4.0 Standard VGA driver

- WinXP, WinME and Win98 multi-monitor, extended desktop support

- Independent resolution, refresh rate and color depth for secondary desktop