

VT8605

ProSavage PM133

66 / 100 / 133 MHz

**Single-Chip Slot-1 / Socket-370 North Bridge
for Desktop PC Systems with
Integrated Savage4 AGP4X Graphics Core
plus Advanced Memory Controller
supporting PC100 / PC133 SDRAM
and Virtual Channel Memory (VCM)**

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VIA TECHNOLOGIES, INC.

S3 INC.

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APOLLO PROSAVAGE PM133

66 / 100 / 133 MHz
Single-Chip Slot-1 / Socket-370 North Bridge
for Desktop PC Systems with
Integrated Savage4 AGP 4X Graphics core
plus Advanced Memory Controller
supporting PC100 / PC133 SDRAM
and Virtual Channel Memory (VCM)

- **Defines Integrated Solutions for Value PC Desktops**

- High performance SMA North Bridge: Integrated VIA Apollo Pro133A and S3[®] Savage4™ in a single chip
- The “P6-bus Desktop PC” member of VIA’s Apollo ProSavage integrated graphics product line
- 64-bit Advanced Memory controller supporting PC100/PC133 SDRAM and VCM
- AGP Expansion Interface supporting AGP 4x, 2x, or 1x external AGP graphics card upgrade
- Combines with VIA VT8231 PCI-LPC South Bridge for state-of-the-art power management

- **High Performance CPU Interface**

- Slot 1 (Intel[®] Pentium[®] II and Pentium III) and Socket 370 (VIA Technologies VIA-Cyrix-III™ and Intel Celeron™)
- 66/100/133 MHz CPU Front Side Bus (FSB)
- Built-in Phase Lock Loop circuitry for optimal skew control within and between clocking regions
- Five outstanding transactions (four In-Order Queue (IOQ) plus one output latch)
- Dynamic deferred transaction support

- **Advanced High-Performance DRAM Controller**

- DRAM interface runs synchronous (66/66, 100/100, 133/133) mode or pseudo-synchronous (66/100, 100/66, 100/133, 133/100) mode with FSB
- Concurrent CPU, AGP, and PCI access
- Supports standard SDRAM and VCM SDRAM memory types
- Support 3 DIMMs or 6 banks for up to 1.5 GB of DRAM (256Mb DRAM technology)
- 64-bit data width
- Supports maximum 8-bank interleave (8 pages open simultaneously); banks are allocated based on LRU
- SDRAM X-1-1-1-1-1-1 back-to-back accesses

- **Accelerated Graphics Port (AGP) Controller**

- AGP Specification Rev. 2.0 compliant
- Supports 266 MHz 4x mode for AD and SBA signaling
- Supports SideBand Addressing (SBA) mode (non-multiplexed address/data)
- Pipelined split-transaction long-burst transfers up to 1GB/sec
- Intelligent request reordering for maximum AGP bus utilization
- AGP Expansion graphics override the integrated graphics by default with no SMA frame buffer

- **Integrated Savage4 2D/3D/Video Accelerator**

- Optimized Shared Memory Architecture (SMA)
- 2 to 32 MB frame buffer using system memory
- Floating point triangle setup engine
- Single cycle 128-bit 3D architecture
- 8M triangles/second setup engine
- 140M pixels/second trilinear fill rate
- Full AGP 4x, including sideband addressing and execute mode
- S3 DX7 texture compression (S3TC)
- Next generation, 128-bit 2D graphics engine
- High quality DVD video playback
- Flat panel monitor support
- 2D/3D resolutions up to 1920x1440

- **3D Rendering Features**

- Single-pass multiple textures
- Anisotropic filtering
- 8-bit stencil buffer
- 32-bit true color rendering
- Specular lighting and diffuse shading
- Alpha blending modes
- Massive 2K x 2K textures
- MPEG-2 video textures
- Vertex and table fog
- 16 or 24-bit Z-buffering
- Sprite anti-aliasing, reflection mapping, texture morphing, shadows, procedural textures and atmospheric effects

- **2D Hardware Acceleration Features**

- ROP3 Ternary Raster Operation BitBLTs
- 8, 16, and 32 bpp mode acceleration

- **Motion Video Architecture**

- High quality up/down scaler
- Planar to packed format conversion
- Motion compensation for full speed DVD playback
- Hardware subpicture blending and highlights
- Multiple video windows for video conferencing
- Contrast, hue, saturation, brightness and gamma controls
- Digital port for NTSC/PAL TV encoders

- **Flat Panel Monitor Support**

- 12-bit digital interface for Flat Panel encoders
- Auto-expansion and centering for VGA modes
- Support for all resolutions up to 1280x1024
- Digital Visual Interface (DVI) 1.0 compliant

- **Concurrent PCI Bus Controller**

- PCI 2.2 compliant, 32-bit 3.3V PCI interface with 5V tolerant inputs
- Supports up to 5 PCI masters
- PCI to system memory data streaming support
- Delay transaction from PCI master accessing DRAM
- Symmetric arbitration between Host/PCI bus for optimized system performance

- **Advanced System Power Management Support**

- Dynamic power down of SDRAM (CKE)
- Independent clock stop controls for CPU / SDRAM, AGP, and PCI bus
- PCI and AGP bus clock run and clock generator control
- VTT suspend power plane preserves memory data
- Suspend-to-DRAM and self-refresh power down
- Low-leakage I/O pads
- ACPI 1.0 and PCI Bus Power Management 1.1 compliant

- **Full Software Support**

- Drivers for major operating systems and APIs: [Windows® 9x, Windows NT 4.0, Windows 2000, Windows 3.x, OS/2® 2.1/3.0 (Warp™), Linux, Direct3D™, DirectDraw™ and DirectShow™, OpenGL™ ICD for Windows 9x, NT, and 2000]
- North Bridge/Chipset and Video BIOS support

- **Additional Features**

- 300 MHz RAMDAC with Gamma Correction
- I²C Serial Bus and DDC Monitor Communications
- 2.5V Core and Mixed 3.3V/5V Tolerant and GTL+ I/O
- 35 x 35mm PBGA package with 552 balls

OVERVIEW

The VT8605 is a high performance, cost-effective and energy efficient SMA chip set for the implementation of AGP / PCI / LPC desktop personal computer systems with 66 MHz, 100 MHz and 133 MHz CPU host bus (“Front Side Bus”) frequencies and based on 64-bit Socket-370 (VIA-Cyrix-III and Intel Celeron) and Slot-1 (Intel Pentium II and Pentium-III) super-scalar processors. In other words, the VT8605 is the P6-bus version of the Apollo ProSavage integrated graphics product line targeted at desktop PCs, developed by the VIA / S3 joint venture. The VT8605 may also be referred to by product name PM133 in VIA and S3 marketing literature.

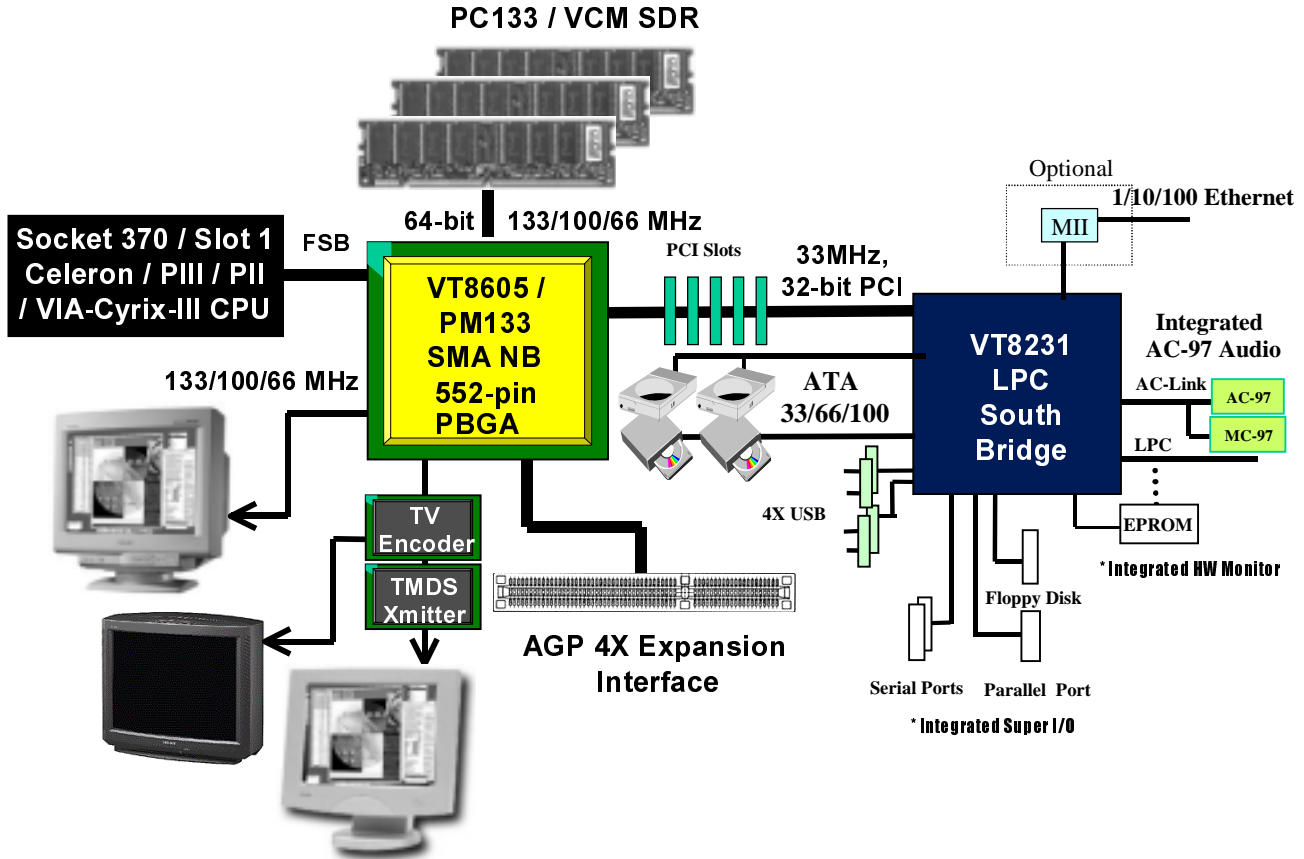


Figure 1. VT8605 System Block Diagram with VT8231 PCI-LPC South Bridge

The VT8605 integrates VIA’s VT82C694X system controller and S3’s Savage4 2D/3D graphics accelerator into a single 552 BGA package. The VT8605 SMA system controller provides superior performance between the CPU, DRAM, AGP bus, and PCI bus with pipelined, burst, and concurrent operation.

The VT8605 supports six banks of DRAMs up to 1.5Gbyte of system memory with 256Mbit DRAM technology. The DRAM controller supports standard Synchronous DRAM (SDRAM) and Virtual Channel SDRAM (VC SDRAM), in a flexible mix / match manner. The Synchronous DRAM interface allows zero wait state bursting between the DRAM and the data buffers at 66/100/133 MHz. The six banks of DRAM can be composed of an arbitrary mixture of 1M / 2M / 4M / 8M / 16M / 32MxN DRAMs. The DRAM controller can run at either the host CPU bus frequency (66 /100 /133 MHz) or pseudo-synchronous to the CPU bus frequency (66/100/133 MHz) with built-in PLL timing control.

The VT8605 system controller also supports full AGP v2.0 capability for maximum bus utilization including 1x/2x/4x mode transfers, SBA (SideBand Addressing), Flush/Fence commands, and pipelined grants. An eight level request queue plus a four level post-write request queue with thirty-two and sixteen quadwords of read and write data FIFO’s respectively are included for

deep pipelined and split AGP transactions. A single-level GART TLB with 16 full associative entries and flexible CPU / AGP / PCI remapping control is also provided for operation under protected mode operating environments. Both Windows-95 VXD and Windows-98 / Windows 2000 miniport drivers are supported for interoperability with integrated Savage4 graphics, AGP Expansion graphics, and DVD-capable multimedia accelerators.

The VT8605 supports two 32-bit 3.3 / 5V system buses (one AGP and one PCI) that are synchronous / pseudo-synchronous to the CPU bus. The chip also contains a built-in bus-to-bus bridge to allow simultaneous concurrent operations on each bus. Five levels (doublewords) of post write buffers are included to allow for concurrent CPU and PCI operation. For PCI master operation, forty-eight levels (doublewords) of post write buffers and sixteen levels (doublewords) of prefetch buffers are included for concurrent PCI bus and DRAM/cache accesses. The chip also supports enhanced PCI bus commands such as Memory-Read-Line, Memory-Read-Multiple and Memory-Write-Invalid commands to minimize snoop overhead. In addition, advanced features are supported such as snoop ahead, snoop filtering, L1 write-back forward to PCI master, and L1 write-back merged with PCI post write buffers to minimize PCI master read latency and DRAM utilization. Delay transaction and read caching mechanisms are also implemented for further improvement of overall system performance.

The VT8605 also integrates S3[®]'s Savage4[™] graphics accelerator into a single chip. The VT8605 brings mainstream graphics performance to the Value PC with leading-edge 2D, 3D and DVD video acceleration into a cost effective package. Based on its capabilities, the VT8605 is an ideal solution for the consumer, corporate desktop users and entry level professionals.

The industry's first integrated AGP 4X solution, the VT8605 combines AGP 4X with S3's DX6 texture compression (S3TC) and massive 2Kx2K textures to deliver unprecedented 3D performance and image quality for the Value PC desktop market.

The 352-pin VT8231 BGA PCI-LPC bridge supports four levels (doublewords) of line buffers, type F DMA transfers and delay transaction to allow efficient PCI bus utilization and (PCI-2.1 compliant). The VT8231 also includes an integrated Super I/O, integrated DS12885 style real time clock with extended 256 byte CMOS RAM, integrated master mode enhanced IDE controller with full scatter / gather capability and extension to UltraDMA-33/66/100 for 33/66/100 MB/sec transfer rate, integrated four USB interface with root hub and two function ports with built-in physical layer transceivers, Distributed DMA support, integrated AC-97 link for basic audio and HSP based modem functions, integrated hardware monitoring and OnNow / ACPI compliant advanced configuration and power management interface. VT8231 also has an integrated MAC and 10Mbit PHY for LAN connection. It can bypass the internal PHY with external home PNA with a 1Mbit PHY or a 10/100Mbit PHY through the MII interface.

For sophisticated power management, the VT8605 provides independent clock stop control for the CPU / SDRAM, PCI, and AGP buses and Dynamic CKE control for powering down of the SDRAM. A separate suspend-well plane is implemented for the SDRAM control signals for Suspend-to-DRAM operation. Coupled with the VT8231 south bridge chip, a complete power conscious PC main board can be implemented with no external TTLs.

High-Performance 3D Accelerator

Featuring a new super-pipelined 128-bit engine, the VT8605 utilizes a single cycle architecture that provides high performance along with superior image quality. Several new features enhance the 3D architecture, including single-pass multitexturing, full scene anti-aliasing, anisotropic filtering, and an 8-bit stencil buffer. The VT8605 also offers the industry's only simultaneous usage of single-pass multitexturing and single-cycle trilinear filtering – enabling stunning image quality without performance loss. The VT8605 further enhances image quality with true 32-bit color rendering throughout the 3D pipeline to produce more vivid and realistic images. The VT8605's advanced triangle setup engine provides industry leading 3D performance for a realistic user experience in games and other interactive 3D applications. The 3D engine is optimized for AGP texturing from system memory.

128-bit 2D Graphics Engine

The VT8605's advanced 128-bit 2D graphics engine delivers high-speed 2D acceleration for productivity applications. Several enhancements have been made to the 2D architecture to optimize SMA performance and to provide acceleration in all color depths.

DVD Playback and Video Conferencing

The VT8605 provides the ideal architecture for high quality MPEG-2 based DVD applications and video conferencing. For DVD playback, the VT8605's video accelerator offloads the CPU by performing the planar to packed format conversion and motion compensation tasks, while its enhanced scaling algorithm delivers incredible full-screen video playback. For video conferencing, the VT8605's multiple video windows enable a cost effective solution.

Flat Panel Desktop Monitor Support

The VT8605 has the capability of displaying graphics on TFT flat panel desktop monitors using a 12-bit digital interface to an external encoder. The VT8605 also supports autoexpansion and centering of all VGA text and graphics modes to ensure that the entire flat panel display will be utilized. All resolutions are supported up to 1280x1024. The solution is Digital Visual Interface 1.0 specification compliant.

High Screen Resolution CRT Support

Resolutions Supported	System Memory Frame Buffer Size (8MB Default)		
	4 MB	8 MB	16/32 MB
640x480x8/16/32	✓	✓	✓
800x600x8/16/32	✓	✓	✓
1024x768x8/16/32	✓	✓	✓
1280x1024x8	✓	✓	✓
1280x1024x16	✓	✓	✓
1280x1024x32		✓	✓
1600x1200x8	✓	✓	✓
1600x1200x16	✓	✓	✓
1600x1200x32		✓	✓
1920x1440x8	✓	✓	✓
1920x1440x16		✓	✓

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Table 10. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
T _A	Ambient operating temperature	0	55	°C	1
T _C	Case operating temperature	0	110	°C	1
T _S	Storage temperature	-55	125	°C	1
V _{IN}	Input voltage	-0.5	V _{RAIL} + 10%	Volts	1, 2
V _{OUT}	Output voltage	-0.5	V _{RAIL} + 10%	Volts	1, 2

Note 1: Stress above the conditions listed may cause permanent damage to the device. Functional operation of this device should be restricted to the conditions described under operating conditions.

Note 2. V_{RAIL} is defined as the V_{CC} level of the respective rail. The CPU interface can be 3.3V or 2.5V. Memory can be 3.3V only. PCI can be 3.3V or 5.0V. Video can be 3.3V or 5.0V. Flat Panel can be 3.3V only. AGP can be 1.5V (4x transfer mode) or 3.3V (2x transfer mode).

DC Characteristics

T_A = 0-55°C, V_{RAIL} = V_{CC} +/- 5%, V_{CORE} = 2.5V +/- 5%, GND=0V

Table 11. DC Characteristics

Symbol	Parameter	Min	Max	Unit	Condition
V _{IL}	Input Low Voltage	-0.50	0.8	V	
V _{IH}	Input High Voltage	2.0	V _{CC} +0.5	V	
V _{OL}	Output Low Voltage	-	0.55	V	I _{OL} =4.0mA
V _{OH}	Output High Voltage	2.4	-	V	I _{OH} =-1.0mA
I _{IL}	Input Leakage Current	-	+/-10	uA	0<V _{IN} <V _{CC}
I _{OZ}	Tristate Leakage Current	-	+/-20	uA	0.55<V _{OUT} <V _{CC}
I _{CC}	Power Supply Current	-		mA	

AC Timing Specifications

AC timing specifications provided are based on external zero-pf capacitance load. Min/max cases are based on the following table:

Table 12. AC Timing Min / Max Conditions

Parameter	Min	Max	Unit
5.0V Power	4.75	5.25	Volts
3.3V Power (I/O Pads, VCCQ for 2x transfer mode)	3.135	3.465	Volts
2.5V Power (Internal Logic)	2.375	2.625	Volts
1.5V Power (VCCQ for 4x transfer mode)	1.425	1.575	Volts
Temperature	0	55	°C

Drive strength for selected output pins is programmable. See Rx6D for details.

MECHANICAL SPECIFICATIONS

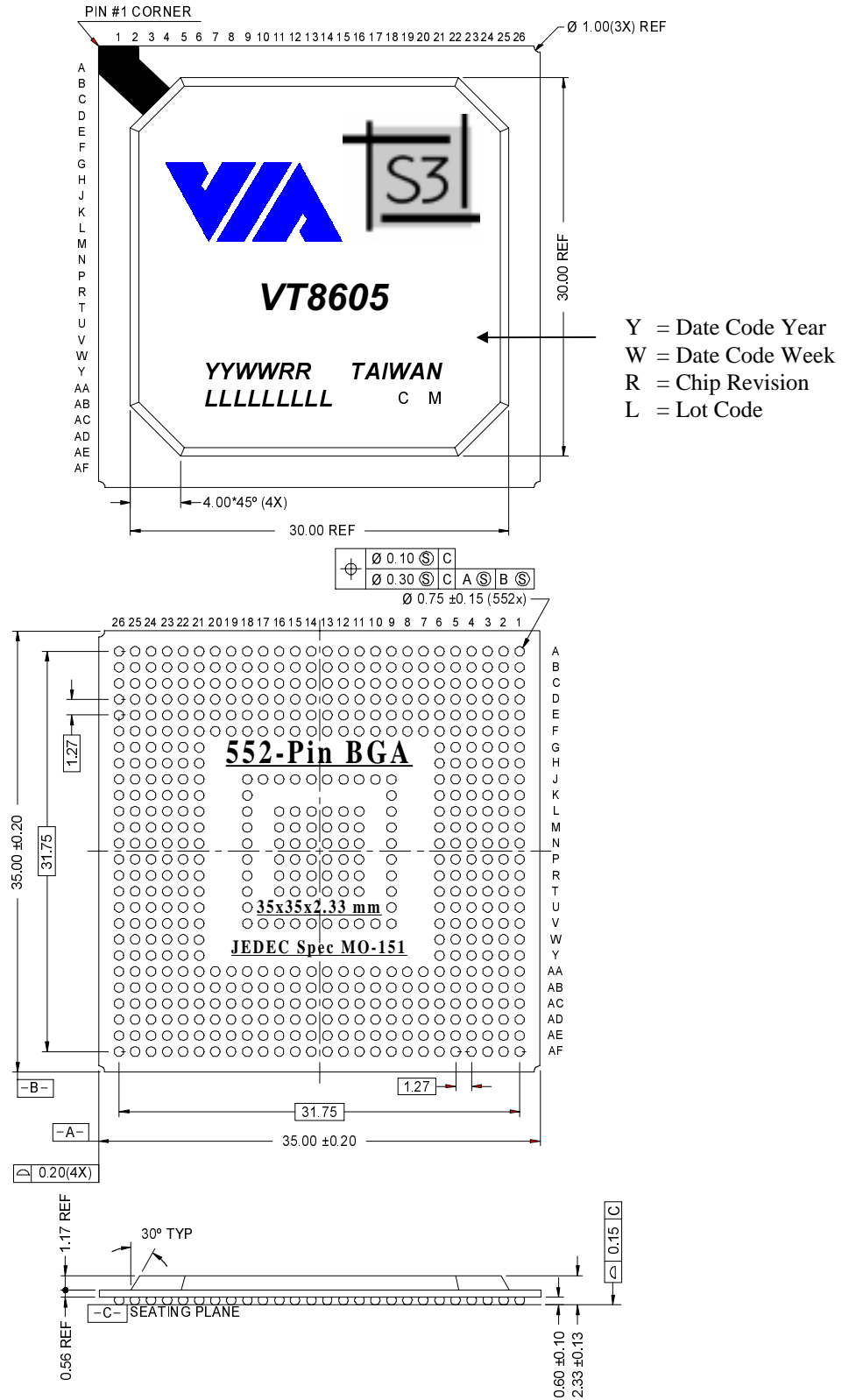


Figure 8. Mechanical Specifications - 552-Pin Ball Grid Array Package